

Digital Radio and Its Application in the HF (2-30 MHz) Band

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For Jo, my wonderful wife

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N C Davies, May 2004

Abstract

Digital Radio and Its Application in the HF (2-30 MHz) Band

Nigel Davies

The propagation environment at high frequencies (HF, 2-30 MHz) has a significant impact on the performance of radio systems (especially data communications). However, the ability to communicate information over very long ranges using ionospheric propagation paths without any intermediate infrastructure makes the use of HF attractive for many applications. In order to increase the utility of HF communications there is a strong desire to increase HF data rates. Currently data rates of up to ~2400 bps can be reliably achieved in standard 3 kHz HF channel allocations. Whilst further increases in data rate within the confines of these narrowband frequency allocations is likely, the use of larger bandwidths (contiguous or otherwise) appears to offer potential for much greater throughputs. This requires a greater understanding of the characteristics of wideband channels and also requires transmitting and receiving equipment capable of wideband/multi-channel operation.

New waveforms have been proposed for the transmission of higher data rates in extended channel bandwidths (6 kHz). The results of laboratory measurements and analysis of data collected during on-air trials of a number of 16 kbps waveforms are presented. Analysis indicates that operation over surface wave and benign skywave channels is possible, demonstrating the benefit of exploiting greater channel bandwidths.

Suitable architectures for the implementation of wideband and multi-channel digital HF radios (software radios) have been investigated. The work presented indicates that it is now possible, for the first time, to construct high performance, direct sampling wideband digital HF receivers. In such a receiver the entire HF band is digitised and then all subsequent processing is undertaken digitally. Conceptually this would allow an arbitrary number of channels to be simultaneously received using a single RF front-end and digitiser. With careful design performance comparable with that of the high

performance conventional super-heterodyne single channel receivers can be obtained. A prototype wideband multi-channel digital HF transceiver with this architecture has been implemented and its performance shown to agree with that predicted.

A particular challenge in complex systems such as software radios is the deployment of software across a number of heterogeneous processors. A new asynchronous, event-based, processing architecture which employs messaging to allow processing tasks to be effectively distributed across a multiple processors and buses is proposed. It has been implemented on the digital transceiver platform and its effectiveness has been demonstrated.

A new low-power pulse-compression oblique HF ionospheric sounder, known as WHISPER, has been developed. This sounder has been implemented as a software application on the wideband HF digital transceiver. Waveforms suitable for making wideband (~80 kHz) measurements of the channel time varying complex impulse response have been designed. These have been used to make measurements on a 170 km path in the UK during Spring 2001. The results of these measurements have been analysed and confirm the ability of the sounding instrument to measure the channel scattering function and the amplitude and phase within individual modes. A number of possible directions for further analysis, pertinent to the design of wideband HF modems, have been proposed.

Contents

Acknowledgements.....	iii
Abstract.....	iv
Contents	vi
List of Figures.....	ix
List of Abbreviations	xv
Chapter 1. Introduction	1
1.1 Structure of Thesis	2
1.2 Original Work	4
Chapter 2. The HF Propagation Environment and Its Impact on Communications.....	7
2.1 Surface Wave Propagation.....	7
2.2 Sky Wave Propagation.....	7
2.3 NVIS Propagation	16
2.4 Impact of Propagation on Radio Waves.....	16
2.5 Propagation Diversity.....	23
2.6 Propagation at Different Latitudes	24
2.7 Propagation of Wideband Signals.....	25
2.8 Noise and Interference	27
2.9 HF Channel Models and their Application	30
2.10 HF Propagation – Summary of Principal Characteristics	35
Chapter 3. HF Data Communications.....	37
3.1 Waveforms for Data Communication Over Fading, Multipath Channels.....	37
3.2 Modulation Schemes for Data Communications	38
3.3 MIL-STD-188-110A - a Serial Tone HF Data Communications Waveform.....	54
3.4 High Data Rate HF Communications	56
3.5 Summary	58
Chapter 4. A High Data Rate Modem for Extended Bandwidth Channels.....	59
4.1 Waveform and Modem Processing Description	60
4.2 16 kbps Modem Performance	62
4.3 On-air Trials	69
4.4 Potential Improvements to the Experimental 16 kbps Modem	72
4.5 Comparison of Extended Bandwidth Modem Performance	73

4.6	Application of Extended Bandwidth HDR Modems	75
4.7	Standardisation of Extended Bandwidth HDR HF Modems	76
4.8	Chapter Summary.....	77
Chapter 5.	On the Specification and Design of Digital HF Radios.....	78
5.1	Applicable Technology Developments	79
5.2	Wideband Digital Radio Architectures	80
5.3	HF Receiver Performance Requirements.....	87
5.4	HF Transmitter Performance Requirements	96
5.5	A Direct Sampling Digital HF Receiver	97
5.6	Front End Filter	97
5.7	Digitally Controlled RF Amplifier.....	99
5.8	Analogue-to-Digital Converter (ADC) Performance	99
5.9	Digital Down-Converter (DDC)	110
5.10	A High Performance Direct Sampling Digital HF Receiver.....	115
5.11	An Alternative Single Conversion Wideband Receiver Architecture.....	117
5.12	Chapter Summary.....	119
Chapter 6.	Performance of a Prototype Direct Sampling Digital HF Receiver	120
6.1	Description of Prototype Receiver	120
6.2	Predicted Performance of Prototype Digital HF Receiver	134
6.3	Prototype Receiver Performance Measurements	136
6.4	Improving the Performance of the Prototype Receiver.....	143
6.5	Chapter Summary.....	145
Chapter 7.	A Wideband, Multi-Channel, HF Software Radio.....	146
7.1	Wideband Digital Transceiver Architecture	148
7.2	Digital Transceiver PCI Bus Interface	150
7.3	Digital Transceiver Bus Arbitration CPLD.....	150
7.4	Digital Signal Processing (DSP) Sub-System.....	151
7.5	Dual SHARC DSP Processor Module	154
7.6	Digital Transceiver Configuration and Software Download	156
7.7	Transceiver Digital Interfaces	158
7.8	Frequency Standard Sub-System	160
7.9	Digital Receiver Sub-System	166
7.10	Transmitter Exciter Sub-System	171
7.11	Power Supplies for Analogue Sub-Systems.....	175
7.12	Front End Protection and Filtering Module	175
7.13	Construction Techniques.....	176
7.14	Digital Transceiver Control Software Architecture	178
7.15	Built-in Self Test and Diagnostics	179
7.16	Chapter Summary.....	181
Chapter 8.	A High Performance Event Driven Processing Architecture	182
8.1	Asynchronous, Event Based, Processing Architecture	183

8.2	Digital Transceiver Platform.....	184
8.3	Intelligent Input/Output (I ₂ O) Messaging	186
8.4	Asynchronous Messaging - Software Implementation	190
8.5	Implementation Issues.....	197
8.6	Practical Demonstration of Event Based Processing Architecture	198
8.7	Possible Extensions to the Event Based Processing Architecture	199
8.8	Chapter Summary.....	200
Chapter 9.	Application of Digital Radio to HF Channel Characterisation	201
9.1	Introduction to Ionospheric Channel Sounding	201
9.2	Measuring the Time Varying Complex Channel Impulse Response (CIR)	205
9.3	Implementation of WHISPER – A Wideband HF Channel Sounder ...	207
9.4	Pulse Compression Sounding Waveform Design	210
9.5	Receive Digital Signal Processing	218
9.6	Laboratory Measurements to Verify Sounder Performance	219
9.7	Suggestions for Improvements to the WHISPER Sounder.....	222
9.8	Chapter Summary.....	223
Chapter 10.	Measurement of the Wideband HF Channel using WHISPER.....	224
10.1	Experiment Deployment	224
10.2	Results.....	225
10.3	Suggested Routes for Further Data Analysis	237
10.4	Chapter Summary.....	237
Chapter 11.	Applications of Digital Radio in the HF Band.....	239
11.1	Digital Broadcast Receivers.....	239
11.2	Chirp Sounder	240
11.3	RF Channel Simulator.....	240
11.4	High Performance ALE Systems	241
11.5	Applications in Other Frequency Bands	242
11.6	Applications to Weather Radar	242
Chapter 12.	Conclusions and Recommendations for Further Work	244
12.1	Recommendations for Further Investigation.....	245
References	250

List of Figures

Chapter 2

Figure 2-1	The Earth's Ionosphere and its Principal Regions [Maslin, 5]	8
Figure 2-2	Typical Electron Concentration within the Ionosphere [Davies, 3].....	9
Figure 2-3	Daily Smoothed Sunspot Numbers Illustrating 11 Year Solar Cycle	11
Figure 2-4	Terrestrial Effects of a Solar Disturbance [5, 3]	12
Figure 2-5	Ray Paths as a Function of Elevation at a Single Frequency [Maslin, 5]	14
Figure 2-6	Predicted Propagation Loss and MUF for Frankfurt-to-London Sky wave Circuit	15
Figure 2-7	Position of Day-Night Terminator at 1200Z in December	16
Figure 2-8	Summary of the Causes of Multipath and Dispersion [after Maslin, 5]	19
Figure 2-9	Typical Oblique HF Ionogram (Malvern to Farnborough 17:31 20- 03-200)	20
Figure 2-10	Effective Noise Figure of a Loss-less Isotropic Antenna Due to External Noise in the HF Band [ITU, 29].....	28
Figure 2-11	Predicted Congestion from Gott-Laycock Occupancy Model	29
Figure 2-12	Block diagram of Watterson model.	32

Chapter 3

Figure 3-1	Components of a Generic Data Communications System	38
Figure 3-2	On-Off Keying (OOK).....	40
Figure 3-3	Non-coherent Matched Filter Structure	41
Figure 3-4	Frequency Shift Keying (FSK)	42
Figure 3-5	M=8, M-ary Multi-Frequency Shift Keying (MFSK).....	43
Figure 3-6	Binary Phase Shift Keying (BPSK)	44
Figure 3-7	8-PSK Constellation.....	45
Figure 3-8	QPSK/MPSK/QAM Modulator	45
Figure 3-9	16-QAM Constellation.....	46
Figure 3-10	BER Performance of Various Modulation Schemes in an AWGN Channel	48
Figure 3-11	Linear Transverse Equaliser.....	49
Figure 3-12	Decision Feedback Equaliser (DFE).....	50
Figure 3-13	Performance of Various Forward Error Correction Codes	53
Figure 3-14	Operation of an (m×n) Block Interleaver.....	54
Figure 3-15	Structure of MIL-STD-188-110A waveform.....	55
Figure 3-16	Measured Performance of 1200 bps MIL-STD-188-110A Modem (BER=10 ⁻³).....	56
Figure 3-17	Current Progress in Development of HF Data Communications (to 2001)	57

Chapter 4

Figure 4-1	16 kbps Modem Waveform Structure	61
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Figure 4-2	16 QAM Constellation Employed in the 16 kbps Modem.....	62
Figure 4-3	16 kbps Modem Laboratory Characterisation.....	63
Figure 4-4	16 kbps ISB Modem Performance in a Gaussian Noise Channel.....	64
Figure 4-5	16 kbps ISB Modem Performance in a Flat Fading Gaussian Noise Channel	64
Figure 4-6	16 kbps ISB Modem Performance in CCIR Good Channel	65
Figure 4-7	16 kbps ISB Modem Performance in CCIR Poor Channel.....	65
Figure 4-8	Constant BER Surface for 16 kbps ISB Modem (HC codec, long interleave).....	66
Figure 4-9	Constant BER Surface for 16 kbps SSB Modem (HC codec, long interleave).....	66
Figure 4-10	Constant BER Surface for 4800 bps MIL-STD-188-110A Modem (un-coded)	67
Figure 4-11	Constant BER Surface for 2400 bps STANAG 4285 Modem (convolutional coder, long interleave).	67
Figure 4-12	Constant BER Surface for 16 kbps ISB Modem using HC Codec and Long Interleave under Rician Channel Conditions	69
Figure 4-13	Configuration for ‘On-Air’ 16 kbps Modem Experiment.....	70
Figure 4-14	Hourly Average BER between Cobbett Hill and Malvern using 16 kbps ISB Modem with HC Codec (histogram shows number of data points in the data set).....	71
Figure 4-15	Diurnal Kilobyte Frame Delivery Statistics between Cobbett Hill and Malvern using 16 kbps ISB Modem with HC Codec.....	72
Figure 4-16	Performance of Extended Bandwidth HDR Waveforms in AWGN Channel	74
Figure 4-17	Performance of Extended Bandwidth HDR Waveforms in a Rician Fading Channel (one non-fading and one –6 dB Gaussian fading mode).....	75

Chapter 5

Figure 5-1	From Conventional Analogue Receiver to Software Radio.....	78
Figure 5-2	A Super-Heterodyne Receiver Architecture.	81
Figure 5-3	Direct Conversion ‘Zero IF’ Receiver Architecture	82
Figure 5-4	Image Suppression in a Quadrature Mixer Due to Amplitude and Phase Imbalance.....	83
Figure 5-5	Super-heterodyne with Zero-IF Stage	84
Figure 5-6	Single Conversion IF-Sampling Receiver.....	85
Figure 5-7	Block Diagram of a Wideband HF Digital Receiver	86
Figure 5-8	Block Diagram of a Wideband Digital Transmitter.....	87
Figure 5-9	Path Loss versus Separation Distance.....	90
Figure 5-10	Snapshot of Measured Signal Power in HF Band [GEC, 99]	91
Figure 5-11	Typical Narrowband Superhet HF Receiver Composite Filter Characteristics [after Pearce, 100]	92
Figure 5-12	Reciprocal Mixing in a Receiver with Frequency Translation	93
Figure 5-13	2 nd and 3 rd Order Intermodulation Product Levels versus Two Tone Input Power	95
Figure 5-14	Wideband Direct Sampling Digital Receiver.....	97
Figure 5-15	Front End Anti-Aliasing Filter Performance Requirement.....	98

Figure 5-16	Error in Sampling Amplitude Due to ADC Aperture Uncertainty (Jitter)	102
Figure 5-17	Predicted AD6644 SNR versus Clock Jitter for Various Analogue Input Frequencies	103
Figure 5-18	Typical High Quality Local Oscillator SSB Phase Noise Specification.....	105
Figure 5-19	ADC Quantisation Errors Due to DNLs [after Brannon, 111].....	106
Figure 5-20	Architecture of High Performance AD6644 14-bit Multi-Stage ADC [Analog, 107].....	106
Figure 5-21	Application of Wideband Dither to Improve ADC SFDR.....	107
Figure 5-22	Improvement in AD6644 Spurious Performance with Addition of a Dither Signal [Analog, 107].....	108
Figure 5-23	Predicted Mean Available Dither Power Due to HF Congestion (Lower Bound).....	109
Figure 5-24	Digital Down-Converter.....	110
Figure 5-25	NCO as a Complex (Quadrature) Direct Digital Synthesiser	112
Figure 5-26	Practical Decimating CIC Filter - Integrator, Decimator and Comb	113
Figure 5-27	Frequency Response of CIC showing Impact of Aliasing (M=100, L=4, R=1).....	113
Figure 5-28	Modelled Frequency Response of CIC Filters as a function of L and R.	114
Figure 5-29	Dynamic Range in the Direct Sampling Digital HF Receiver	114

Chapter 6

Figure 6-1	Block Diagram of Prototype Direct Sampling Digital HF Receiver	121
Figure 6-2	Measured Selectivity of Combined 28 MHz Elliptic Low Pass Filter	123
Figure 6-3	Front-End Filter Group Delay Variation.....	123
Figure 6-4	Prototype Front-End Filter Impedance Matching	124
Figure 6-5	SNA586 GaAs RF Amplifier Test Circuit.....	125
Figure 6-6	MMIC RF Amplifier Test Pieces.....	125
Figure 6-7	SNA-586 GaAs RF Amplifier Characteristics Measured on Network Analyser	126
Figure 6-8	SNA-586 GaAs RF Amplifier Gain and Linearity Measurements	127
Figure 6-9	SNA-586 RF Amplifier 2 nd and 3 rd Harmonic Performance (Extrapolated).....	128
Figure 6-10	Selectivity of 5 th Order Harmonic Filter (Modelled with SPICE)	129
Figure 6-11	Programmable Digital Down-Converter [after Graychip, 124]	131
Figure 6-12	GC4014 DDC NCO Implementation [Graychip, 124]	131
Figure 6-13	GC4014 Numerically Controlled Oscillator (NCO) Spurs [Graychip, 124]	132
Figure 6-14	Frequency Response of GC4014 CFIR Filter (3 kHz Nyquist bandwidth)	133
Figure 6-15	Modelled Performance of GC4014 DDC (3 kHz Nyquist bandwidth)	133
Figure 6-16	Effect of Adding Dither to ADC Input Signal (Input tones are - 20 dBFS)	137
Figure 6-17	Measured Digital Receiver Sensitivity: -158 dBm/Hz.....	137
Figure 6-18	Measured Digital Receiver IMD using 2 tones at -20 dBm.....	138

Figure 6-19	Measured Receiver Instantaneous Dynamic Range with -15 dBm input	139
Figure 6-20	62.208 MHz Sampling Clock Phase Noise (Free Running)	140
Figure 6-21	62.208 MHz Sampling Clock Performance (VCXO locked to TCXO)	141
Figure 6-22	62.208 MHz Sampling Clock Phase Noise (VCXO/TCXO/Ext. Standard)	141
Figure 6-23	Receiver Under-sampling Performance: -15 dBm input at 200 MHz	142

Chapter 7

Figure 7-1	Prototype (Serial No. 001) Digital Transceiver with Dual SHARC DSP	147
Figure 7-2	Architecture of Wideband Digital Transceiver	149
Figure 7-3	SHARC ADSP-2106x Architecture (from [Analog, 135])	153
Figure 7-4	Dual SHARC Processor Module with 2Mx48 Shared Memory	155
Figure 7-5	Dual SHARC Processing Module Interconnections	155
Figure 7-6	Digital Transceiver Configuration Architecture (Simplified)	157
Figure 7-7	Photograph of Digital Transceiver RF Sub-Systems and Interfaces	159
Figure 7-8	Block Diagram of Digital Transceiver Frequency Standard Sub-System	160
Figure 7-9	Frequency Standard User Interface	161
Figure 7-10	Excerpt of Frequency Standard Sub-System Schematic	162
Figure 7-11	CPLD Design for Frequency Standard Showing Control Register	163
Figure 7-12	CPLD Implementation of Phase-Frequency Detector (PFD)	164
Figure 7-13	Phase-Frequency Detector (PFD) State Machine	165
Figure 7-14	One Channel of Digital Receiver RF Front-End (Excerpt from Schematic)	167
Figure 7-15	Dither Generator (Schematic Excerpt)	168
Figure 7-16	Block Diagram of 4-Channel Digital Receiver ASIC [Graychip, 124]	169
Figure 7-17	Digital Receiver Graphical User Interface	170
Figure 7-18	Block Diagram of 4-Channel Digital Transmitter ASIC [Graychip, 146]	172
Figure 7-19	Digital Transmitter DAC and RF Chain (Excerpt from Schematic)	173
Figure 7-20	Digital Transmitter Graphical User Interface	174
Figure 7-21	Triple PCI Front End Protection and Filtering Module	176
Figure 7-22	Digital Transceiver PCB 'Stack-up' (0.062"±0.008 Finished Thickness)	177
Figure 7-23	Class Diagram for Digital Transceiver (CDigitalTransceiver)	179
Figure 7-24	Diagnostics for Digital Transceiver Platform	180

Chapter 8

Figure 8-1	Implementation of I ₂ O Messaging using PLX9054	187
Figure 8-2	Organisation of I ₂ O Messaging Queues (from [PLX, 131])	189
Figure 8-3	Structure of Message Header	190
Figure 8-4	Structure of Message ID Field	190
Figure 8-5	UML Diagram of Asynchronous I ₂ O Messaging Implementation	195

Figure 8-6	Five Simultaneous Processes Running on Digital Transceiver.....	199
------------	---	-----

Chapter 9

Figure 9-1	Alternative Sounding Geometries	202
Figure 9-2	Vertical Ionogram Produced by a Digisonde Pulse Compression Sounder	204
Figure 9-3	Comparison between Pulse and Chirp Sounding [Barry, 165]	205
Figure 9-4	Configuration of WHISPER Receive System.....	208
Figure 9-5	UML Sequence Diagram Illustrating Sounder Receiver	210
Figure 9-6	Pulse Compression Waveform Performance Metrics	211
Figure 9-7	N_T Chip PN-Sequence Periodic Autocorrelation Function.....	213
Figure 9-8	Simulated Radio Filters (80 kHz Complex Baseband)	214
Figure 9-9	64 kchip/s PN-1023 Pulse Compression Waveform in 80 kHz Channel	215
Figure 9-10	Band-limited 64 kchip/s PN1023 Waveform CIR versus Doppler Offset.....	216
Figure 9-11	Band-limited 64 kchip/s PN1023 Waveform CIR versus Doppler Offset (close in).....	216
Figure 9-12	Performance of as a Function of Frequency Offset	217
Figure 9-13	Use of Windows in Calculating the Scattering Function	219
Figure 9-14	WHISPER Occupied Bandwidth (Waveform: tx1023-64r).....	220
Figure 9-15	WHISPER Back-to-back Test: Measured Ambiguity Response	220
Figure 9-16	WHISPER Back-to-Back Test: Complex Impulse Response Resolution	221
Figure 9-17	Back-to-Back Test: Doppler Resolution (512 CIRs, Hanning Window).....	221
Figure 9-18	Centre of Measured 'tx1023-64r' Waveform Power Spectrum (PRF=62.5 Hz)	222

Chapter 10

Figure 10-1	Measured Channel Scattering Function (3.9 MHz, 10 Apr 2001 07:38)	226
Figure 10-2	Measured Channel Scattering Function after Doppler Filtering (3.9 MHz 10 Apr 2001 07:38).....	226
Figure 10-3	Oblique Ionogram (10 Apr 2001 07:38)	228
Figure 10-4	Magnified View of Channel Scattering Function (3.9 MHz 10 Apr 2001 07:38)	228
Figure 10-5	Channel Power and Phase (Radians) plotted for 2.7 ms Mode versus Measurement Time (3.9 MHz, 10 April 2001 07:38).....	229
Figure 10-6	Channel Power and Phase (Radians) plotted for ~4.3 ms Mode versus Measurement Time (3.9 MHz, 10 April 2001 07:38).....	229
Figure 10-7	Channel Power and Phase (Radians) plotted for ~6 ms Mode versus Measurement Time (3.9 MHz, 10 April 2001 07:38).....	230
Figure 10-8	Ionogram (9 April 2001 20:31UT).....	231
Figure 10-9	Measured Scattering Function (6.7 MHz, 9 April 2001 20:30)	232
Figure 10-10	Measured Scattering Function after Doppler Filtering (6.7 MHz, 9 April 2001 20:30).....	232

Figure 10-11	Power and Phase Plot of 3.7 ms Mode Showing Rapid Movement of Layer (6.7 MHz, 9 April 2001 20:30).....	233
Figure 10-12	Oblique Ionogram (10 April 2001 08:10UT).....	234
Figure 10-13	Measured Scattering Function (5.7 MHz, 10 th April 2001 08:10UT).....	235
Figure 10-14	Measured Scattering Function After Doppler Filtering (5.7 MHz, 10 th April 2001 08:10UT)	235
Figure 10-11	Power and Phase Plot of ~3 ms Modes (5.7 MHz, 10 th April 2001 08:10UT).....	236
Figure 10-11	Power and Phase Plot of ~5.4 ms Spread Mode (5.7 MHz, 10 th April 2001 08:10UT).....	236

Chapter 11

Figure 11-1	Frequency Agile Simulator Architecture	241
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List of Abbreviations

ACF	Auto-correlation function
ADC	Analogue-to-digital converter
AGC	Automatic gain control
ALC	Automatic level control
ALU	Arithmetic logic unit
API	Application programming interface
ARP	Applied Research Programme
ARQ	Automatic repeat request
ASIC	Application specific integrated circuit
ATU	Antenna Tuning Unit
BDR	Blocking dynamic range
BER	Bit error rate
BIT	Built-in test
BLOS	Beyond line-of-sight
bps	Bits-per-second
BPSK	Binary PSK
CAST	Configurable radio with advanced software technology (EU research programme)
CCF	Cross-correlation function
CDA	Circularly disposed antenna array
CFIR	Compensating FIR (filter)
CIC	Cascaded integrator-comb
CIR	Complex impulse response
CRC	Communications research centre (Ottawa, Canada)
CRP	Corporate research programme
CVSD	Continuously variable slope delta-modulation
CW	Continuous wave

DAC	Digital-to-analogue converter
DAMSON	Doppler and multipath sounding network (HF sounder)
dBFS	Decibels below full-scale
DCE	Data communications equipment
DDC	Digital down-converter
DERA	Defence Evaluation and Research Agency (UK MOD)
DFT	Discrete Fourier transform
DLP	Data-link protocols
DNL	Dynamic non-linearities
DMA	Direct memory access
DOD	US Department of Defence
DPP	Delay power profile
DRM	Digital radio Mondiale
DSP	Digital signal processing (or processor)
DTE	Data terminal equipment
DUC	Digital up-converter
E2PROM	Electrically erasable programmable memory
EEPROM	Electrically erasable programmable memory
FEC	Forward error correction
FFT	Fast Fourier transform
FIR	Finite impulse response (filter)
FM	Frequency modulation
FMCW	Frequency modulated continuous wave
FPGA	Field programmable gate array
FSK	Frequency shift keying
GPS	Global positioning system (US DOD satellite navigation system)
GUI	Graphical user interface
HC	Hyper-code

HDR	High data rate
HF	High frequency
I₂O	Intelligent Input/Output
IDR	Instantaneous dynamic range
IF	Intermediate frequency (radio systems)
IIR	Infinite impulse response
IMD	Intermodulation distortion
INL	Integral non-linearity
I/O	Input/output
IRQ	Interrupt request
ISB	Independent side-band
ITS	Institute of telecommunications sciences (US Federal agency)
ITU	International telecommunications union
JTAG	Joint test action group
JTRS	Joint tactical radio system (US military software radio programme)
kbps	Kilo-bits per second
LED	Light emitting diode
LO	Local oscillator
LPF	Low pass filter
MCI	Module control interface
MFA	Message frame address
MFLOPS	Million floating point operations per second
MFSK	Multi-tone FSK
MIMO	Multiple-input, multiple-output
MMIC	Miniature microwave integrated circuit
MSPS	Mega-samples per second
NATO	North Atlantic Treaty Organisation
NF	Noise figure

NVIS	Near vertical incidence sky-wave
OFDM	Orthogonal frequency division multiplex
OMG	Object Management Group
OS	Operating system
PA	Power amplifier
PC	Personal Computer
PCB	Printed circuit board
PCI	Peripheral component interconnect
PFD	Phase-frequency detector
PLL	Phase locked loop
PN	Pseudo noise (sequences)
PFD	Phase-frequency detector
PFIR	Programmable FIR (filter)
PPF	Deterministic phase function
PPM	Parts-per-million
PRF	Pulse repetition frequency
PRI	Pulse repetition interval
PSK	Phase shift keying
PU	Participating Unit
QAM	Quadrature amplitude modulation
RF	Radio frequency
RAM	Random access memory
RMS	Root mean squared
RRS	Recursive running sum
RTOS	Real-time operating system
SCA	Software communications architecture (for JTRS)
SDR	Software defined radio
SFDR	Spurious free dynamic range

SGL	Scatter gather list
SHARC	Super Harvard architecture (DSP processor)
SIG	Special interest group
SINAD	Signal plus noise and distortion to noise and distortion ratio
SMF	Stochastic modulating function
SMT	Surface mount technology
SNR	Signal-to-noise ratio
SRAM	Static random access memory
SSB	Single side-band
SWF	Shortwave fadeout
TCXO	Temperature compensated crystal oscillator
TDMA	Time division multiple access
TOF	Time of flight
UML	Unified modelling language
USB	Upper side-band
VCXO	Voltage controlled crystal oscillator
WHISPER	Wideband HF Ionospheric Sounder for Propagation Environment Research

Chapter 1.

Introduction

This thesis describes novel work in the areas of digital radio and its application to the high frequency (HF, 2-30 MHz) band. The propagation environment at these frequencies has a significant impact on the performance of radio systems (especially data communications). However, the ability to communicate information over very long ranges using ionospheric propagation paths without any intermediate infrastructure makes the use of HF attractive for many applications. In order to increase the utility of HF communications there is a strong desire to increase HF data rates. Currently data rates of up to ~2400 bps can be reliably achieved in standard 3 kHz HF channel allocations. Whilst further increases in data rate within the confines of these narrowband frequency allocations is likely, the use of larger bandwidths (contiguous or otherwise) appears to offer potential for much greater throughputs. This requires a greater understanding of the characteristics of wideband channels and also requires transmitting and receiving equipment capable of wideband/multi-channel operation.

This thesis details research undertaken over a three year period between April 1998 and April 2001 funded by the author's employer, the Defence Evaluation and Research Agency (DERA), part of the UK Ministry of Defence. The research was undertaken as a working collaboration with scientists and engineers at the Communications Research Centre (CRC) in Ottawa, Ontario, Canada under a UK-Canadian government agreement on collaboration on defence science and technology [MOD, 1].

The original aim was to investigate the characteristics of wideband HF ionospheric propagation channels in order to exploit them for high data rate (HDR) communications. Very early on an opportunity was identified to work with CRC to implement and demonstrate a HDR modem providing 16 kbps in a 6 kHz bandwidth. The success of this work contributed to the standardisation of extended bandwidth HDR waveforms in a widely used military modem standard; MIL-STD-188-110B [DOD, 2]. Work started on the development of a new channel sounder to provide data to be used in the investigation of the wideband channel. This involved the design of wideband

transmission and reception equipment. What started out as a means to an end became a key focus of the research as it became apparent that it would be possible to build a high performance direct-sampling digital HF radio. A new wideband digital HF transceiver (HF software radio) with such an architecture has been implemented and is presented in this thesis. This was used as a platform on which a new wideband channel sounder, known as WHISPER, has been developed. The development of WHISPER and its use to investigate the wideband (~ 80 kHz) HF channel is also documented.

1.1 Structure of Thesis

This chapter provides an introduction and some background to the research presented in this thesis.

Chapter 2 introduces the HF propagation environment and its impact on radio systems (particularly communications). The effects of noise and interference are also summarised. HF channel simulation techniques that may be used to develop and test communications systems are discussed. Characteristics of the wideband HF channel and applicable channel models are considered, identifying a number of areas in which work is required to provide a better understanding of the processes at work.

In chapter 3 the key technologies used to implement data communications waveforms are reviewed including forward error correction, interleaving, modulation and channel equalisation. Practical application to HF is illustrated by examining the design of a modern narrowband serial tone waveform. Finally techniques applicable to wideband and high throughput communications are introduced.

Chapter 4 describes a novel high data rate 16 kbps prototype modem operating in an extended bandwidth of 6 kHz. Results from HF simulator measurements and on-air testing of the modem are presented. The performance limitations of such high data rate modems are discussed leading to an identification of the range of applications for which they can be expected to be used reliably: notably on surface wave paths and on benign Skywave paths. Finally a number of alternative extended bandwidth waveforms are proposed and their performance compared with that of recently developed high throughput narrowband (3 kHz) waveforms.

Chapter 5 focuses on the architectures and implementation of wideband and multi-channel digital HF radios. The requirements that the HF environment places on high

performance receiver design are considered. Results obtained from the characterisation of a high quality conventional narrowband HF receiver are given to establish a basis for comparison. A very high performance, direct sampling wideband digital HF receiver is proposed. Such a receiver would (conceptually) allow an arbitrary number of channels to be simultaneously received using a single RF front-end and digitiser. The design and performance of a practical receiver of this type is considered in detail.

In chapter 6 the design and implementation of a new prototype direct-sampling digital HF receiver is presented along with measured performance results. These are discussed and suggestions for improvements to the prototype design are advanced.

Chapter 7 describes the implementation of a wideband, multi-channel digital HF transceiver, using the direct sampling architecture. The design of the transceiver, which has been specifically conceived as a highly re-configurable software defined radio system, is explained. Descriptions of the key sub-systems including the diversity receiver, transmitter, the digital signal processing (DSP) sub-system and the control software are given.

Chapter 8 deals with a particular challenge of complex systems such as software radios - the effective deployment of application software across a number of heterogeneous processors. This chapter proposes a new asynchronous, event-based, processing architecture which employs lightweight (low overhead) active messaging to allow processing tasks to be effectively distributed across multiple processors and across buses. The architecture and its effective implementation on the digital transceiver hardware are described. Suggestions for further developments and improvement have been made.

Chapter 9 provides a brief introduction to channel sounding techniques before introducing, WHISPER, a new oblique wideband HF ionospheric sounder. The design of this low power pulse-compression sounder, which is based on software radio techniques, is introduced and its implementation as an application on the wideband digital HF transceiver described. The chapter then considers the design of sounding waveforms suitable for an investigation of the wideband (~ 80 kHz) channel characteristics of mid-latitude Skywave propagation channels. Finally, the results of back-to-back measurements performed at RF are analysed to confirm the performance of the sounder.

Chapter 10 describes a short campaign of wideband measurements that have been made over a 170 km path in the UK during Spring 2001 using the WHISPER sounder. The results of these measurements have been analysed and confirm the ability of the sounding instrument to measure the channel scattering function and the amplitude and phase within individual modes. A number of possible directions for a more detailed analysis of the data are then suggested.

Chapter 11 identifies a number of areas in which digital HF radio may be applied to advantage.

Finally, chapter 12, draws some conclusions from the work presented in this thesis and identifies recommended areas for further work.

1.2 Original Work

This thesis contains several elements of original work in the areas of high throughput HF communications, high performance HF digital radio architectures and their implementation, implementation of a wideband HF channel sounder using the digital radio and in the conclusions drawn from the analysis of wideband channel measurements obtained during on-air trials. Specific contributions to development of the field are identified below:

1.2.1 High Throughput HF Data Communications Employing Extended Bandwidth (6 kHz) Channels

New waveforms have been proposed for the transmission of higher data rates in an extended HF channel bandwidth (6 kHz). The results of laboratory tests and analysis of data collected during on-air trials of these 16 kbps waveforms are presented. Analysis undertaken indicates that these new waveforms are capable of reliable operation over surface wave and benign HF Skywave channels providing a sufficient received signal-to-noise ratio can be maintained. The work presented has contributed to the international standardisation of higher throughput waveforms (specifically US MIL-STD-188-110B). It has also demonstrated the value in exploiting wider bandwidths for HF radio applications.

1.2.2 Architectures for Wideband Digital Receivers and Transmitter Exciters

Architectures for the implementation of wideband and multi-channel digital HF radios (software radios) have been investigated. A new direct-sampling architecture for a digital HF receiver has been proposed. In such a receiver the entire HF band is digitised and then all subsequent processing is undertaken digitally. Conceptually this would allow an arbitrary number of channels to be simultaneously received using a single RF front-end and digitiser. The requirements for high performance receivers due to the HF propagation, noise and interference environment have been established. A high performance conventional narrowband super-heterodyne receiver has been characterised to establish a basis for comparison. A design for a practical direct sampling receiver is proposed and analysis presented which indicates that is now possible, for the first time, to construct a high performance receiver of this architecture. The work shows that, with careful design, such a receiver should attain performance comparable with (or even exceeding) that of the majority of conventional super-heterodyne single channel receivers. A prototype wideband direct sampling receiver (part of a digital HF transceiver platform) has been implemented and its performance characterised confirming the potential for such a design.

1.2.3 Implementation of a Wideband Digital HF Transceiver

A new high performance wideband, multi-channel HF transceiver (HF software radio) using the direct sampling architecture has been designed and implemented. It has been implemented as a highly re-configurable software defined radio platform intended to support diverse applications including use as a radio/modem, channel sounders and an RF channel simulator. It incorporates a two channel diversity front end feeding four independent receiver channels and a four channel transmitter exciter with a single RF output. The design is very compact, being implemented on a single peripheral component interconnect (PCI) card which can be plugged into a host personal computer (PC).

1.2.4 Development and Implementation of a High Performance Asynchronous Event Based Processing Architecture

A lightweight event based processing architecture for use across an array of heterogeneous processors has been conceived, developed and implemented on the wideband digital HF transceiver platform. It uses an active messaging concept in which messages arriving in a queue cause pre-defined processing activities to take place.

1.2.5 Design and Implementation of a Wideband HF Channel Sounder using the Digital HF Transceiver

A new, high resolution wideband oblique HF channel sounder, which has become known as WHISPER, has been developed and implemented as an application on the wideband digital HF transceiver platform. The system is very flexible with sounding waveforms and their characteristics (sounding waveform, bandwidth, repetition interval etc) being determined by a configuration file. The sounder makes use of an external GPS receiver to provide accurate synchronisation of transmitter and receiver in order to allow time-of-flight measurements to be made. Pulse-compression sounding waveforms with carefully controlled time sidelobes have been designed to allow high fidelity measurement of the time varying characteristics of wideband (~80 kHz) HF channels. The high performance of the complete sounding system has been verified through back-to-back RF tests in the laboratory.

1.2.6 Analysis of On-Air Wideband HF Channel Characterisation Measurements

The WHISPER wideband sounder has been used to make high resolution measurements of the time varying complex impulse response on a 170 km path in the southern UK. The results of these measurements have been analysed and confirm the ability of the sounding instrument to measure the channel scattering function and the amplitude and phase within individual modes. A number of research directions for a more detailed analysis, pertinent to the design of wideband HF modems, have been proposed.

Chapter 2.

The HF Propagation Environment and Its Impact on Communications

This chapter introduces the HF propagation environment and its impact on radio systems particularly communications. For a much more comprehensive and detailed treatment of the subject the reader is referred to the texts that have been extensively used in this chapter's preparation; [Davies, 3], [Goodman, 4] and [Maslin, 5].

HF radio propagation (2 to 30 MHz) provides both line-of-sight (LOS) and beyond line-of-sight (BLOS) coverage and can occur by a variety of mechanisms. Direct wave propagation provides true LOS communications whereas the surface wave mechanism supports shorter range BLOS communications and is especially effective over sea paths providing typical ranges of 200 km or more. For greater ranges sky wave propagation must be exploited.

2.1 Surface Wave Propagation

Surface wave (or ground wave) propagation is supported over short distances on land (perhaps up to ~30 km depending on terrain) and at much greater distances over highly conducting sea water [Maslin, 5]. This mode of propagation requires the use of vertically polarised antennas and is commonly used for extended line-of-sight communications. Curves which show field strength versus range for ground wave propagation are given in ITU-R P.368-7 [ITU, 6].

2.2 Sky Wave Propagation

2.2.1 Structure of the Ionosphere

Sky wave communications, which involve transmitting signals beyond the radio horizon, rely upon refraction of the signals by the earth's ionosphere [Davies, 3]. The ionosphere is a highly inhomogeneous ionised region of the earth's atmosphere lying in

the altitude range 85 - 1,000 km. Its presence is primarily due to solar radiation including ultra violet (UV), x-rays and energetic charged particles all of which cause ionisation of neutral gases. Recombination (loss processes) occur due to the collision of electrons and positive ions and the attachment of electrons to neutral gas atoms or molecules (the principal chemical reactions are given in [Davies, 3, p63]). Different ionisation and loss processes become predominant at different altitudes (related to density and temperature profiles as well as incident solar radiation) resulting in a layered structure (Figure 2-1). The principal regions of the ionosphere are designated *D*, *E* and *F*. Some of these regions are themselves layered or structured (e.g. *E*, *E_s*, *F1* and *F2*). The number of layers, their heights and their ionisation density vary with time and in space. Variations occur diurnally (Figure 2-1, Figure 2-2), seasonally, with the 11 year solar cycle and due to changes in geomagnetic activity. The high latitude ionosphere is particularly complicated and will often be significantly different to that observed at mid and lower latitudes.

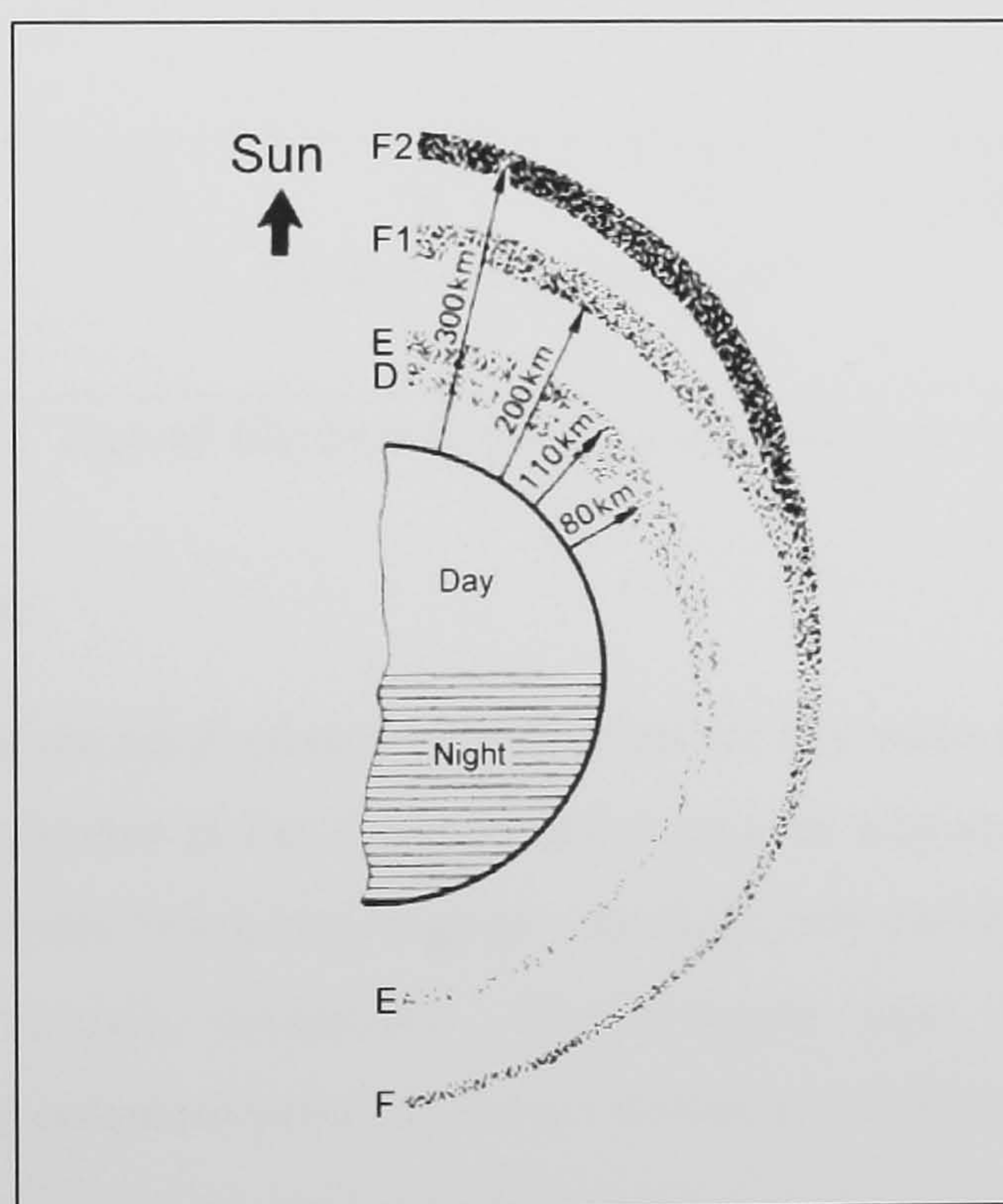


Figure 2-1 The Earth's Ionosphere and its Principal Regions [Maslin, 5]

2.2.2 D-Region

The *D*-region, principally responsible for signal absorption, extends from 70 - 90 km and is only weakly ionised. During the day solar ionisation leads to strong HF signal absorption. At mid and low latitudes within a couple of hours of sunset *D*-region

absorption becomes negligible contributing to the stronger signal strengths and increased noise experienced in the HF band at night. As the region is caused by solar radiation it is observed to be stronger during the summer than the winter.

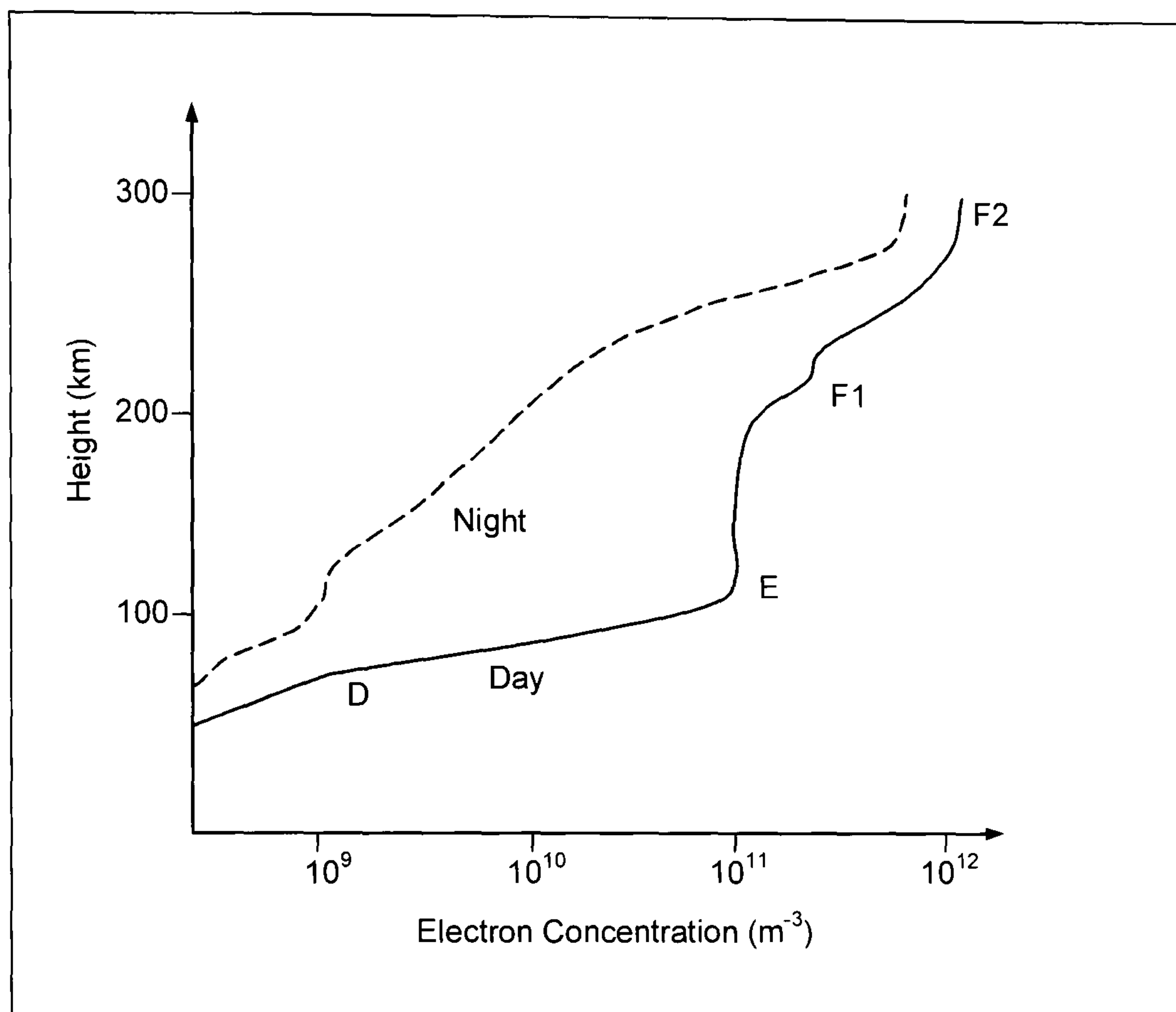


Figure 2-2 Typical Electron Concentration within the Ionosphere [Davies, 3]

2.2.3 E-Region

The *E* and *F* regions are predominantly responsible for sky wave reflections. The level of solar induced ionisation in the *E*-region peaks near an altitude of 110 km with the daytime region generally being very regular. At night only residual ionisation remains and the *E*-region virtually disappears. The *E*-region plays an important part in supporting sky wave communications at shorter distances (<2000 km).

Within the *E*-region there can exist spatially and temporally variable patches of enhanced ionisation, known as sporadic-*E* (E_s), which can scatter and reflect HF radio wave signals. Its presence is highly latitude dependent; at mid-latitudes it is more frequent during the day than at night and more frequent in the summer than the winter. At high latitudes, it is a regular night time phenomena. E_s can support good sky wave propagation but, by its nature, is hard to predict and requires the use of systems employing real-time channel evaluation (RTCE) to exploit this effectively. The

presence of strong E_s can result in an increase in the critical frequency, f_o , the highest frequency at which a vertically incident ray is reflected, and can result in very long range propagation at very high frequencies (sometimes well in excess of 30 MHz).

2.2.4 *F-Region*

The *F*-region consists of two layers known as *F1*, which lies between 150 - 200 km. and *F2*, which lies above from 250 - 400 km. The *F1* region only exists during the daytime. Whilst it can sometimes act a reflecting layer, obliquely incident signals that penetrate into the *E*-region will often pass through *F1*, suffering some absorption, before being reflected by the *F2* layer. At night, the absence of *F1* region and the reduction in *D*-region absorption cause signal strengths and noise levels (including interference) to be generally higher than during the day.

The highest ionospheric layer, *F2*, generally has the greatest electron density. The relatively low molecular densities present in this region mean that collision rates are low and solar energy can be stored for substantial periods of time (hours), thus its properties are not simply related to the solar zenith angle (incident solar radiation) in the same way as the *D* and *E* regions. The *F2*-region height and ionisation vary diurnally, seasonally and with the sunspot cycle. Further, *F2* variation is complex being strongly influenced by dynamic effects including winds and diffusion [Maslin, 5]. The *F2* region is principally involved in reflecting signals which support long range HF sky wave propagation.

It is often the case that the reflection of signals by the *F*-region results in signal time dispersion; a phenomenon known as *spread-F*. This is caused by the scattering of the incident signal from small (1-2 km) to large (hundreds of kilometres wide) irregularities (regions of higher electron density), in the inhomogeneous ionosphere. At the geomagnetic equator *spread-F* is observed between local sunset and the middle of the night. At high latitudes it is a constant feature particularly during the winter when there is no diurnal variation [Davies, 3, pp.148-151]. Whereas the critical frequencies of the *E* and *F1* layers (f_oE and f_oF1) vary through the year in phase with the solar zenith angle, the critical frequency of the *F2*-layer (f_oF2) *increases* in winter [Davies, 3, p.135]. This is known as the winter anomaly and only occurs during winter days due to recombination being slower. The high latitude *F*-region is significantly different to that observed at lower latitudes.

2.2.5 The Changing Ionosphere

The ionosphere is constantly changing. Some of these changes are well ordered and highly predictable (e.g. diurnal changes) whilst others are the result of transient events (e.g. solar disturbances). These variations are principally related to:

- **Diurnal** – Changes in the solar zenith angle and hence the amount of solar radiation incident on a particular region of the ionosphere due to the earth's rotation.
- **Latitude** – In addition to the relationship of latitude with the solar zenith angle the coupling of the solar wind with the earth's magnetic environment results in the significant differences observed between the low, mid and high-latitude ionospheres.
- **Seasonal** – Changes related to the solar zenith angle, recombination rates and the effective change in latitude of a particular geographic region.
- **Solar Cycle & Ionospheric Disturbances** – The sun has an 11 year cycle of activity (see Figure 2-3, data from [SPIDR, 7]) which impacts the radiation and the number of energetic particles coupled into the earth's ionosphere. Significant solar events particularly solar flares have major impact on the ionosphere and hence on signals propagating through it.

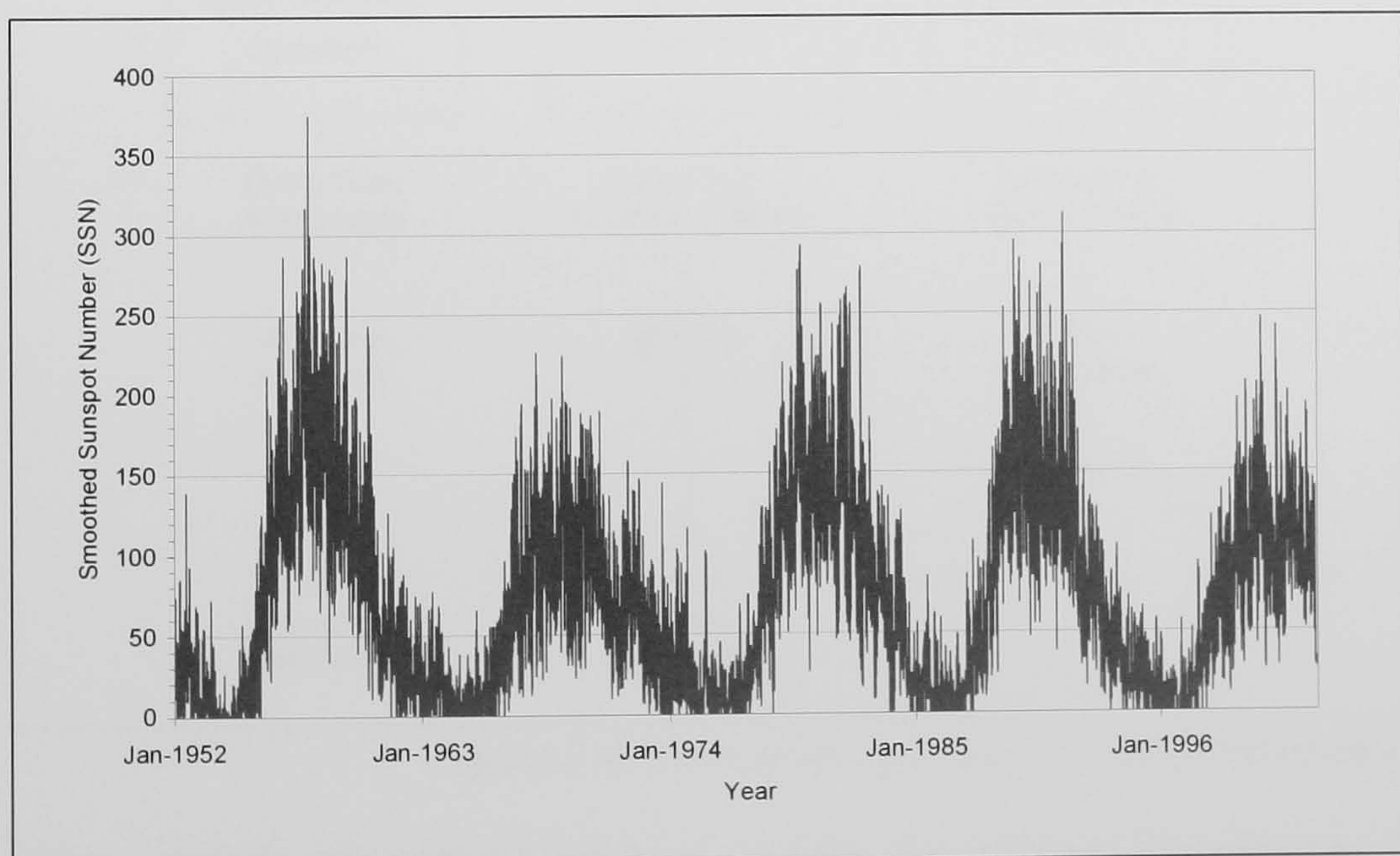


Figure 2-3 Daily Smoothed Sunspot Numbers Illustrating 11 Year Solar Cycle

2.2.6 Ionospheric Disturbances

Whilst even the undisturbed ionosphere is complex and highly inhomogeneous there are mechanisms that can cause major transient disruptions, known collectively as ionospheric disturbances. These can significantly impact radio systems that rely on ionospheric propagation. The disturbances are generally a result of events taking place on the sun (e.g. solar flares) and involve very large quantities of energy. The principal causes of ionospheric disturbances [Davies, 3, pp.312-366] is one or a combination of solar flares (bursts of high intensity optical, x-ray and UV radiation lasting minutes), Coronal mass ejections, Coronal holes (areas of low density on the sun’s surface that can last for many days) and disappearing filaments (the re-absorption of loops of plasma on the sun’s surface). The principal mechanisms and their effects are summarised in Figure 2-4 .

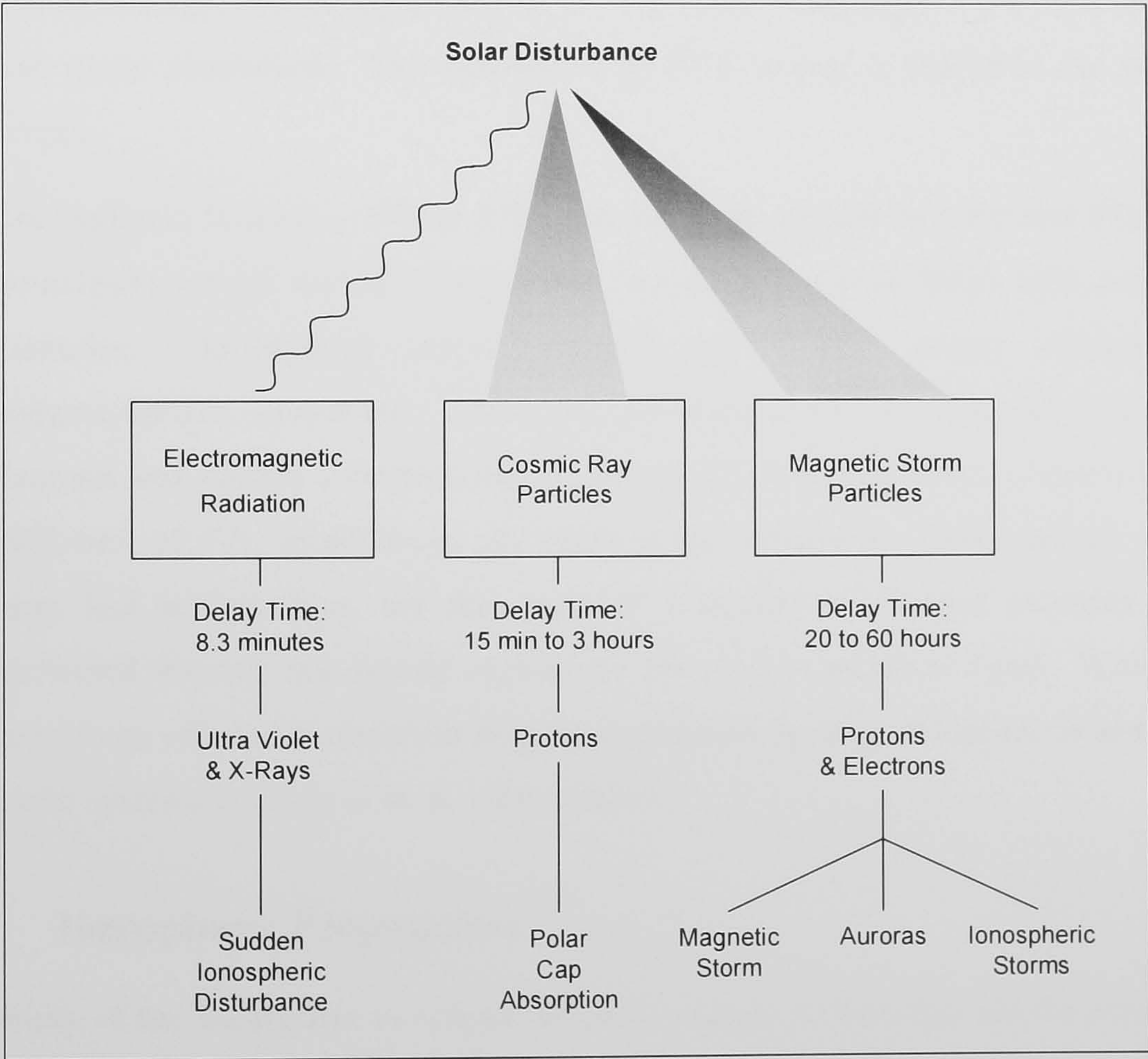


Figure 2-4 Terrestrial Effects of a Solar Disturbance [5, 3]

The effects include phenomena such as sudden ionospheric disturbances (SIDs), ionospheric storms and polar-cap absorption (PCA) events:

- **Sudden Ionospheric Disturbances (SIDs)** – Shortwave fadeouts (SWFs) are caused by solar flare x-ray energy that causes an increase in D-region absorption. They typically exhibit a rapid onset (minutes) and a slower decay (generally within one or two hours). Sudden frequency deviations (SFDs) cause a positive and then negative Doppler shift to be applied to propagating signals as the effective layer height reduces (due to increased ionisation) and then to return to its original position. If SFDs occur with little change in absorption then the principal cause is UV radiation.
- **Polar Cap Absorption (PCA) Events** – The polar cap is generally considered to be the region at a latitude of $>70^\circ$. During large flares highly energetic protons are released. On entering the ionosphere, they cause ionisation by colliding with gas molecules. The resulting PCA can last for as long as several days exhibiting strong absorption through the day time. The effect starts high in the polar cap and can move southward. The occurrence of PCA events is linked to the sunspot cycle.
- **Ionospheric Storms** – Whilst SIDs last for short periods of time and PCAs are principally a high latitude phenomena, ionospheric storms affect mid- and low-latitudes. Ionospheric storms include geomagnetic storms, auroral and magnetospheric storms etc. These may be accompanied by *D*-region absorption (auroral and sudden commencement), auroral E_s , *F*-region storms (expansion and diffusion of F_2), scintillation, and radio noise emissions. These storms, which may last several days, are the result of a stream of charged particles being deflected towards the auroral regions by the earth's magnetic field. Whilst the maximum effects are observed at solar maximums the biggest impact on terrestrial radio systems is likely to be at solar minima.

2.2.7 Ionospheric Propagation

The ability of the ionosphere to refract HF radio signals so that they are directed back towards the earth (rather than passing into space), is determined by the level of ionisation present and the frequency and angle of incidence of the signals. Consequently, frequency selection for BLOS communications is dependent upon many factors including the link geography and time-of-day.

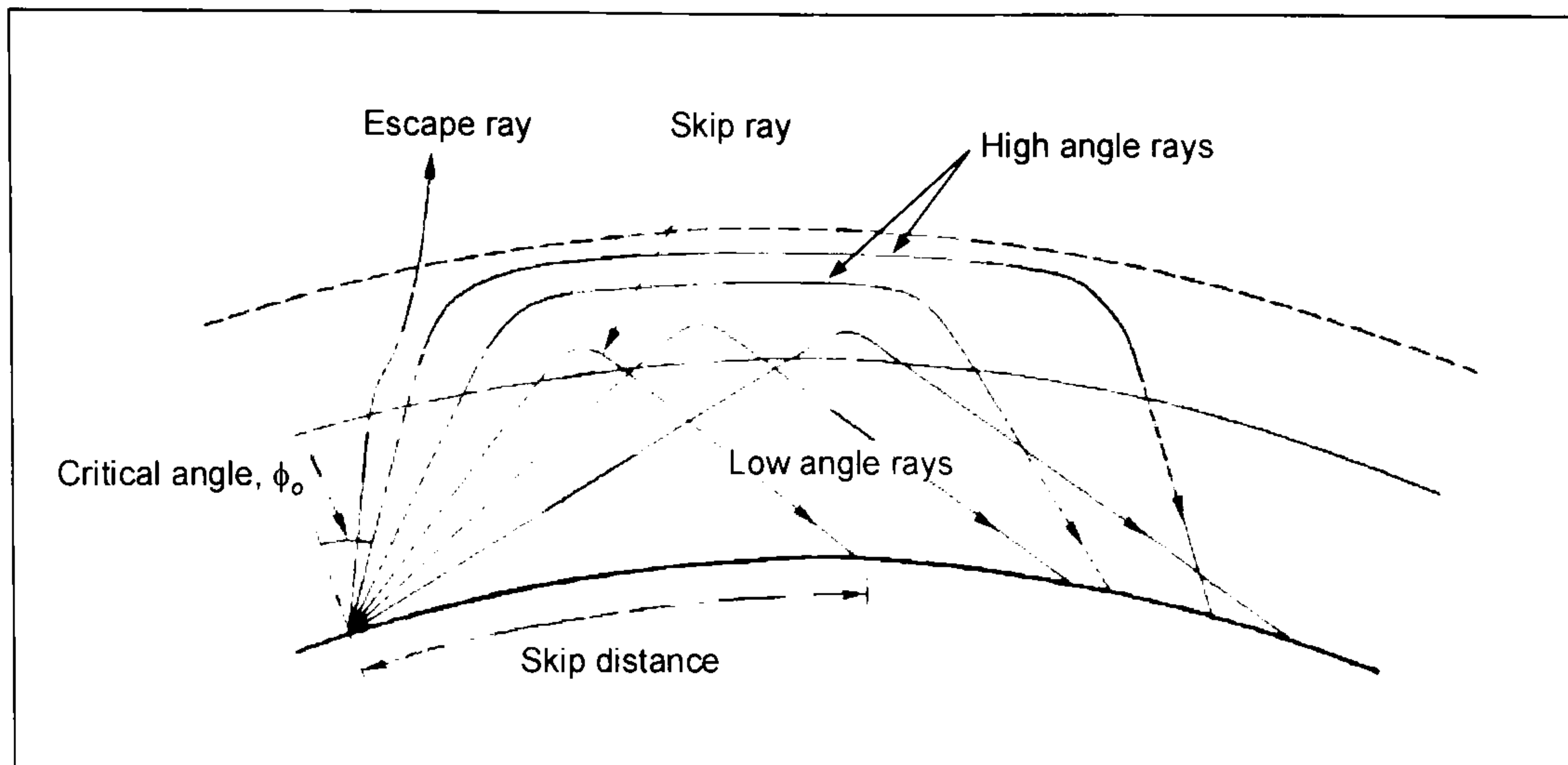


Figure 2-5 Ray Paths as a Function of Elevation at a Single Frequency [Maslin, 5]

Figure 2-5 shows how the trajectory of a single frequency signal varies as a function of elevation. Low elevation signals will be reflected by the ionosphere and return to earth at a considerable distance from the launching antenna. The critical angle for sufficient refraction to occur to produce reflections from a layer is proportional to its electron density. As the elevation of the transmitted radio wave increases it is reflected to earth at shorter and shorter ranges. The region where no signals can be received, between the transmitter and where the sky wave returns fall, is known as the skip zone. At still higher elevations the ionosphere does not refract the signal sufficiently to reflect it immediately and it penetrates further into the ionosphere and is dispersed over much greater distances (high angle ray). When the launch elevation exceeds the critical angle for the layer altogether the ray will pass through it and is termed an escape ray.

When an electromagnetic wave interacts with electrons in the ionosphere the earth's magnetic field causes the signal to split into two components; the ordinary (*O*) and extraordinary (*X*) waves (together '*O-X*'). Further interactions result in the resulting *O-X* wave having a particular polarisation ellipse. This is discussed in much greater detail in [Davies, 3, pp.226-232] and the reader is referred there for a more complete description.

The maximum usable frequency (MUF), for communications at a particular distance and for a specific layer is approximated by:

$$MUF = f_o \sec \phi \quad (2-1)$$

where f_o is the critical frequency of the layer and, ϕ is the angle of incidence on the reflecting layer. Over longer distances the curvature of the earth and the vertical

ionisation profile must be taken into consideration so a correction factor, k , whose value falls between 1.0 and 1.2, is introduced [Davies, 3], [Van Valkenburg, 8]:

$$MUF = kf_o \sec \phi \tag{2-2}$$

Figure 2-6 depicts a VOACAP [Hand, 9] monthly median propagation prediction for a sky wave circuit from Frankfurt, Germany to London, UK. The figure illustrates how the MUF and circuit propagation loss typically vary with diurnal, seasonal and sunspot activity.

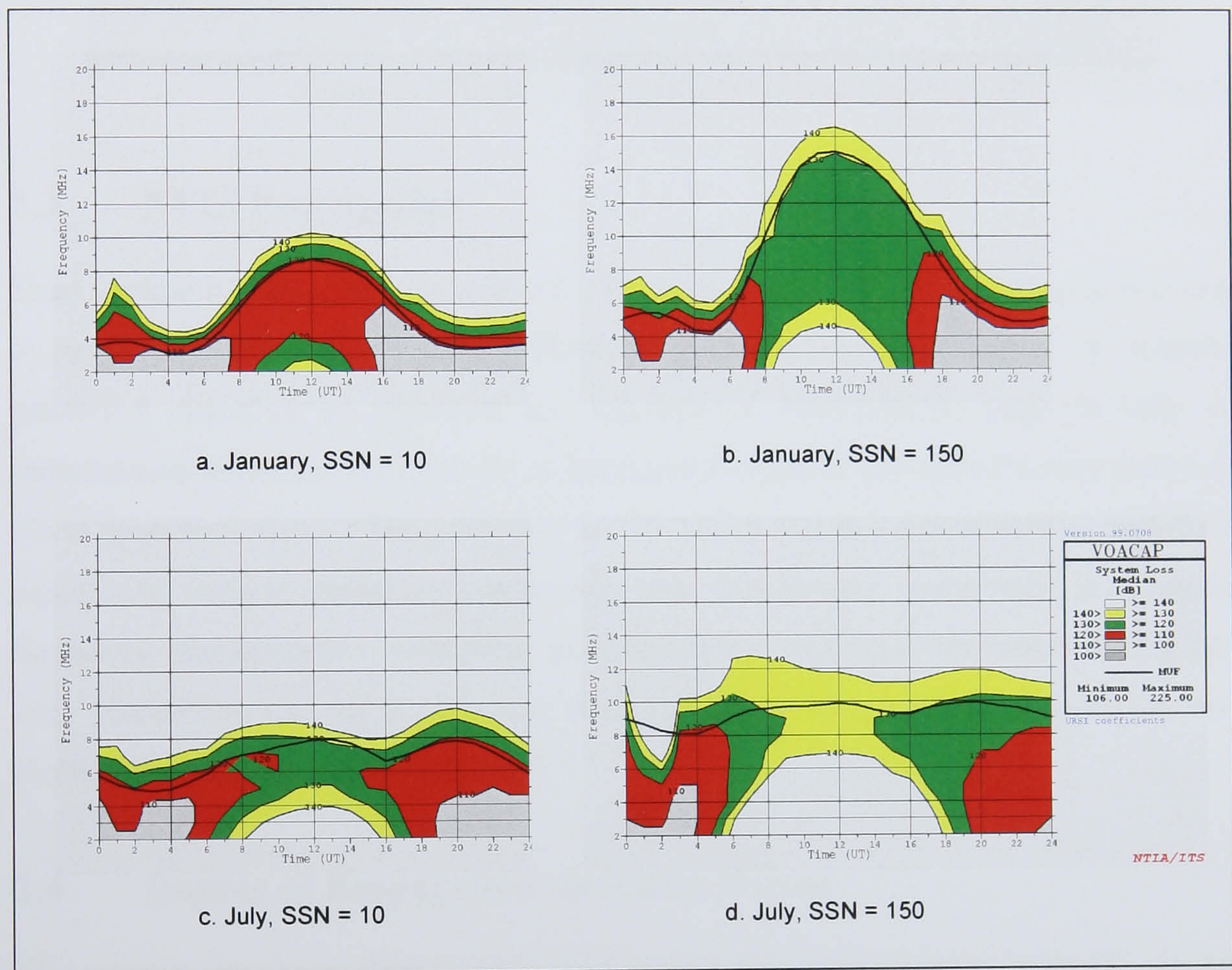


Figure 2-6 Predicted Propagation Loss and MUF for Frankfurt-to-London Sky wave Circuit

Over long distance communications paths (with an East-West component) differences in the time-of-day are encountered, resulting in varying degrees of ionisation and structure in the ionosphere. Daylight portions of the path favour higher propagation frequencies, whereas night time portions favour lower frequencies. This can make the selection of suitable communications frequencies for communications across the so-called day/night terminator (see Figure 2-7) a difficult task.



Figure 2-7 Position of Day-Night Terminator at 1200Z in December

2.3 NVIS Propagation

Near vertical incidence sky wave (NVIS) supports terrain independent communications to ranges of ~ 150 km and beyond [Maslin, 5]. Where ground stations or airborne platforms operating at low-level are required to communicate deep in hilly or mountainous areas, the NVIS mode of operation frequently provides the only means of direct communication. The effective use of NVIS requires antennas that provide a significant vertical radiation component (i.e. horizontally polarised) and careful frequency management. Achieving an acceptable signal level (and overcoming day time absorption) can be a particular challenge when low powered transmitters and electrically small antennas are utilised.

2.4 Impact of Propagation on Radio Waves

This section introduces the principle mechanisms that perturb propagating HF signals and describes the impact that they have. Whilst these effects are often considered to be purely detrimental the following discussion also seeks to identify how the resulting changes in signals can be used to advantage in a suitable system by exploiting the resulting diversity in the received signals.

The ionosphere is a dispersive medium leading to spreading of the pulses travelling through it. Reflections from multiple layers combined with multi-hop propagation results in multipath returns. Time dispersion and multipath may be of the order of several milliseconds (occasionally ≥ 10 ms), and Doppler spread (fading) of many Hertz (occasionally ≥ 40 Hz) may be observed. The severity of these effects is particularly

significant at high latitudes (above 65° , i.e. in auroral and polar cap regions, [Davies, 3], [Angling, 10]) where the ionosphere is severely affected by energetic particles arriving indirectly from the sun. Similar disturbances may also be observed at low latitudes (i.e. within 15° of the equator).

2.4.1 Attenuation

The principal causes of radio wave signal attenuation are:

- **Free space Propagation Loss** – essentially the loss due to the spatial spread of energy.
- **Environmental Absorption and Ground Reflection Losses** – Absorption in the environment due to low conductivity media (e.g. terrain losses) and surface scattering.
- **Reflection Losses** – Imperfect reflection of signals or scattering in the ionosphere.
- **Ionospheric absorption** – Absorption in the ionosphere.
- **Polarisation Loss** – An inability to pick-up all the available power at a receive antenna because it does not match the polarisation of the incoming radio wave.

2.4.2 Multipath and Signal Dispersion

A number of mechanisms cause multiple, time delayed, versions of the transmitted signal to be received. These are commonly termed multipath where distinctly separate returns (modes) can be identified. The principal forms of multipath and time dispersion are:

- **Groundwave/Skywave Interaction** - Under conditions where both a ground wave and sky wave component can propagate (Figure 2-8a) there will be a significant differential in the relative time of flight (>2.5 ms is possible on short links during the day-time).
- **Reflections from Different Layers** – Even for narrow transmitter antenna vertical beam widths, signals are launched with a range of elevation angles. Radio waves will only be reflected if they arrive at an angle exceeding the critical angle for a layer to produce reflections and this is proportional to its electron density.

Multipath is generated when signals arrive at the receiver having been reflected by different layers with different electron densities (Figure 2-8b).

- **Differing Number of Hops** – Signals arrive having undergone a different number of ionospheric and ground reflections (i.e. hops), see Figure 2-8c.
- **High angle/Low angle** – As previously described, the angle at which radio waves impinge on the ionosphere can result in them taking substantially different trajectories to the receive location (Figure 2-8d).
- **Mode Dispersion** – Finite antenna beam widths and the thickness of the ionospheric layers and their varying refractive index, causes a continuum of returns at the receiver; mode dispersion (Figure 2-8e). Typical time dispersion within a mode may be $\sim 200 \mu\text{s}$ [Maslin, 5] although narrowband HF systems are unable to resolve such effects. A more dramatic example of this phenomenon is in the presence of *spread-F*; when the *F*-region is inhomogeneous contains many irregularities. Under such conditions, and particularly at high latitudes, delay spreads of several milliseconds are possible.
- **Magneto-ionic Splitting** – When a transmitted signal is incident upon the ionosphere it leads to the excitation of differently polarised waves termed the ordinary and the extraordinary (together abbreviated *O-X*), see Figure 2-8f. The *O-X* waves then propagate independently and are subject to differing amounts of delay, fading and attenuation. The relative delay is related to frequency and is typically measured in micro-seconds. Narrowband systems are unable to resolve this small time delay and thus the presence of *O-X* waves may only be detected by their interaction which leads to single-mode fading (flat fading). With wider reception bandwidths ($> \sim 50 \text{ kHz}$) it becomes possible to directly observe the two returns and thus they are of importance to wideband system design.

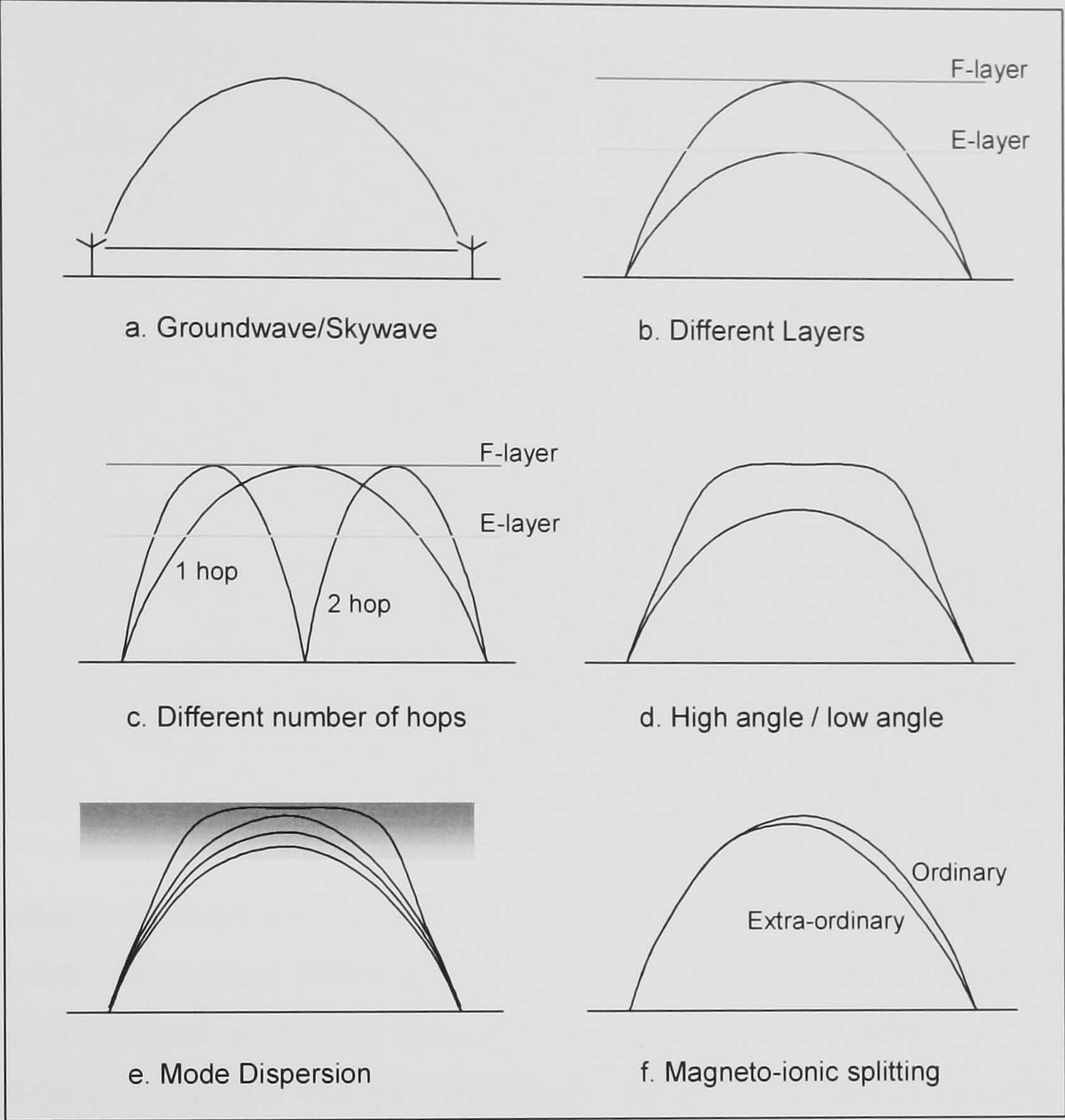


Figure 2-8 Summary of the Causes of Multipath and Dispersion [after Maslin, 5]

It should be noted that it is quite possible for a number of these mechanisms to be at work simultaneously causing a complex series of multipath modes, some with appreciable dispersion, to be received. This is illustrated in Figure 2-9 which reproduces an oblique ionogram collected using an IRIS FM CW sounder [Arthur, 11].

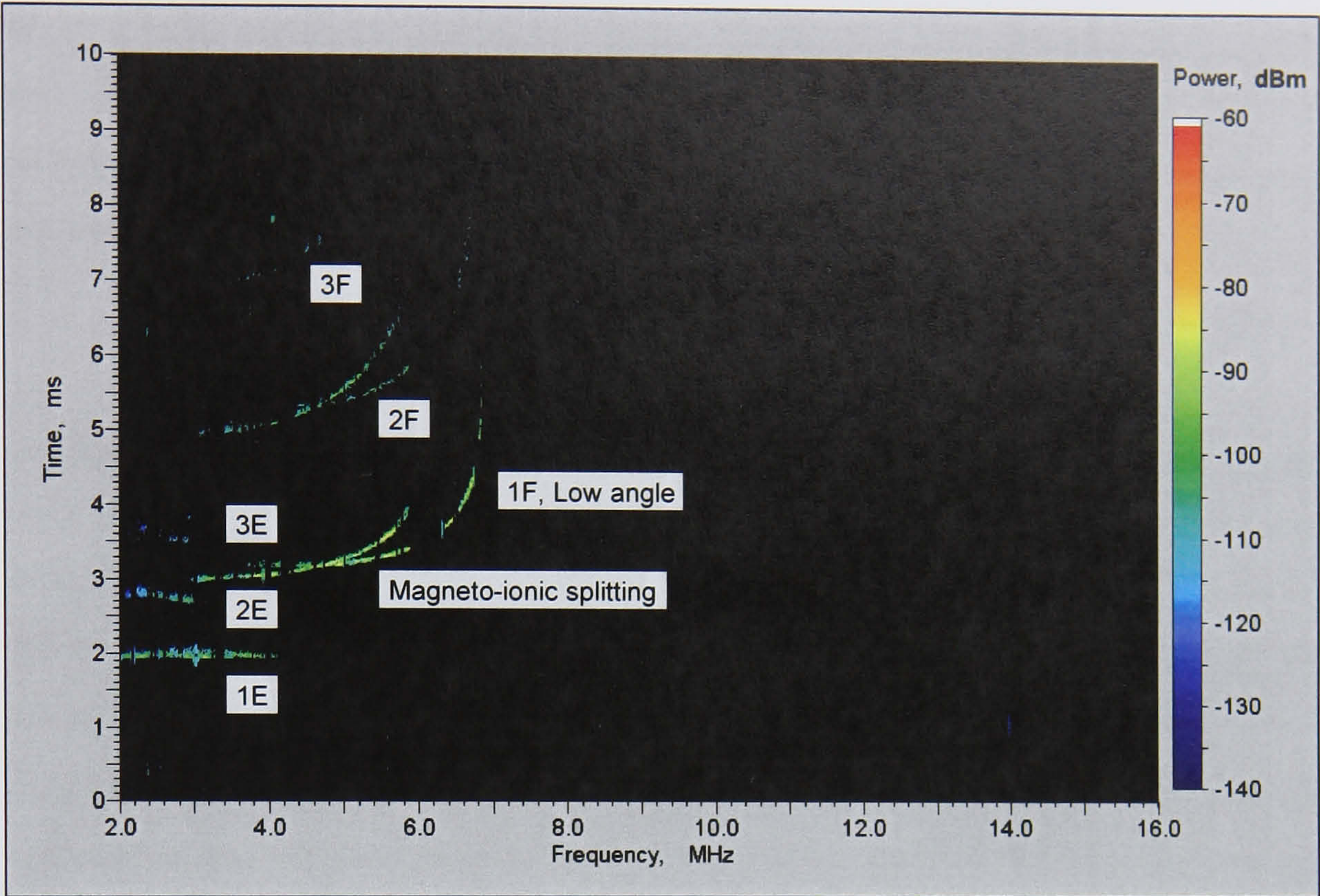


Figure 2-9 Typical Oblique HF Ionogram (Malvern to Farnborough 17:31 20-03-200)

The coherence bandwidth of a system is proportional to the reciprocal of the multipath dispersion. In a system with a bandwidth smaller than the coherence bandwidth the impact of multipath is observed as non-frequency selective ‘flat’ fading. In a system with a bandwidth greater than the coherence bandwidth the fading will be observed to be frequency selective as the interaction of the multipath components varies between constructive and destructive interference as a function of frequency.

2.4.3 Doppler Effects

There are two principal mechanisms that cause Doppler effects to be applied to propagating signals: ionospheric Doppler and platform induced Doppler.

Ionospheric Doppler is caused when the reflecting layer is moving in such a way that the overall path length is changing. The Doppler shift is proportional to the rate of change of the phase path. For a signal with frequency, f_c , relative velocity, v , travelling close to the speed of light, c , Doppler shift, f_D , is:

$$f_D \approx \frac{f_c v}{c} \tag{2-3}$$

Given a radio wave reflecting off a single, ionospheric layer moving vertically with speed v_v , the imposed Doppler shift will be related to the angle of incidence with the reflecting layer, ϕ . There also arises a factor of two because both the upward and downward phase path lengths are changing:

$$f_D \approx -\frac{2f_c v_v}{c} \cos \phi \quad (2-4)$$

In addition to purely vertical movements (such as normal diurnal changes or due to rapid changes in ionisation caused by ionospheric disturbances), ionospheric Doppler shifts can be caused in more complex situations. Examples include off-great circle reflections from moving irregularities, high angle sky wave propagation through an inhomogeneous ionosphere etc.

Clearly, Doppler shift can also be imposed on a radio wave by the component of velocity of the receiver relative to the transmitter (normal to the direction of propagation). Values of radio platform induced Doppler shift are generally larger than those caused in the ionosphere particularly for fast moving platforms such as aircraft. Equation (2-3) is applicable. For example at 90 km/h (25 ms^{-1}) the maximum induced Doppler shift imposed on a 10 MHz signal would be $\sim 0.8 \text{ Hz}$. An aircraft travelling at 300 ms^{-1} would produce a Doppler shift of $\sim 30 \text{ Hz}$ on a 30 MHz signal. A useful ‘rule-of-thumb’ is that the Doppler shift produced by a moving radio platform is ‘*One Hertz per Mach per Megahertz*’. The acquisition and tracking of signals in the presence of changing Doppler shift, i.e. Doppler rate, is particularly challenging.

The same effect as Doppler shift can also be caused by frequency offsets between radio system equipments due to frequency reference errors or setting errors is colloquially termed Doppler offset. It is typical for HF radio systems to be designed to operate with a frequency offsets of up to $\pm 75 \text{ Hz}$ to cope with the combined total frequency offset.

2.4.4 Fading and Doppler Spread

The term fading is generally applied to any situation in which there is a variation of received signal energy with time. This may be caused by mechanisms at work within a single propagating mode (intra-mode fading) as identified in Table 2-1 or due to interference between modes (inter-mode fading); Table 2-2.

The interference of multiple modes leads to the establishment of patterns of constructive and destructive interference repeated at the fading rate. This results in frequency selective fading. For a channel with two multipath components, which have an inter mode separation of d s, the correlation bandwidth of the channel is approximately $1/d$ Hz [Proakis, 14, p764]. Where the fading is caused within a single mode it generally results in non-frequency selective fading termed flat fading.

Cause of Intra-Mode Fading	Fading Type	Fading Period	Comments
Small scale irregularities in F-region.	Flutter	10 -100 ms	Typically associated with Spread-F.
Movement of irregularities in ionosphere.	Diffraction	10 - 20 s	Typically follow a Rayleigh distribution.
Rotation of axes of polarisation ellipse.	Polarisation	10 - 100 s	Requires both O and X magneto-ionic components.
Curvature of the reflecting layer [Davies, 3].	Focusing	15 - 30 min	
Time variation of ionospheric absorption.	Absorption	60 min	Has greatest impact at sunset and sunrise.
Time variation of the MUF	Skip	Usually non-periodic	

Table 2-1 Summary of the Causes of HF Fading within a Single Propagation Mode

Mechanisms that cause fast fading (fade periods of less than ~10 s) are of particular interest to the designers of HF data communications systems because they have a major impact on modulation schemes that rely on amplitude or phase stability and thus often require special adaptive processing to overcome them.

Fading Type	Fading Period
High/low angle rays	0.5 - 2 s
Sky waves	1 - 5 s
Groundwave/skywave	2 - 10 s
Magneto-ionic splitting	10 - 40 s

Table 2-2 HF Fading Due to Inter-Mode Interactions

Frequency dispersion of a propagating signal is termed Doppler spread. It may be caused by a number of mechanisms associated with the fine structure of the ionosphere. Varying degrees of off-great circle propagation can result in a signal containing a continuum of Doppler shifts (due to systematic variations in the phase path length). Experimental work by Watterson et al [Watterson, 12], [ITU,13] suggested that mid-latitude Doppler spread in narrowband channels could be modelled using a Gaussian

distribution. However, where the reflecting layer is tilted or moving with a component of velocity perpendicular to the principal direction of propagation the resulting Doppler spread is likely not be Gaussian or even symmetrical.

2.5 Propagation Diversity

The preceding description of the perturbations suffered by trans-ionospheric radio waves indicates the difficulty of developing HF radio communications systems. However these mechanisms result in inherent diversity that can sometimes be exploited to improve the quality and availability of communications:

- **Time-of-Arrival/Frequency Diversity** – Where a multi-mode signal is received, each mode will generally have uncorrelated Doppler spread. In a Rake type receiver [Proakis, 14, pp797-806] these can be re-combined providing diversity gain. Essentially this exploits in-band frequency diversity where the channel bandwidth significantly exceeds the correlation bandwidth.
- **Spatial Diversity** – As two closely spaced receivers are moved apart the correlation between the received signals decreases (as their paths through the inhomogeneous ionosphere become significantly different). The correlation distance is defined as the distance at which the correlation coefficient reduces to $1/e$. Useful spatial diversity can be obtained with antenna separation distances of a few wavelengths, with a spacing of $\geq 10\lambda$ being considered to provide a high degree of de-correlation, defined as a correlation coefficient < 0.61 , [ITU, 15].
- **Polarisation Diversity** – Since, even where signals are launched with a single polarisation rotation in the polarisation ellipse results in signals being received with significant polarisation de-correlation. Experiments by workers such as Jorgenson et al [Jorgenson, 16] have demonstrated that co-located antennas with orthogonal polarisation can provide the same benefits as spatial diversity.
- **Angle-of-Arrival Diversity** – Where modes propagate through the ionosphere and arrive at the receiver at differing elevations they may be resolved using an antenna array that separates signals by angle-of-arrival (i.e. using a beam former). By this means signals that would otherwise not be resolvable and appear as flat fading (due to the finite signal bandwidth) may be resolved and exploited independently.

- **Out-of-band Frequency Diversity** – Out-of-band frequency diversity can be exploited in multi-channel or frequency agile communications systems to exploit the significant de-correlation and gross differences in propagation conditions at different frequencies across the HF band. This is increasingly being used in modern systems as a second order adaptation mechanism to maintain the quality and availability of logical communications links.

2.6 Propagation at Different Latitudes

As previously described the physical processes perturbing HF radio wave signals vary with geomagnetic latitude. These generally have their greatest impact when control points (ionospheric reflections) occur at high latitudes (typically $>65^\circ$ N) or close to the equator. The results of detailed measurement campaigns at different latitudes can be found in results published by a number of workers; [Watterson, 12], [Shepard, 17], [Angling, 18], [Cannon, 19], [Wagner, 20] etc).

Table 2-3 provides a useful (if necessarily crude) summary of applicable multipath and Doppler spread values at different latitudes under quiet, moderate and disturbed geomagnetic conditions [ITU, 13]. In this table differential time delay is defined as the multipath delay between two modes representing the first and last principal modes, while the frequency spread is the 2σ value of a Gaussian power distribution.

Latitude	Conditions	Differential Multipath	Doppler Spread 2σ	Comment
Low-Latitude	Quiet	0.5 ms	0.5 Hz	
	Moderate	2 ms	1.5 Hz	Equivalent to ‘CCIR Poor Channel’ as per ITU-R F.520
	Disturbed	6 ms	10 Hz	
Mid-Latitude	Quiet	0.5 ms	0.1 Hz	Equivalent to ‘CCIR Good Channel’ as per ITU-R F.520
	Moderate	1 ms	0.5 Hz	Equivalent to ‘CCIR Moderate Channel’ as per ITU-R F.520
	Disturbed	2 ms	1.0 Hz	Equivalent to ‘CCIR Poor Channel’ as per ITU-R F.520
	Disturbed NVIS	7 ms	1.0 Hz	Additional ground-wave components should be added if required.
High-Latitude	Quiet	1 ms	0.5 Hz	Equivalent to ‘CCIR Moderate Channel’ as per ITU-R F.520
	Moderate	3 ms	10 Hz	
	Disturbed	7 ms	30 Hz	

Table 2-3 Representative Channel Parameters for Comparative Testing [from ITU, 13]

In addition the following occurrence statistics for disturbed conditions are noted in ITU Recommendation F.1487:

- **Low latitudes** - Differential time delays of 4 ms will be exceeded approximately 5% of the time. Doppler spreads of 3 Hz will be exceeded approximately 5% of the time.
- **High latitudes** - Differential time delays of 5 ms will be exceeded approximately 5% of the time. Doppler spreads of 25 Hz will be exceeded approximately 5% of the time.

2.7 Propagation of Wideband Signals

A small number of workers have researched the propagation of wideband HF signals (wideband being defined as bandwidths greater than ~12 kHz) and made applicable measurements. Of particular note is the work carried out by the MITRE Corporation and US Naval Research Laboratory (NRL) which included measurements of wideband Skywave channel parameters at mid-latitudes [Perry, 21], [Rifkin, 22], [Rifkin, 23] and

at high latitudes [e.g. Wagner, 20] in support of studies into possible direct sequence spread spectrum (DSSS) communications systems. In addition to presenting the observed time dispersion, Doppler shift and Doppler spread, the results confirmed that the large measurement bandwidths employed exceeded the channel coherence bandwidth and signal fading depths were greatly reduced (by 10 dB when increasing the bandwidth from 4 kHz to 1 MHz). Further, measurements indicated that the HF channel was essentially stationary for ~ 10 s on the benign paths measured.

This work, together with theoretical studies by workers such as Milsom [Milsom, 24], indicate that the following may have a significant impact on wideband signal propagation:

- **Exceeding coherence bandwidth** – leading to a reduction in flat fading;
- **Group time delay slope (GTDS)** – because of the large bandwidths employed the delay slope may be appreciable (compared with symbol durations in a wideband communications system, for example);
- **Changes in Virtual Height** – Changing virtual height of the ionospheric layers or, more particularly, the resulting rate of change of mode delay may be appreciable. Observations of Doppler shift indicate that rates as great as 250 ns/s may occur due to changing layer heights;
- **Delay Jitter** – the possible existence of resolvable delay time jitter has been suggested [Ince, 25]; and
- **Mode Stability** – the phase stability within a mode including its dispersive elements and the extent to which correlation occurs within a dispersed mode. This has not previously been investigated in detail.

Wideband HF channel measurements have also been reported for ground wave propagation over an essentially smooth (i.e. non-mountainous) surface [Barsoum, 26]. The associated measurements indicated that the channel did not place any limitations on wideband systems (up to ~ 1 MHz) and the path loss was the same for both wideband and narrowband signals.

2.8 Noise and Interference

2.8.1 Environmental Noise

Radio interference from environmental noise sources and other emitters, both intentional and unintentional, has a significant affect upon HF radio systems. Environmental noise at HF frequencies includes both natural sources (including Galactic and Atmospheric caused by electromagnetic radiation due to lightening discharges) and man made components (e.g. car ignition, rotating electric machines). The level of man-made noise is highly correlated with human activity in the vicinity of interest. Values typically used in HF systems planning recognise that link margins can be reduced by tens of decibels, particularly at the bottom of the band [Maslin, 5], [ITU, 27], [ITU, 28], [ITU, 29]. Values from [ITU, 29] are plotted in Figure 2-10.

Radio noise is often treated as AWGN although a combined AWGN and impulsive noise model more accurately incorporates both the ambient and atmospheric (generally lightning induced noise spikes can be detected many thousands of kilometres away). Such a model, with a world map specifying the driving parameters, is presented in CCIR Report 322 [ITU, 27] and more recently ITU-R P.372 [ITU, 29] but remains known colloquially as ‘CCIR-322 noise’.

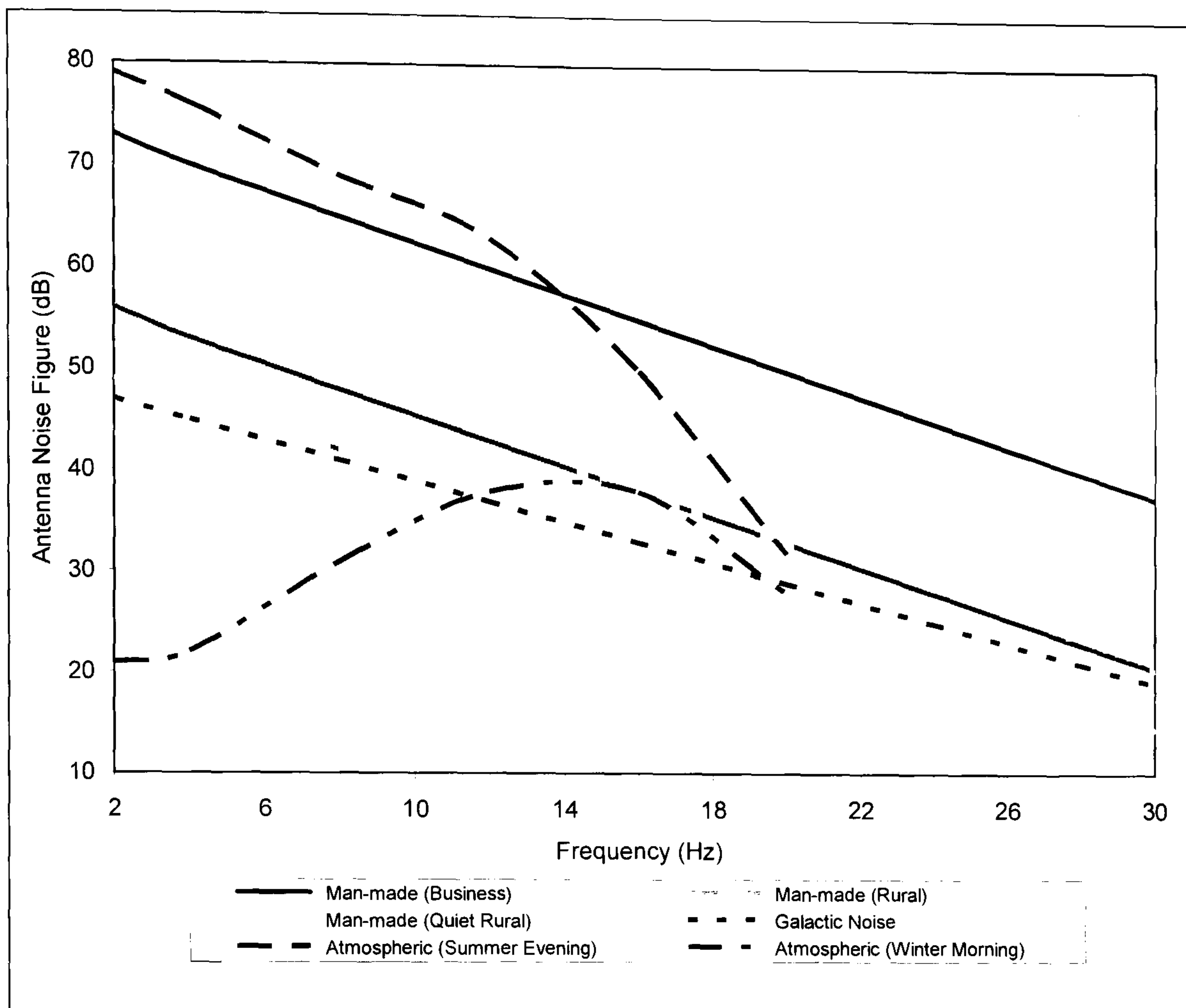


Figure 2-10 Effective Noise Figure of a Loss-less Isotropic Antenna Due to External Noise in the HF Band [ITU, 29].

2.8.2 Spectral Occupancy

It has been shown [Gott, 30], [Pantjiaros, 31] that it is possible to statistically model the probability that a channel of a given bandwidth is occupied by a signal above a certain power level i.e. that it is occupied. The latest stable day and stable night model are based on ~9 years of measurements at four sites in Europe (including one at high latitude). They predict congestion on a frequency given its ITU frequency allocation number (1 to 95), allocation centre frequency, bandwidth, location (latitude/longitude), Sunspot number, week (1 to 52) and incident field strength threshold. Figure 2-11 shows a typical prediction of occupancy for both stable day and stable night using the model variant published by Economou et al [Economou, 35]. The impact of day-time absorption (most prevalent in the summer) and of the reduced MUF at night-time can clearly be seen. More latterly this work has been extended to include consideration of low and high angle reception and azimuthal angle of arrival [Pantjiaros, 36], [Pantjiaros, 37].

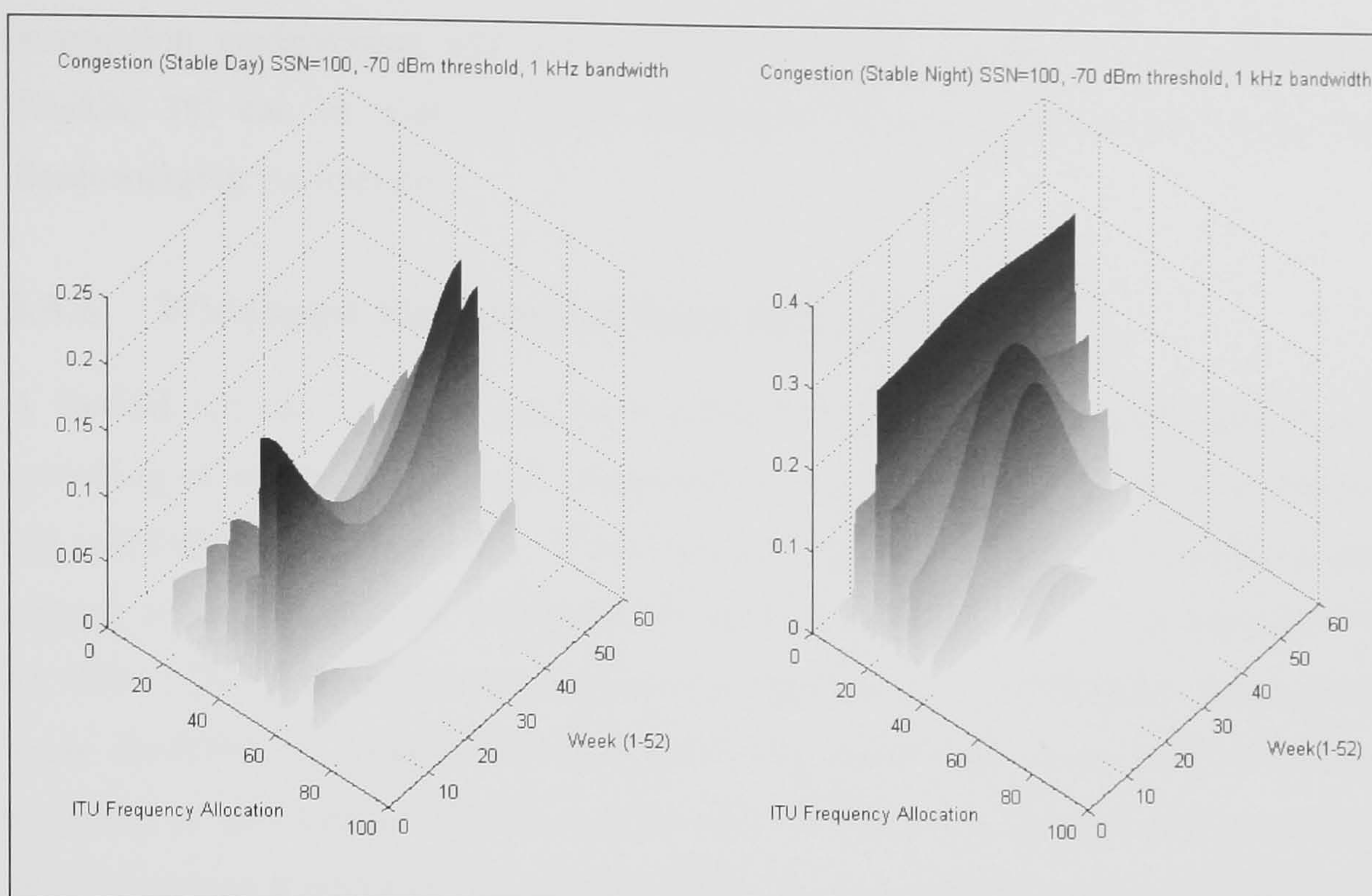


Figure 2-11 Predicted Congestion from Gott-Laycock Occupancy Model

2.8.3 Interference and Jamming

The impact of co-channel interference (interference from other users), is related to diurnal and seasonal propagation conditions, frequency of operation and geography. For example, the interference environment in central Europe is particularly dense as there are a great many HF users. The problem is exacerbated at night, when propagation constrains users to the lower part of the HF band but often supports signal propagation over long ranges. The reasons for the existence of co-channel interference include the same frequency being allocated to many users of an HF network, long range propagation of frequencies allocated to different users in different ITU world regions and misuse.

Deliberate interference, or jamming, can be used to disrupt communications by either degrading communications or by introducing spurious signals that are misinterpreted as being valid (spoofing). Basic classes of jamming include a wide range of techniques from simple pulse and noise jammers to sophisticated follower jammers and waveform spoofing or re-play attacks. Jammers and interferers are subject to the same physical propagation mechanisms as is the communications signal. However, the path geometries for a wanted signal and an interfering one to a victim receiver may be very different (particularly for the sky wave mechanism). With an understanding of the

propagation environment and likely emitter locations models such as HF-EEMS [Shukla, 38] can be used to select frequencies favouring the wanted signal but disadvantaging the interferer.

2.8.4 Wideband Modelling of Noise and Interference

A limited amount of work has been published relating to the investigation and modelling of wideband noise and interference by workers such as Lemmon [Lemmon, 32] and Fishman [Fishman, 33]. These sources analyse wideband measurements and suggest a basic model for wideband HF noise and interference in a bandwidth of ~ 1 MHz. The proposed model consists of a Gaussian noise component, atmospheric noise modelled by filtered impulses (Delta functions) and narrowband interferers modelled as sine waves. The results presented are based on a limited data set and the need to analyse a wider variety of atmospheric noise conditions is acknowledged as is the need to improve the understanding of the changing nature of man-made interference with time (to which the more recent work by Gott and his co-workers is directly applicable).

2.9 HF Channel Models and their Application

2.9.1 Introduction and History

Channel simulators have been used for many years to evaluate the performance of data modems. They allow testing to be carried out using repeatable, well specified propagation conditions and allow performance comparisons to be made between different modems. Additionally, they allow simulation of a wide range of propagation conditions, whilst avoiding the expense of extended on-air testing.

Common HF channel simulation techniques can, for convenience, be split into four basic classes, as follows:

- Replay simulators;
- Raleigh Fading (Watterson) Model;
- Wave Propagation Based Models; and
- Advanced Parametric Simulators.

The basic implementation, application and limitations of the four classes are considered in the following sections.

In order to support scenario modelling, i.e. other than fixed channel conditions, it is necessary to be able to change the driving parameters of the channel model as a function of time and, in the case of simulating mobile users, position.

2.9.2 Replay Simulators

The transmission of a signal through a communications channel can be written as a convolution of the transmitted signal with the channel impulse response, viz:

$$y(t) = x(t) * h(t, \tau) + n(t) \quad (2-5)$$

where t is the time variable, τ is the delay variable, $x(t)$ is the input signal, $y(t)$ is the output signal, $h(t, \tau)$ is the time variant channel complex impulse response (CIR), and $n(t)$ is a noise signal.

Replay simulators, as their name suggests, replay the exact channel conditions that existed at the time when a channel was measured. This is done by repeatedly measuring and storing estimates of the channel CIR [Giles, 34]. These can then be directly utilised to drive the coefficient taps of a linear phase finite impulse response (FIR) filter which convolves the test signal with the ‘replayed’ channel characteristic. A number of criteria must be met for a replay simulator to accurately model the measured channel. It must sample the complex impulse response sufficiently often that the convolution filter adaptation is realistic and that non-realistic discontinuities in the channel response do not occur.

The biggest advantages of true replay simulators are that they are conceptually simple and that, if the channel CIR is accurately determined, they can model a channel exactly. However, this class of simulator only allows simulations for actually measured channel conditions. Therefore, for broad applicability, a comprehensive database of propagation ‘scenarios’ is required. Replay simulators do not really contain a channel model so their implementation and use confers no knowledge of the physical mechanisms at work or their manifestation. Additionally, the quantity of data required for any simulation is directly proportional to the bandwidth and the length of the simulation (i.e. extremely

large). They do not allow ‘what if’ type testing that aims to explore situations for which data has not already been collected.

2.9.3 Watterson Model

Most narrow band HF simulators are based on the Watterson model [Watterson, 12]. It has been the standard representation of the HF channel used in simulators for many years. This model considers the channel as an ideal tap delay line (Figure 2-12), where at each tap the delayed signal can be modulated by a tap gain function $G_i(t)$.

In general, each tap gain function is defined by:

$$G_i(t) = \tilde{G}_{ia}(t)e^{j2\pi\nu_{ia}t} + \tilde{G}_{ib}(t)e^{j2\pi\nu_{ib}t} \quad (2-6)$$

where the subscripts a and b indicate the two possible magneto-ionic components, the exponentials allow Doppler shifts to be added to the signal, and the tildes indicate that the G terms are sample functions of two independent complex Gaussian ergodic random processes, each with zero mean values and independent real and imaginary components with equal RMS values that produce Rayleigh fading. The tap gain functions are then specified so as to produce a Gaussian Doppler spread on the signal, and one tap is used for each propagation mode.

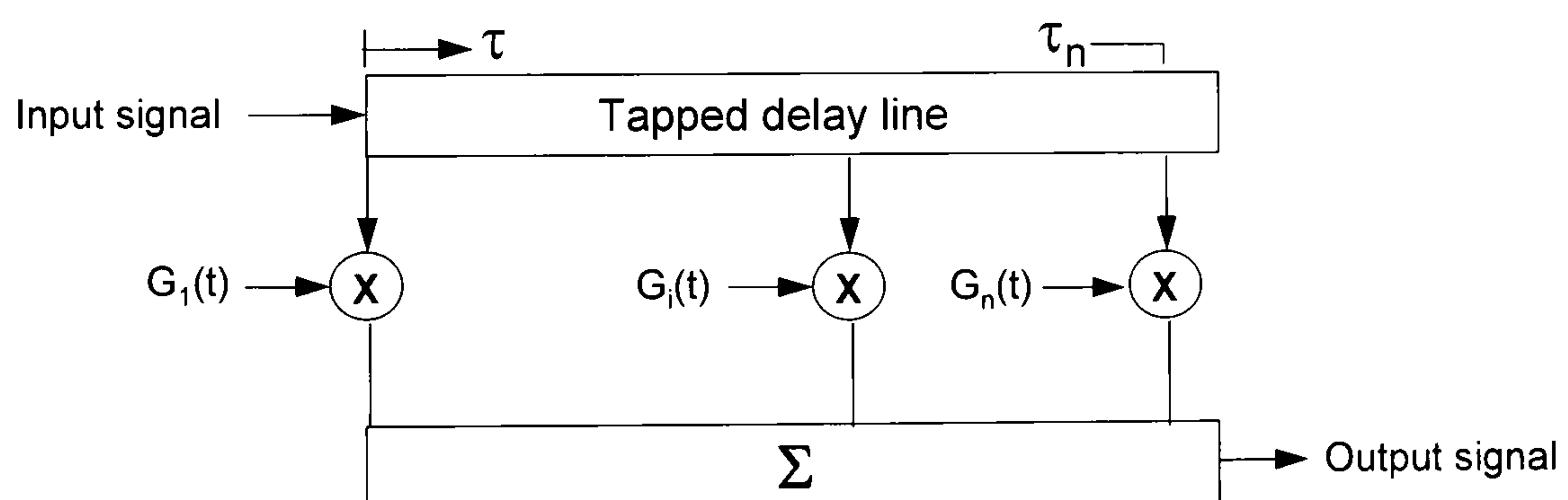


Figure 2-12 Block diagram of Watterson model.

In practical implementations of Watterson simulators, only a single magneto-ionic component is simulated, and a limited number of propagation modes (taps) are allowed (generally 4 or 5). A facility to include a specular mode is usually provided, which can be used to simulate a direct (non-fading) propagation path.

The Watterson model was validated using 36 minutes of mid-latitude data that was taken on a 1300 km path during quiet ionospheric conditions on a single day in

November 1967. The model is restricted by the constraints that the channel fading must be Rayleigh in nature, that any Doppler spread has a Gaussian power spectrum, and that none of the modes exhibit delay spread. Also, the model was only verified for narrow bandwidths (up to 12 kHz). Although simulators based on this model have proven extremely useful, they are not satisfactory for testing equipment specifically designed for use in conditions not concomitant with the restrictions of the Watterson model, such as those experienced at high and equatorial latitudes. This has led to a desire to develop new HF channel models.

The Watterson model, whilst it contains a parametric channel model, does not specify the driving parameters. The lack of a model for the occurrence statistics of multipath and Doppler effects is a significant limitation. In actual fact, no comprehensive, global model exists for Doppler effects¹. Simulator testing can, therefore, be conducted in two ways: either a limited number of simulator tests may be devised which, it is hoped, cover the most probable multipath and Doppler conditions; or the simulator may be driven by measurements collected on a real ionospheric path (i.e. a replay simulator). Both methods have limitations. A limited number of simulator tests may not cover all eventualities and the weight that the results from a particular test should be given may not be known. Equivalently a replay simulator must have data sets that are representative of a sufficient number of different paths so that any reasonable deployment may be tested.

2.9.4 Wave Propagation Based Channel Models

For many years effort has been applied to developing more sophisticated HF propagation models, for the most part to develop more accurate propagation prediction codes. The more advanced models are based on ray tracing (e.g. [Norman, 39], [Vastberg, 40], [Gherm, 41]) through a parametrically specified or fully specified model of the physical ionospheric. Their highly computationally intensive nature has, to date, made their use in simulators impractical. However, wave propagation approaches still have an important part to play in helping to understand the physical mechanisms present and verifying simulator models.

¹ Work by Angling et al [Angling, 18]; Cannon, 19] has started to address this problem by making long term measurements to quantify the occurrence statistics of Doppler spread at different latitudes.

2.9.5 Advanced Parametric Channel Models

An alternative approach to wave propagation based modelling has been work to develop more sophisticated channel models that attempt to faithfully reproduce the gross effects of the real channel. Of particular note is the improved ionospheric channel model that has been proposed by Vogler et al of the US Institute of Telecommunication Sciences (ITS) [Vogler, 43]. The model includes asymmetric delay spread power profiles and non Gaussian fading, but simplifies to the standard Watterson model for zero delay spread and Gaussian fading. Although developed as a wide-band model, the ITS model can also be applied to narrow band channels. An introduction to the ITS channel model including a description of its formulation is provided in Appendix B. The model has been used as the basis for a number of channel simulator implementations (e.g. [Mastrangelo, 44], [Behm, 45], [Angling, 46]).

2.9.6 Improving the Fidelity of Wideband HF Channel Models

The ITS wideband model is capable of reproducing good approximations of the macroscopic features that have been observed for a limited number of HF channel measurements used in developing the model. There are a number of areas in which the veracity of the model has not been verified:

- The choice of delay power profiles and fading characteristics for wideband HF system evaluations is unclear as few real measurements have previously been made and so only very limited data exists;
- It remains unclear how fading within a single propagation mode should actually be related as a function of delay time - the ITS model assumes that fading is uncorrelated with delay time but there is no clear evidence for this;
- In order to be physically representative wideband models must be able to reproduce variations that occur as a function of carrier frequency (e.g. group delay slopes); and
- The model is complex and requires a large number of input parameters to fully specify a single propagation condition (a similar criticism may be levelled at the Watterson model but its relative simplicity lessens the impact). Workers have sought to address this particular difficulty in different ways. The work of

Strangeways et al [Strangeways, 47] has led to the development of an enhanced simulator based on a detailed physical ionospheric model whilst the work of Angling et al [Angling, 46] has produced an enhanced parametric HF simulator driven by a time series of HF measurements.

In order to address these limitations there is a clear need to undertake more work including making detailed measurements of the characteristics of individual propagation modes. Chapter 10 of this thesis details relevant new work which undertook detailed wide bandwidth propagation measurements in order to investigate the structure of individual propagation modes.

2.9.7 Summary – HF Channel Models

This section has reviewed both established and recent work to develop HF channel models with good fidelity. It is concluded that the well established Watterson model is useful for simulation of narrowband channels (up to ~12 kHz bandwidth). Other models are being developed for wider bandwidths but the need for more work has been identified to ensure that these are truly representative.

2.10 HF Propagation – Summary of Principal Characteristics

This chapter has introduced HF propagation and, in particular, discussed the sky wave mechanism used to support long range BLOS communications. Signals propagating through the HF environment can display gross characteristics that significantly affect the management and performance of communication systems:

- Attenuation;
- Multipath and dispersion;
- Doppler spread (fading);
- Doppler shift;
- Environmental noise;
- Interference;
- Variations due to path geography; and
- Diurnal, seasonal and solar cycle variations.

The combination of these channel characteristics, the limited HF spectrum resource and the bandwidth of standard frequency allocations necessarily constrains the data throughput that can be reliably achieved. With current technology HF data rates of between 75 and ~2400 bits per second (bps) are typical in a standard bandwidth of 3 kHz with the latest generation of modems able to provide up to 9.6 kbps under favourable conditions. New work is being undertaken to specify even higher data rates for applications such as digital broadcasting - Digital Radio Mondiale (DRM) [Stott, 50] being a key example.

The use of wider bandwidths requires consideration of both the gross (macroscopic) and fine (microscopic) characteristics of the channel. At the macroscopic level these include, in particular, changes in propagation characteristics as a function of frequency. At the microscopic level, the increased bandwidth allows separation of modes that would be not be resolvable in narrowband systems. Of particular interest is whether the microscopic structure of modes, including phase stability and timing jitter as suggested by workers such as Milsom [Milsom, 24] is significantly different to that observed in narrowband systems.

Having introduced some of the key features of the HF propagation and noise environment in this chapter the next chapter considers the implementation of radio data communications and techniques used to communicate traffic reliably over HF paths.

Chapter 3.

HF Data Communications

For many years the principal information passed over radio channels was analogue (e.g. voice, analogue television). Communications are now increasingly dominated by a requirement to pass digital data; whether digital information (text messages, file transfer, internet browsing etc), or digitised analogue information (digital voice, images). Radio data communications systems designs generally seek to transfer the required information as efficiently as possible (minimising transmission time, bandwidth and transmit power).

This Chapter considers the key technologies used to implement waveforms for narrowband HF data communications and then introduces some techniques applicable to wideband, high throughput communications.

3.1 Waveforms for Data Communication Over Fading, Multipath Channels

In order to successfully communicate over fading, multipath channels (such as skywave HF), the communications waveform and reception signal processing must be carefully specified including:

- Modulation Scheme;
- Equalisation;
- Forward error control coding;
- Interleaving; and
- Synchronisation and tracking.

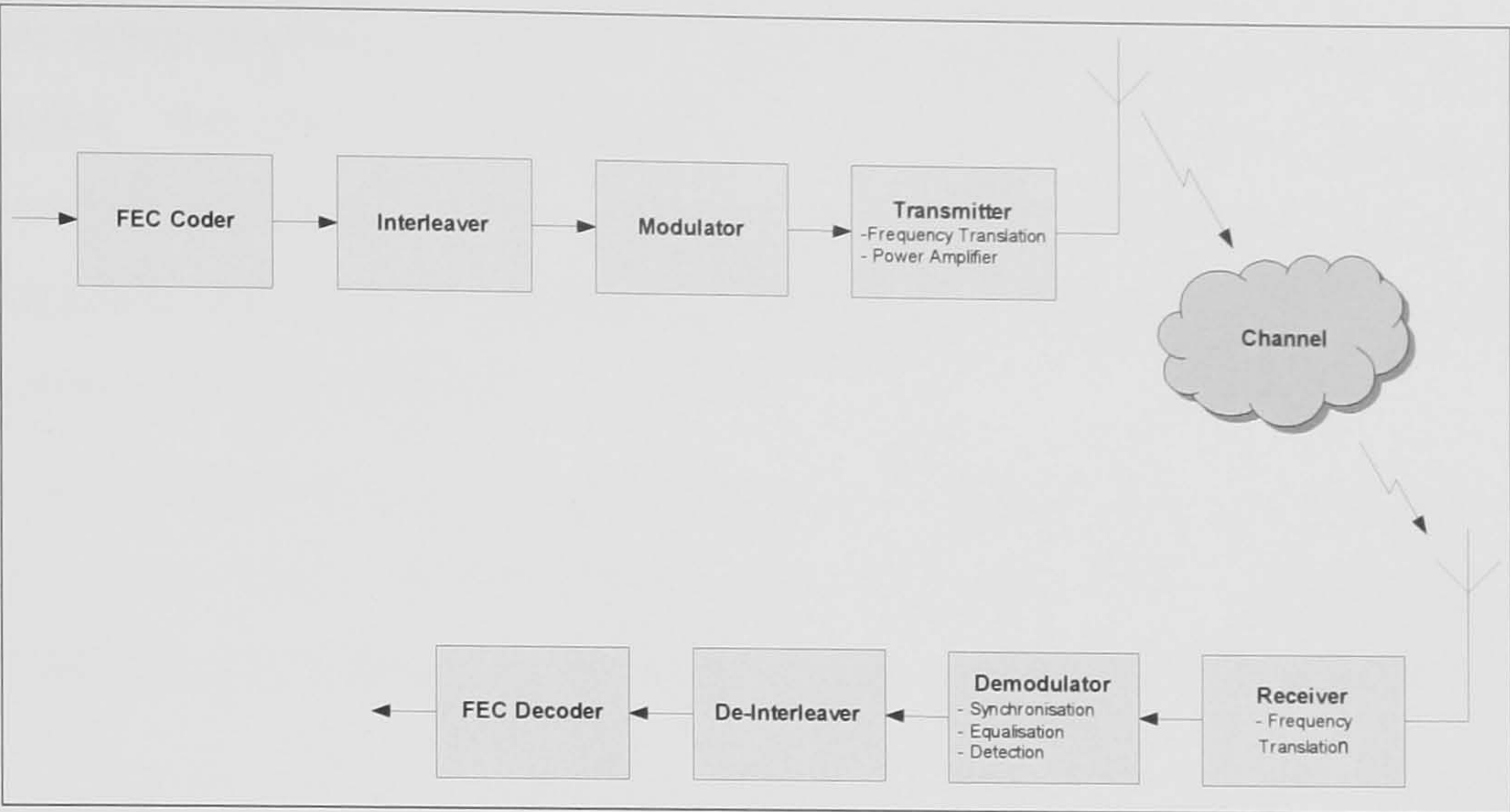


Figure 3-1 Components of a Generic Data Communications System

3.2 Modulation Schemes for Data Communications

Conventional communications utilise a signal format, $s(t)$, which is based on the modulation of a carrier signal:

$$s(t) = A_m(t) \cos[\omega_c t + \phi_m(t)] \tag{3-1}$$

where

- $A_m(t)$ is a time-varying amplitude modulation;
- $\omega_c t$ is the carrier ($2\pi f_c t$);
- $\phi_m(t)$ is a time-varying phase modulation.

Simple schemes apply either amplitude or phase modulation (of which frequency modulation is one form). More complex schemes employ both. For digital communications the size of the phase and amplitude changes are usually quantised, producing an alphabet of possible symbols. Information is communicated as a time series of these symbols. It can be seen that, in the limit, the alphabet of signal symbols approaches infinity as the quantisation interval is decreased thereby increasing throughput for a given symbol rate. However, as the signal space distance between unique symbols decreases the likelihood of noise or interference causing the correct symbol to be detected increases. The design of a signal therefore becomes a trade-off between the quantity of information that can be communicated per symbol and the signal's robustness.

For data communications, modulation changes are normally applied abruptly at symbol boundaries. Any discontinuities result in '*sinc(x)*' type time-domain ringing causing inter-symbol interference (ISI). This can be effectively controlled using Nyquist filtering using square root cosine filtering [e.g. Burr, 51] which forces the ISI to be zero at the symbol sampling interval.

It was shown by Shannon [Shannon, 52] that the maximum data rate, C , which can be received without error in an additive white Gaussian noise (AWGN) channel of bandwidth B , having a band-limited signal-to-noise ratio (SNR), S/N , is given by:

$$C = B \log_2 (1 + S/N) \text{ bits/s} \quad (3-2)$$

It is possible to re-arrange the Shannon equation, (3-2), to give a lower bound on the required energy-per-bit-to-noise ratio (E_b/N_0) to successfully convey a certain information capacity:

$$\frac{E_b}{N_0} \geq \frac{2^\eta - 1}{\eta} \quad (3-3)$$

where $\eta = C/B$ bps/Hz is the normalised capacity per Hertz of bandwidth, also termed the spectral efficiency.

It can be shown that there is an absolute lower bound on E_b/N_0 (irrespective of the complexity of the modulation and coding schemes employed) below which communication is not possible:

$$\lim_{\eta \rightarrow 0} \left[\frac{2^\eta - 1}{\eta} \right] = \ln(2) = 0.693 \text{ or } -1.6 \text{ dB} \quad (3-4)$$

In practice, it has proved very difficult to achieve anything close to the Shannon bound with even remotely achievable receiver complexity. Only with the discovery of iterative coding, so-called Turbo-codes, [Berrou, 53] in the mid-1990s have practical systems started to approach close to the Shannon bound.

This section provides a summary of the basic modulation techniques employed to convey data communications over a radio channel. The application of adaptive equalisation to mitigate the effects of multipath and Doppler spread is introduced. In addition, consideration is given to the use of error control coding techniques to reduce bit error rates (BERs) in a received transmission to a tolerable level.

3.2.1 Amplitude Shift Keying (ASK)

In amplitude shift keying the amplitude of the carrier is modulated by the data stream to be transmitted. In the simplest case this results in binary on-off keying (OOK) as depicted in Figure 3-2. A successful demodulation technique employs incoherent detection (envelope detection, Figure 3-3) and a Law assessor [Law, 54] to establish an adaptive decision threshold for each symbol based on the energy present in a number of preceding symbols. This helps to mitigate the impact of signal fading and interference. In a more general implementation of ASK, a number of binary symbols may be mapped to a multi-level amplitude modulation. This will increase the spectral efficiency (bps/Hz) at the expense of decreasing the signal's robustness. In practice ASK is not generally used, in part because of its poor power efficiency.

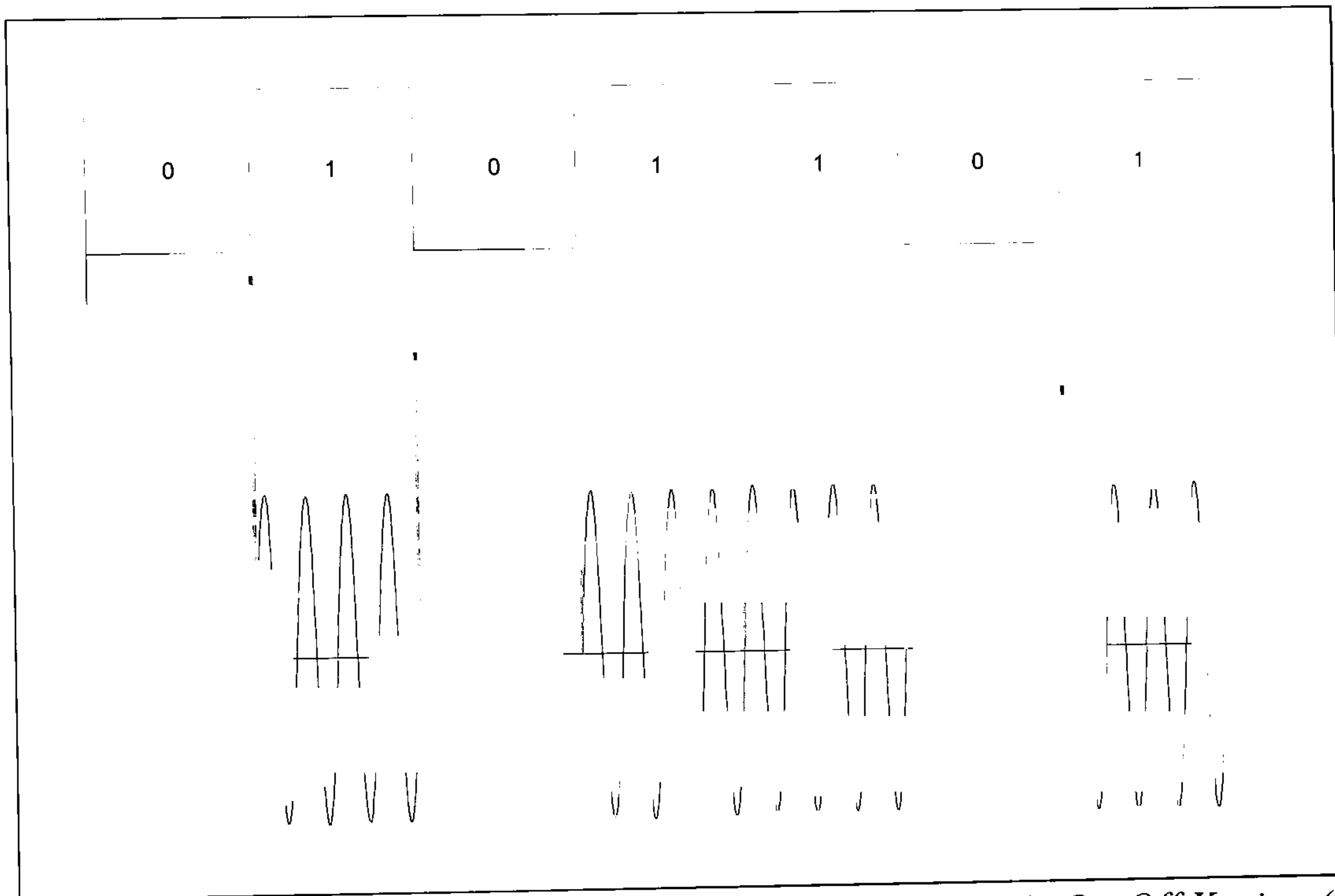


Figure 3-2 On-Off Keying (OOK)

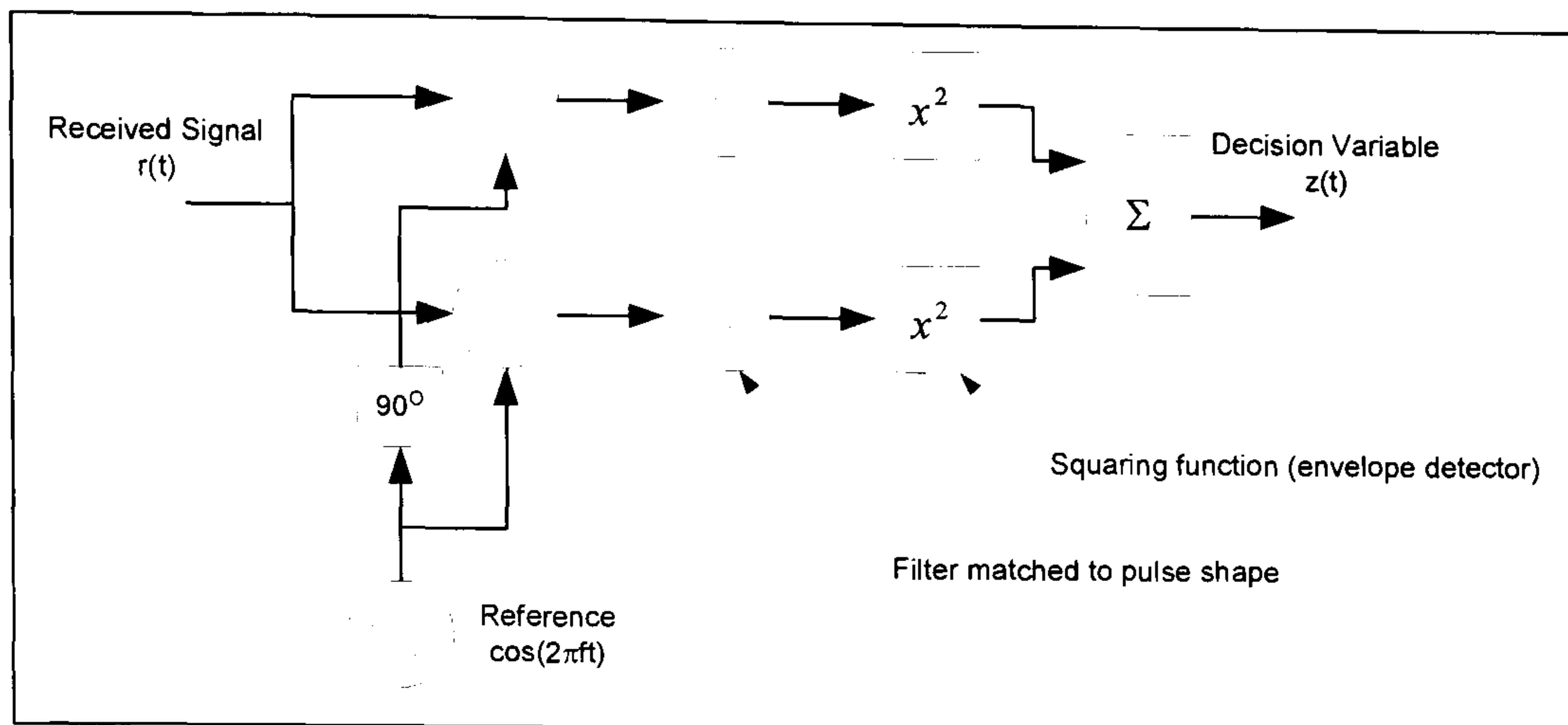


Figure 3-3 Non-coherent Matched Filter Structure

3.2.2 Frequency Shift Keying (FSK)

In binary frequency shift keying (FSK), as depicted in Figure 3-4, the binary data sequence to be sent is used to modulate the carrier frequency. This was traditionally implemented either phase continuously using a single voltage controlled oscillator (VCO) or, non-phase continuously, by switching between the output of two oscillators at the two tone frequencies, known as frequency exchange keying (FEK).

FSK may be received using a number of techniques. The optimum performance in an AWGN channel is obtained utilising orthogonally spaced tones [Burr, 51] and coherent detection using two matched filters. Two signals, $x_1(t)$ and $x_2(t)$, are orthogonal if their inner product is zero:

$$\int_{t_1}^{t_2} x_1(t)x_2^*(t)dt = 0 \quad (3-5)$$

For use on HF channels, wide deviation FSK, with non-coherent detection and a Law assessor is often utilised. Even though non-coherent detection suffers a penalty of ~1 dB compared with coherent detection in AWGN, this technique has increased robustness in a fading channel. To mitigate against narrowband interference and frequency selective fading the signal is detected as two independent OOK signals and then a decision is made given the additional knowledge that the two are complementary.

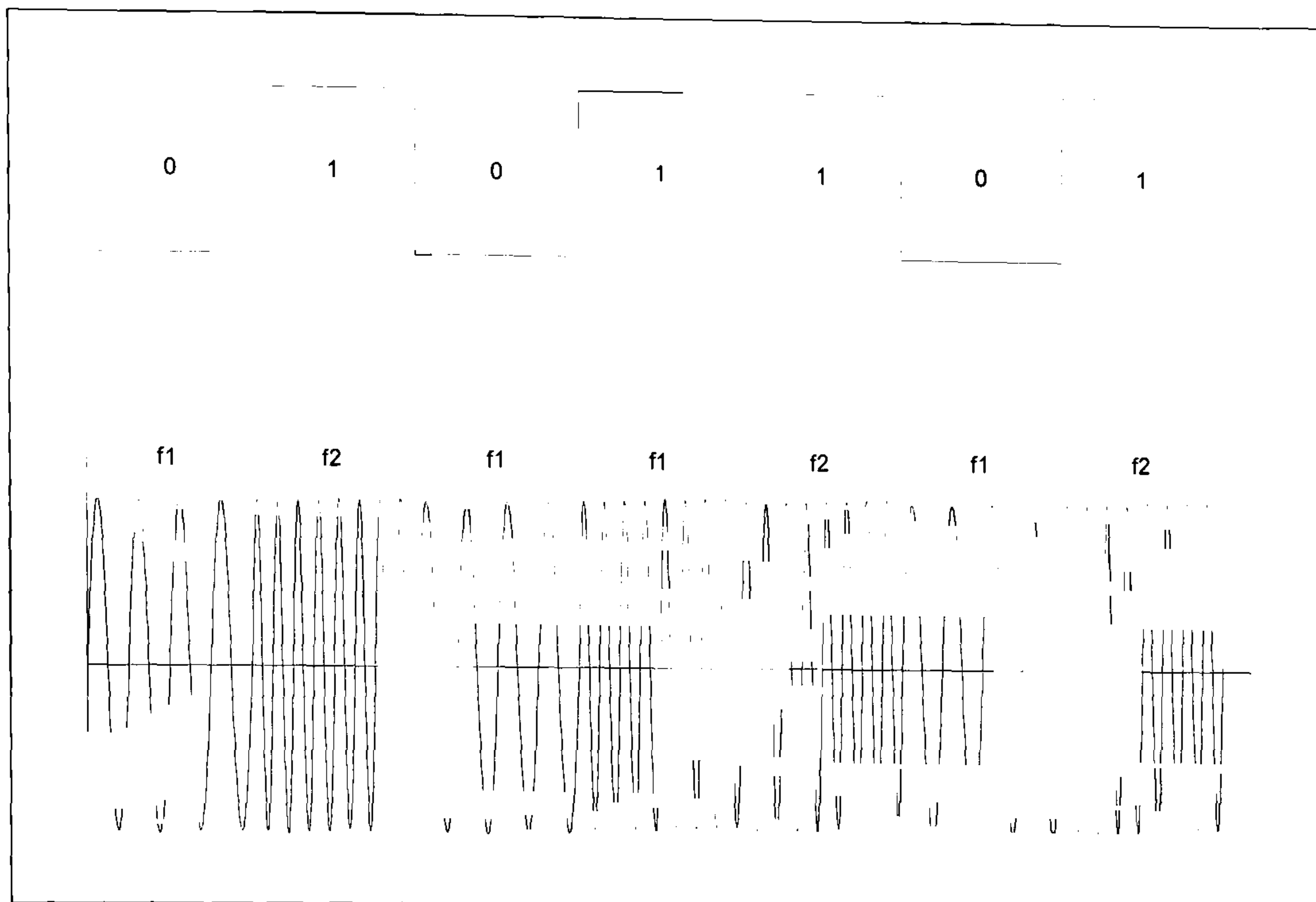


Figure 3-4 Frequency Shift Keying (FSK)

3.2.3 Multi-level Frequency Shift Keying (MFSK)

A generalised multi-level extension of binary FSK (2-FSK) is MFSK in which multiple tones are utilised. The source data is encoded into a stream of multi-bit symbols and each resulting symbol mapped to a particular tone frequency. If ' M ' tones are used, then each tone may carry ' k ' bits of information, where:

$$k = \log_2(M) \text{ or } M = 2^k \quad (3-6)$$

This is illustrated in Figure 3-5 for 8-ary MFSK. In this case $k=3$ consecutive bits are encoded into a symbol which is transmitted as one of eight possible tones.

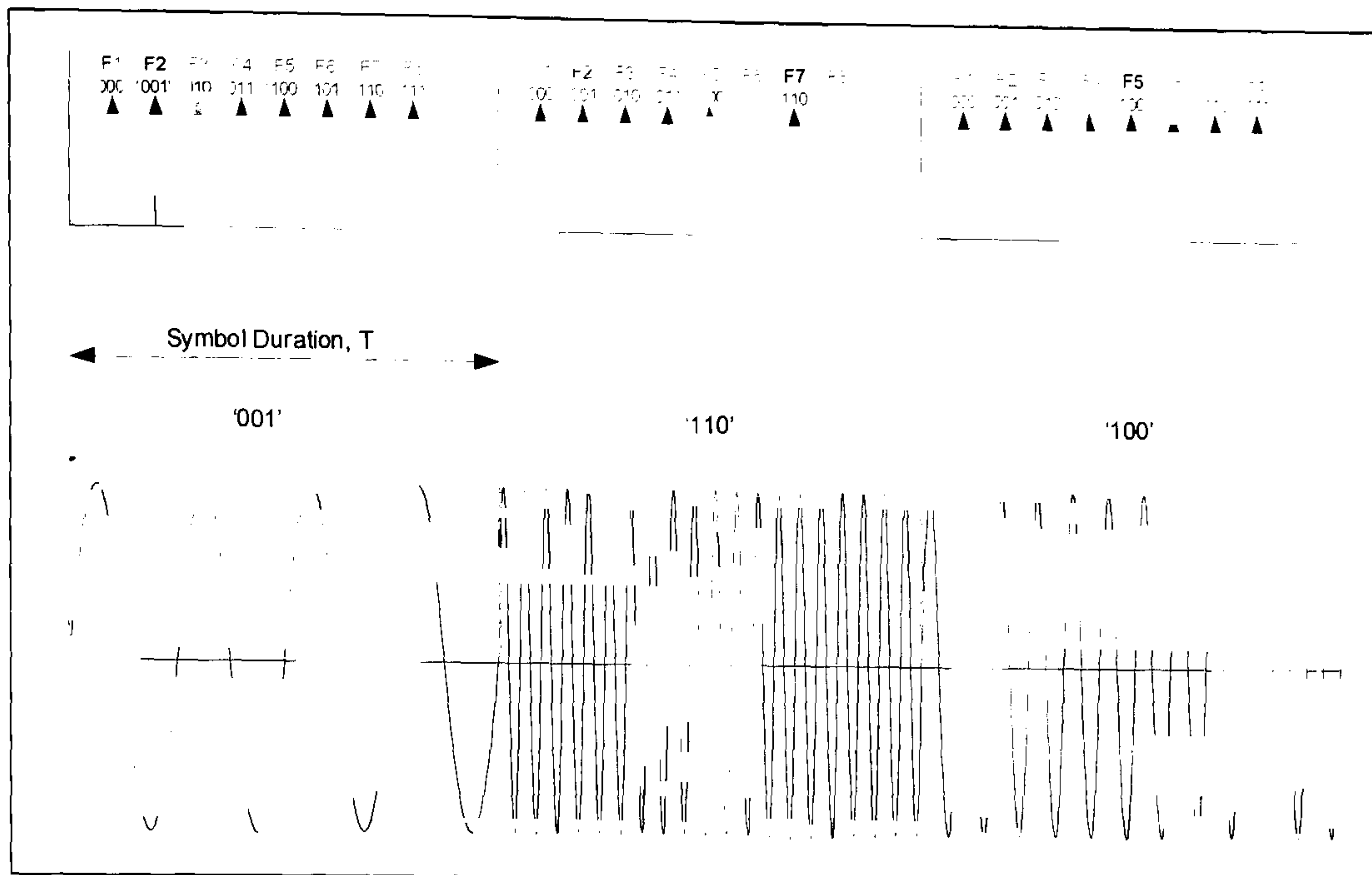


Figure 3-5 $M=8$, M -ary Multi-Frequency Shift Keying (MFSK)

MFSK receivers for use on fading radio channels generally employ a bank of non-coherent matched filters (as per Figure 3-3). A non-coherent matched filter, optimised to the symbol length 'T', has a frequency response which is a sinc function with nulls every $1/T$ Hz. It can be shown that performance is maximised if the tones are spaced orthogonally if the tone spacing, Δf , is [Sklar, 55]:

$$\Delta f = \frac{n}{T}, \text{ where } n=1, 2, 3, \dots \quad (3-7)$$

Normally, unless very high levels of Doppler spread are anticipated, ' $n=1$ ' is chosen to minimise the occupied spectrum (i.e. maximise spectrum efficiency):

$$\Delta f_{\min} = \frac{1}{T} \quad (3-8)$$

MFSK has proven to be particularly suitable for the very robust transmission of data over HF channels at low data rates [Ralphs, 56; Clark, 57] including for disturbed channels (high multipath and Doppler spread) and at low SNRs. For a commensurate data rate a higher order MFSK waveform ($M=16$ or $M=32$ is typical) can significantly outperform 2-FSK. The long symbol durations in MFSK are able to protect against the effect of inter-symbol interference (as caused by multipath).

3.2.4 Phase Shift Keying (PSK)

In phase shift keying (PSK) information is transmitted using a constant amplitude carrier, modulating its phase according to the symbols to be transmitted. In binary PSK (BPSK) the phase change is 180° (Figure 3-6b). In an AWGN channel coherent detection offers the maximum performance. In practical systems, particularly those working over disturbed channels it is difficult to establish the required phase reference. In this case differential PSK (DPSK) can be utilised. For DBPSK the phase is unaltered if the next symbol is a '0' and reversed if the next symbol is a '1'. In this case the phase reference for each symbol is the previous one (Figure 3-6c). Whilst this is easier to implement, errors tend to come in pairs, and its performance is ~ 3 dB worse than coherent BPSK. An alternative approach, which is commonly applied in modern HF waveforms which seek to maximise performance, is to take additional measures to equalise the effects of the channel making coherent detection possible. The equalisation of received signals is discussed in greater detail in section 3.2.8.

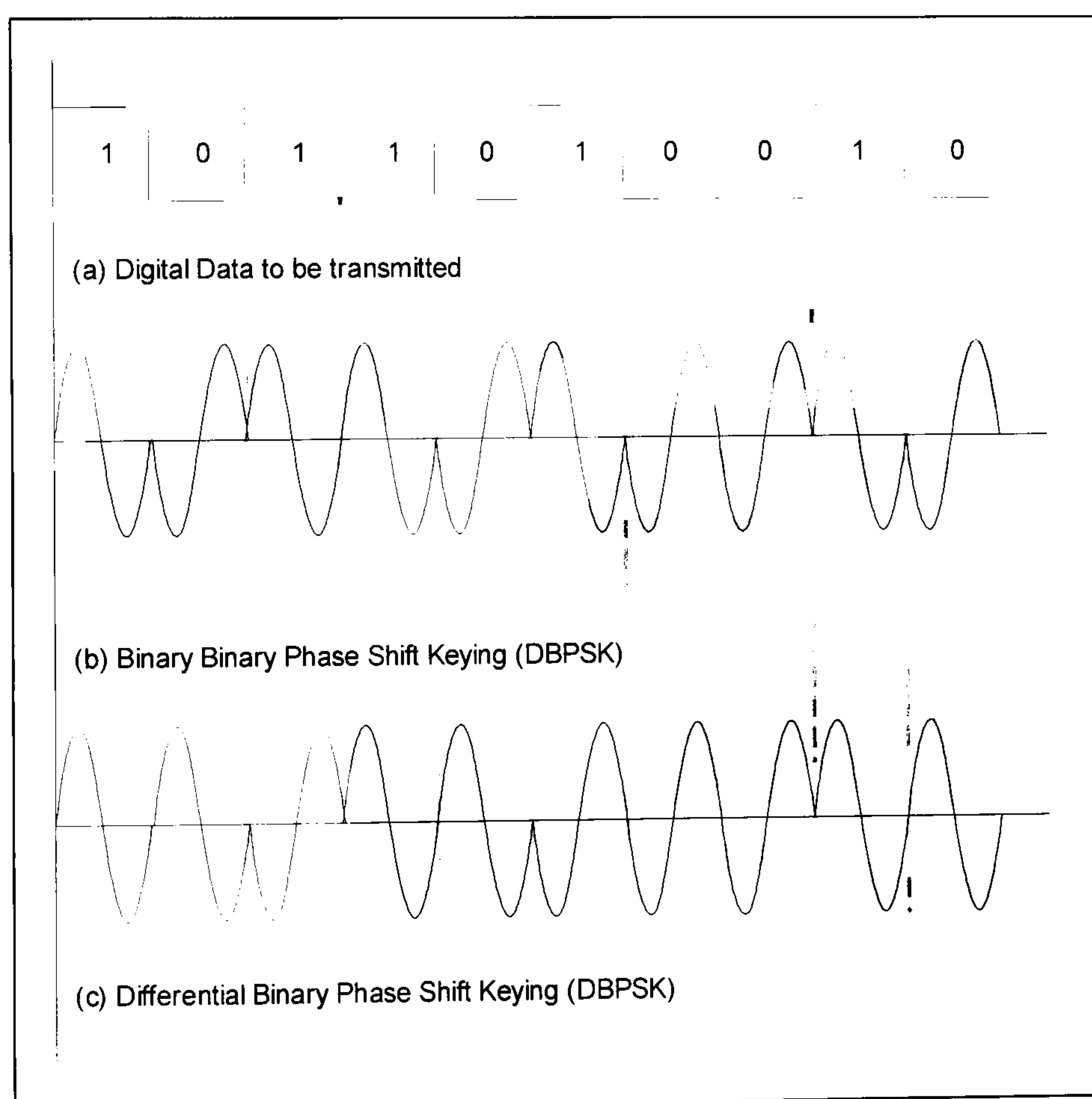


Figure 3-6 Binary Phase Shift Keying (BPSK)

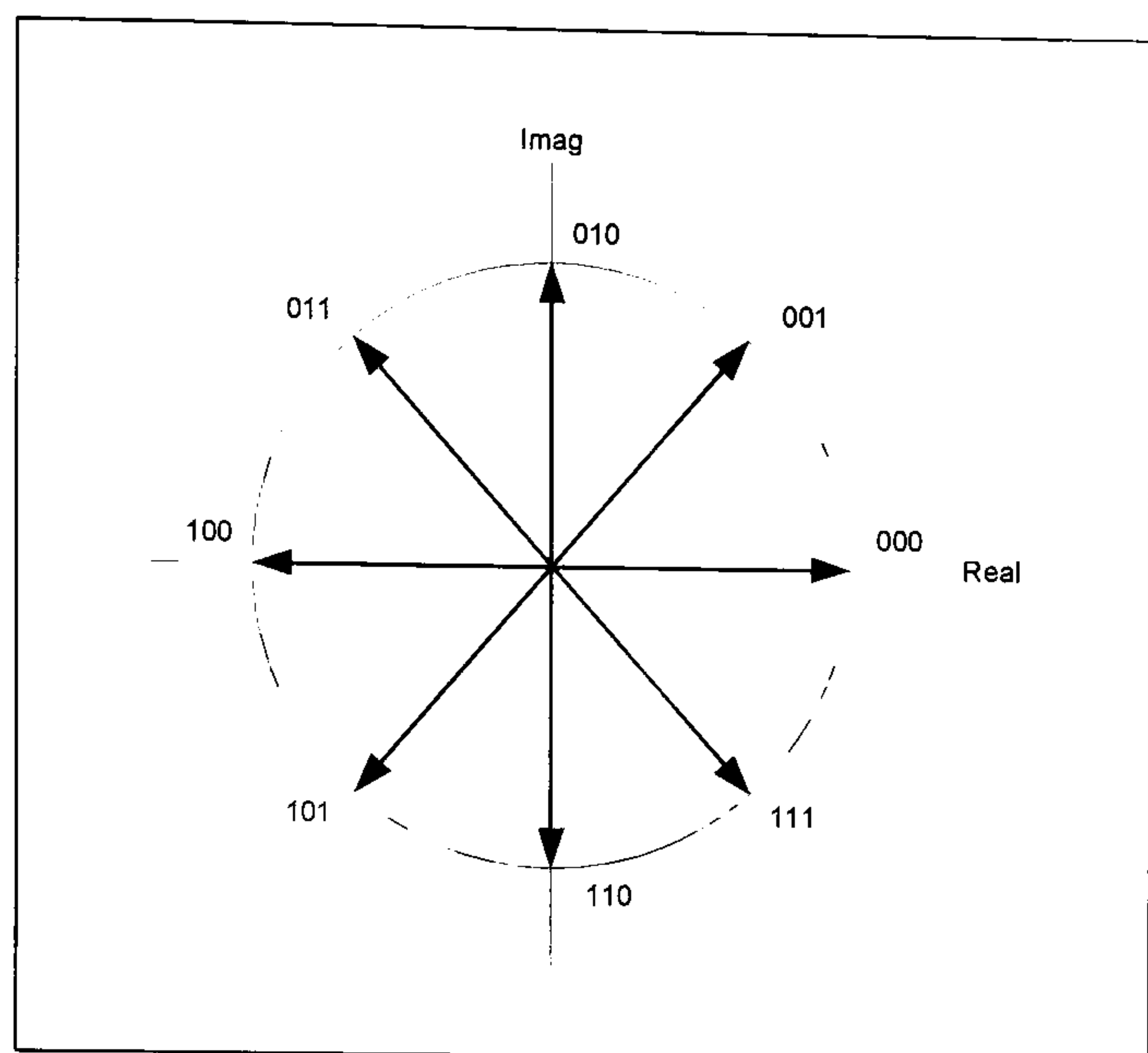


Figure 3-7 8-PSK Constellation

Multi-phase PSK (M-PSK) encodes a number of data bits to be transmitted into a symbol which maps to a particular phase. For example, in 8-PSK three information bits map to a single symbol (Figure 3-7). This increases the throughput (spectral efficiency) at some cost in the required E_b/N_0 to maintain a given BER (as the distance between constellation points is reduced). 4-PSK or quadrature PSK (QPSK) is a special case in that the distance between symbols in the constellation is the same as for BPSK and so, theoretically the performance is the same. A common method of implementing a QPSK modulator is illustrated in Figure 3-8. Practical M-PSK waveforms for use at HF require the use of equalisation to provide acceptable performance.

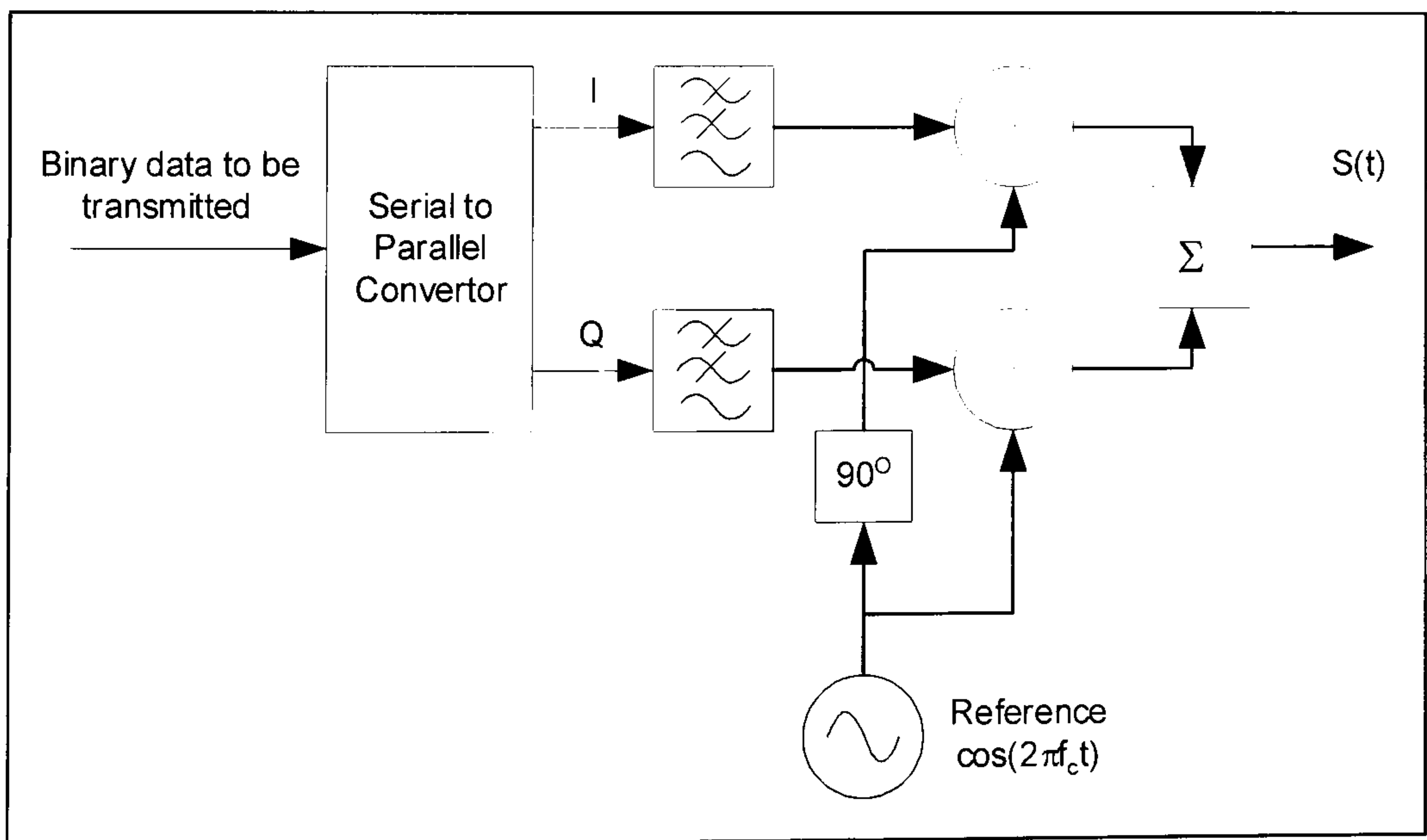


Figure 3-8 QPSK/QAM Modulator

3.2.5 Higher Order Modulation - Quadrature Amplitude Modulation (QAM)

Where higher spectral efficiencies are required, combined phase and amplitude modulation can be employed, effectively still modulating a single carrier. In quadrature amplitude modulation (QAM) a series of binary digits to be transmitted is mapped to a symbol which represents a phase/amplitude combination. 16-QAM (Figure 3-9) has a theoretical 4 bps/Hz spectral efficiency although this is reduced in practical implementations by the inclusion of error correction codes and synchronisation/training data (discussed later).

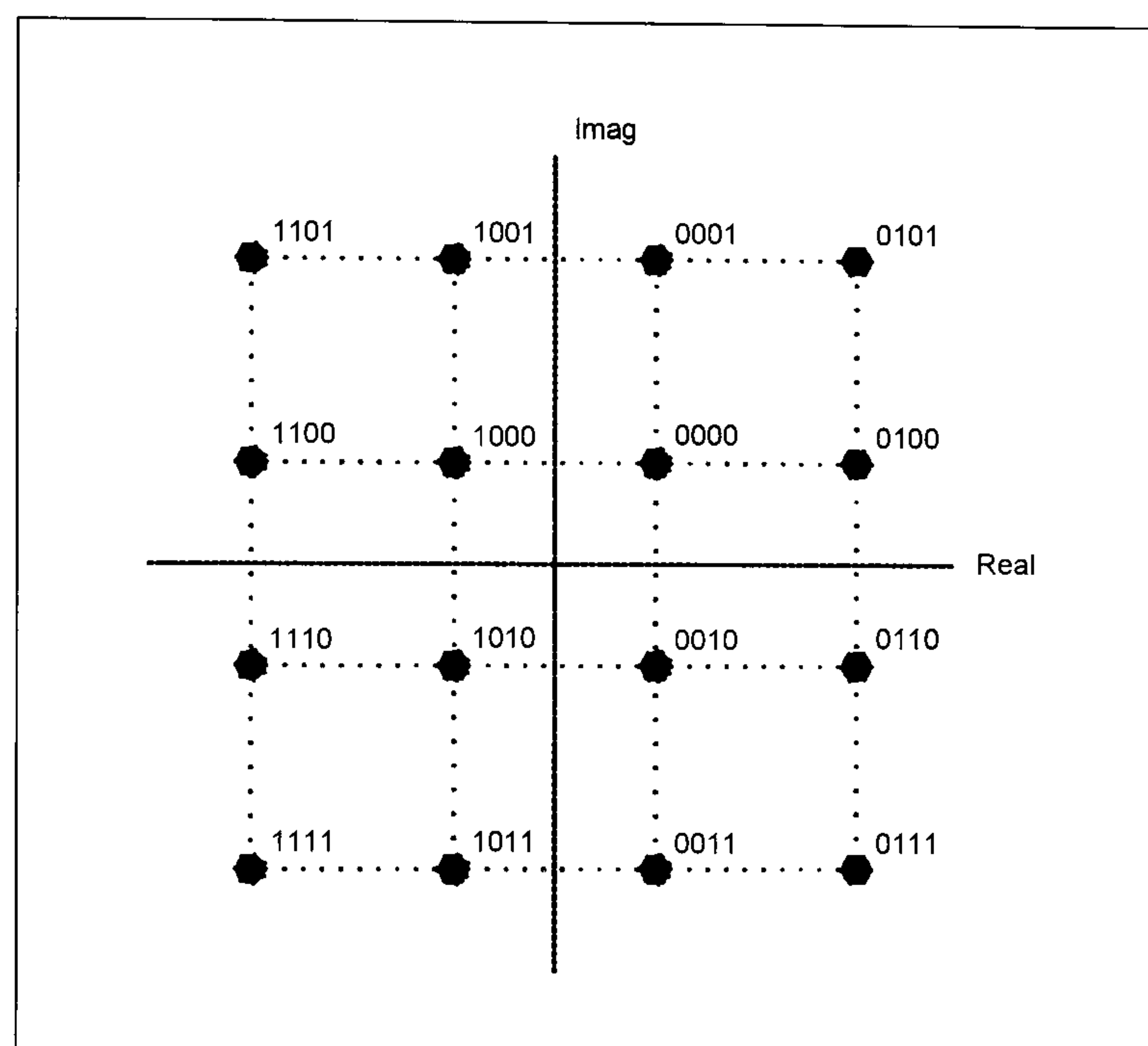


Figure 3-9 16-QAM Constellation

The application of modulation schemes, such as QAM to HF is still relatively new and requires the use of sophisticated receiver implementations to mitigate the effects of the HF channel (including adaptive equalisation, effective error control coding). Even so, the application, particularly of higher order QAM schemes, is limited to relatively benign channels with good SNR.

3.2.6 Higher Order Modulation – Multi-Carrier Techniques

An alternative approach to using single tone waveforms (such as QAM) to provide high spectral efficiencies is to modulate a series of carriers. Most modern multi-carrier waveforms are implemented as orthogonal frequency division multiplexing (OFDM).

The modulation applied to each carrier varies from simple schemes such as DBPSK (e.g. Kiniplex, [Mosier, 58]) to using multi-level schemes like QAM (e.g. Digital Radio Modiale MF/HF broadcasting, [Stott, 50]). A particular advantage of OFDM is that it may be efficiently implemented using Fast Fourier Transform (FFT) filter banks as the core components of both modulator and demodulator. The implementation of OFDM provides an inherent tolerance to multipath as the symbol rate on each carrier is very low. However, additional measures do have to be taken. In particular a guard period (in effect a lengthening of the symbol period) has to be applied to reduce the inter-symbol caused by multipath. In order to allow coherent demodulation known pilot tones and pilot symbols are inserted to allow the impact of the channel to be identified and mitigated. Other techniques such as interleaving are utilised to mitigate against frequency selective fading and narrowband interference. These issues are well described in [Burr, 51].

The construction of the transmitted signals from a series of independently modulated carriers results in the transmitted signal having a significant peak-to-mean amplitude ratio (PAR). This is because at some instances the outputs of the individual modulators will add coherently). Where, as is often the case at HF, system performance is limited by SNR, transmitter power is a key factor. In a practical system it is not untypical for the transmitter to have to be backed off by ≥ 10 dB to avoid saturation at peak powers. This issue is not always reflected in comparative waveform performance comparisons. A number of techniques have been developed to reduce the impact of the PAR including semi-orthogonal symbol mapping [Shepherd, 59] and adaptive clipping which takes advantage of the fact that the severest excursions rarely occur [Enright, 60].

3.2.7 Relative Performance of Modulation Schemes

The relative performance of many of the modulation schemes discussed can be compared in the AWGN BER performance plots presented in Figure 3-10 (based on analysis from [Burr, 51], [Proakis, 14] and [Stremmler, 61]). A number of additional observations are appropriate:

- The performance plotted is for an AWGN channel. Performance in fading HF channels will be poorer and, in the case of PSK and QAM at least, require equalisation.

- Higher order MFSK modulation provides improved robustness (i.e. lower E_b/N_0 operation) at the expense of reduced spectral efficiency. Conversely higher order PSK and QAM provide increased spectral efficiency (bps/Hz) at the expense of robustness.
- As would be expected from an inspection of the M-PSK and M-QAM constellations, at $M > 8$ the robustness of QAM starts to exceed that of PSK.

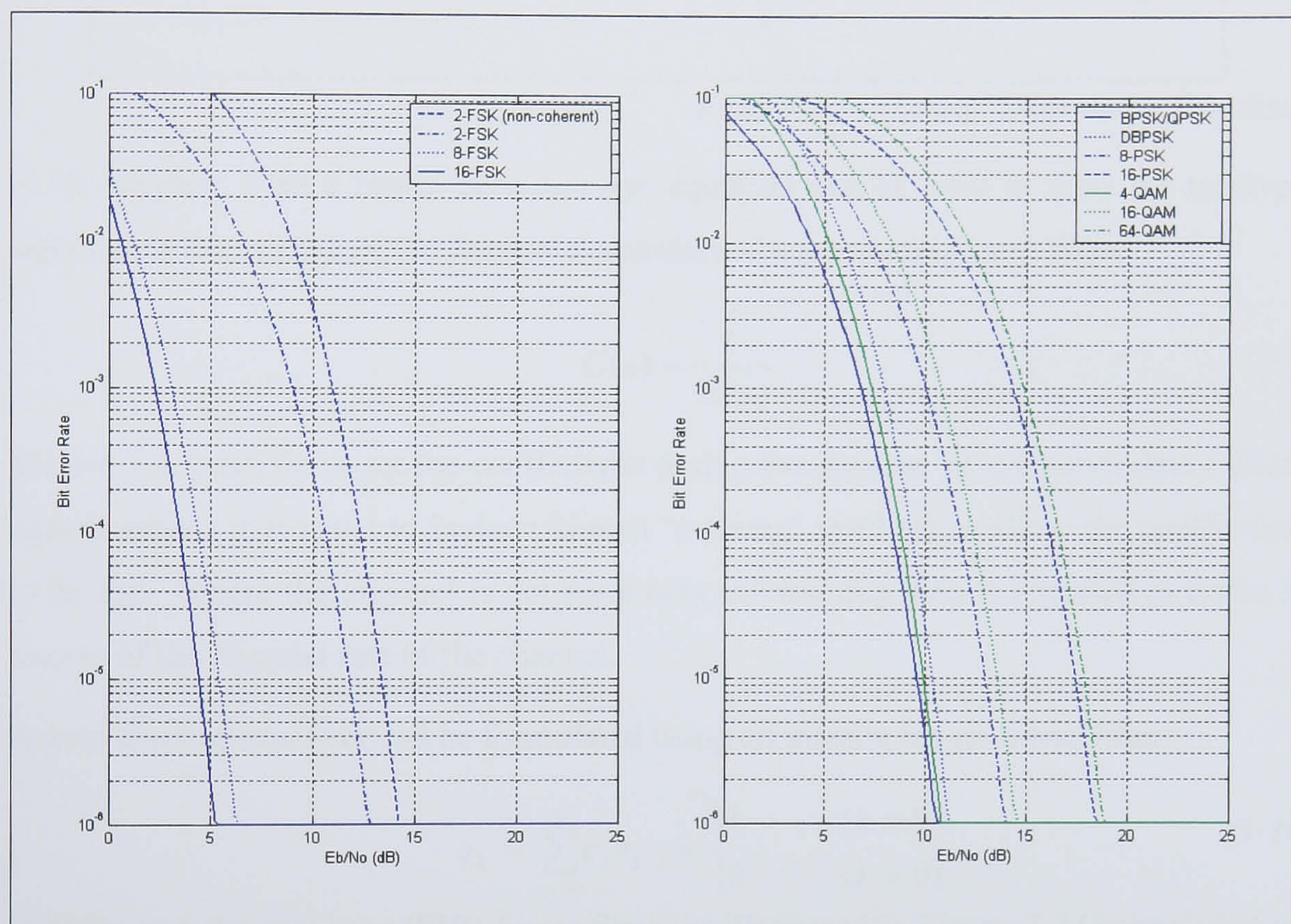


Figure 3-10 BER Performance of Various Modulation Schemes in an AWGN Channel

3.2.8 Adaptive Equalisation to Mitigate Multipath and Doppler Spread

The relative delay between signals arriving at a receiver due to multipath can cause severe ISI, particularly in channels such as HF Skywave where the multipath may span many symbols. For example, the symbol duration in a standardised 3 kHz HF waveform such as MIL-STD-188-110A [US DOD, 62] is $\sim 417 \mu\text{s}$ (2400 symbols/s) compared with the multipath which may be in excess of 5 ms. Further, frequency dispersion (Doppler spread) and distortion introduced by the transmitter/receiver will cause phase and amplitude variations in the received waveform which can adversely effect demodulation. This may be corrected by employing equalisation.

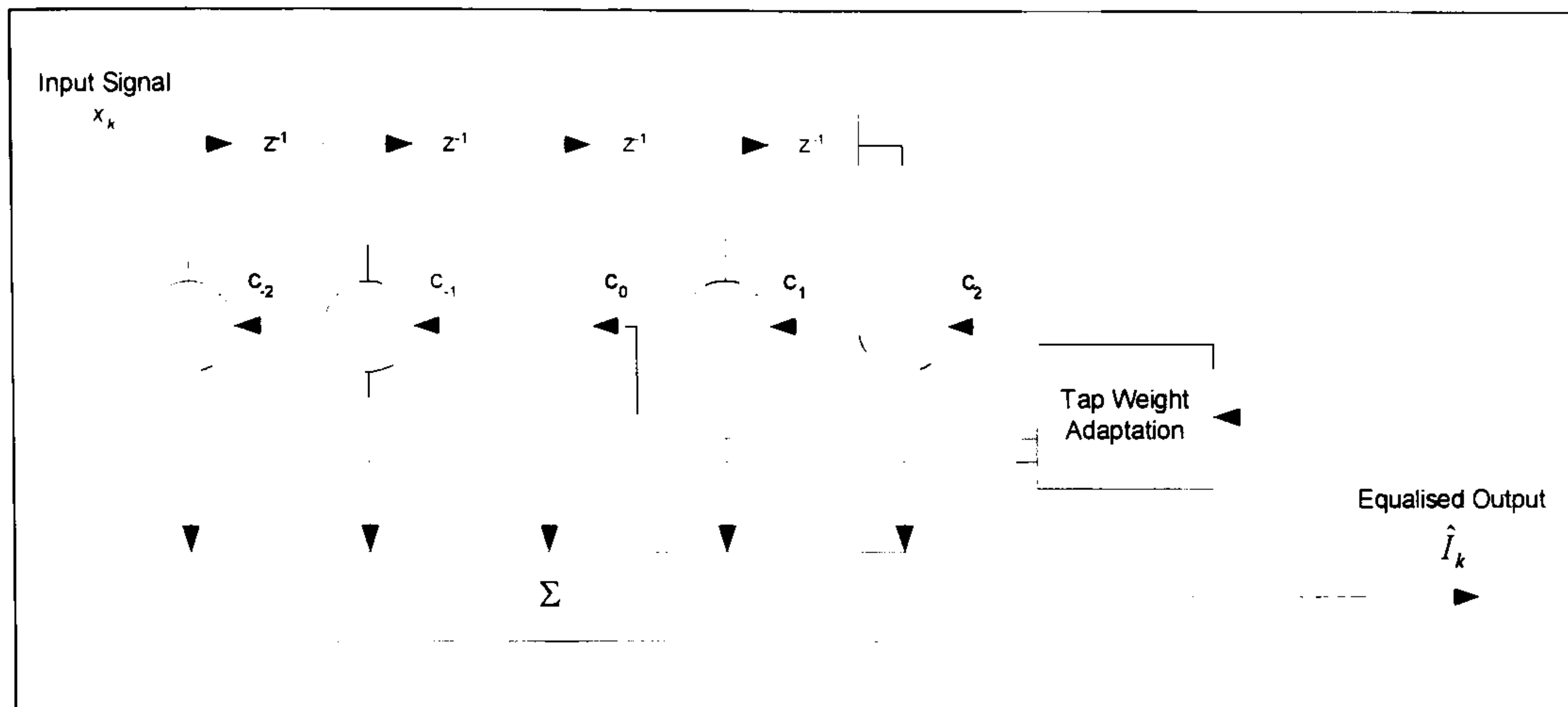


Figure 3-11 Linear Transverse Equaliser

In its simplest form a linear ‘zero forcing’ equaliser can be used to filter the received signal with the inverse of the channel z -transform frequency response, $H(z)$:

$$C(z) = \frac{1}{H(z)} \quad (3-9)$$

Whilst it is possible to set the coefficients during the passage of unknown data (‘*Blind equalisation*’) it is usual to include known ‘*training*’ symbols to allow the coefficients to be set. Where the channel is not stationary the training data is repeated at a rate in excess of the Nyquist rate of the channel.

A zero forcing equaliser can be formulated using an infinite length linear filter:

$$q_k = \sum_{j=-\infty}^{\infty} c_j v_{k-j} = \begin{cases} 1 & (k = 0) \\ 0 & (k \neq 0) \end{cases} \quad (3-10)$$

A finite impulse response (FIR) linear filter (as illustrated in Figure 3-11) approximates this:

$$\hat{I}_k = \sum_{j=-K}^K c_j v_{k-j} \quad (3-11)$$

However, such an equaliser’s performance is sub-optimal [Proakis, 14]. In particular the performance of such a linear equaliser is very poor in the presence of fading when the filter can significantly amplify noise in the absence of a real signal. Indeed, to ensure stability, a noise-whitening filter whose impulse response is the conjugate of the equaliser filter is sometimes employed.

A better approach than the zero-forcing criteria is to minimise the mean square error (MSE), between the symbol transmitted, I_k , and that detected, \hat{I}_k .

A more advanced equaliser is the non-linear decision feedback equaliser (DFE), illustrated in Figure 3-12. The feed forward section is the same as for the linear equaliser described above. However, a feedback filter is added whose input is previously detected symbols. Functionally its aim is to remove from the present estimate that part of the ISI caused by previously detected symbols.

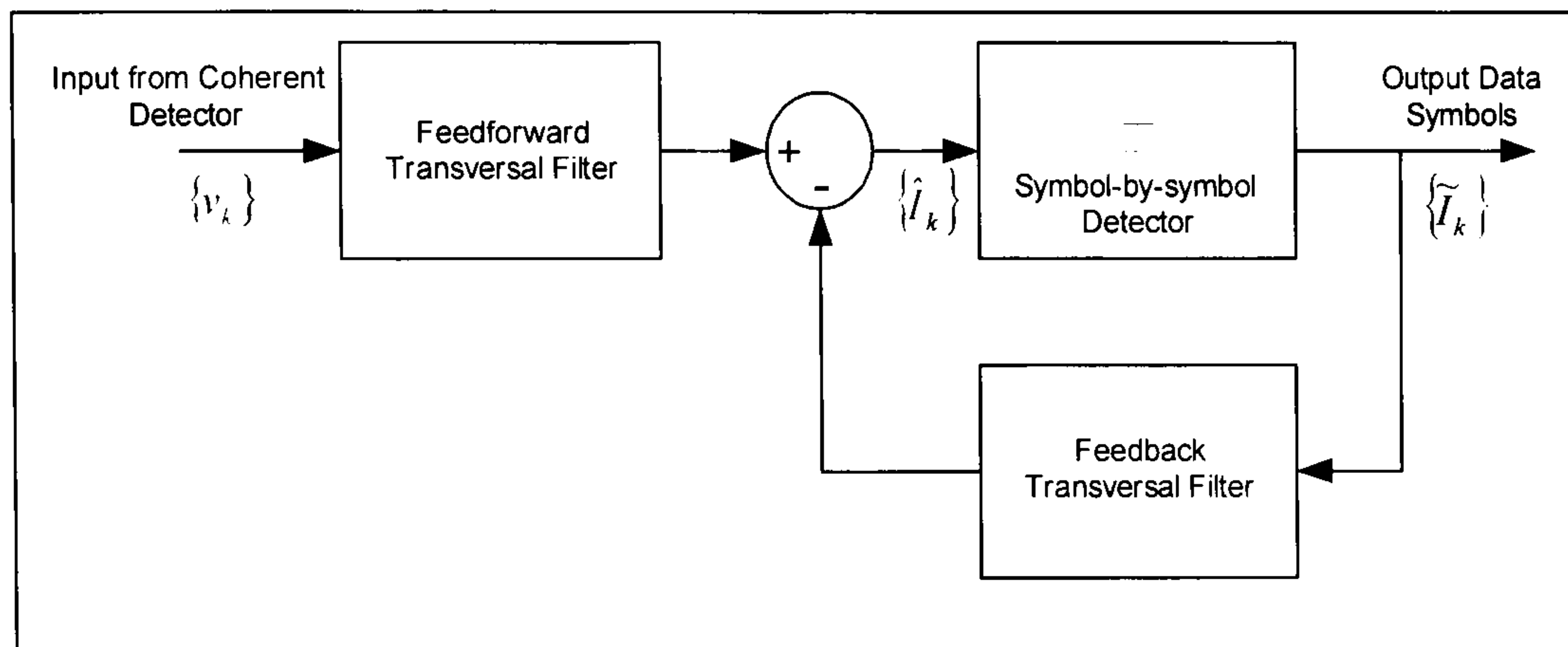


Figure 3-12 Decision Feedback Equaliser (DFE)

In this case the equaliser output can be expressed as:

$$\hat{I}_k = \sum_{j=-K_1}^0 c_j v_{k-j} + \sum_{j=1}^{K_2} c_j \tilde{I}_{k-j} \quad (3-12)$$

where

\hat{I}_k is an estimate of the k th symbol as before,

\tilde{I}_k is the k th detected symbol

c_j are the K_1+1 feed forward and K_2 feedback coefficients

Given the requirement to jointly optimise coefficient sets K_1 and K_2 to achieve the MSE criteria:

$$J(K_1, K_2) = E \left| I_k - \hat{I}_k \right|^2 \quad (3-13)$$

the coefficients of the feed forward filter are given by [Proakis, 14]:

$$\sum_{j=-K_1}^0 \psi_{ij} c_j = h_{-i}^*, \quad i = -K_1, \dots, -1, 0 \quad (3-14)$$

where

$$\psi_{ij} = \sum_{m=0}^{-i} h_m^* h_{m+i-j} + N_0 \delta_{ij}, \quad i, j = -K_1, \dots, -1, 0 \quad (3-15)$$

and

$h_0 \dots h_{L-1}$ are the taps of the channel (length L);

N_0 is the channel noise density;

δ_{ij} is the Kronecker delta matrix: $\delta_{ij} = 1$ for $i=j$, $\delta_{ij} = 0$ otherwise.

The coefficients of the feedback filter can be expressed in terms of the coefficients of the feed forward filter:

$$c_k = \sum_{j=-K_1}^{-i} c_j h_{k-j}, \quad k = 1, 2, \dots, K_2 \quad (3-16)$$

The feedback filter is able to completely cancel the ISI from previous symbols providing these have been correctly detected and that the filter length, K_2 , exceeds the channel length (total multipath dispersion).

Since the multipath fading channels, such as Skywave HF, are not stationary practical modem implementations must be able to adapt continually and sufficiently quickly to track the changing channel. Therefore the coefficients must be calculated using computationally affordable, fast converging algorithms such as the Kalman Recursive Least Squares (RLS) algorithm [Hsu, 63].

There are a number of alternative adaptive equaliser structures including the optimum (but computationally expensive) Viterbi maximum likelihood sequence estimation (MLSE) algorithm [Bartlett, 64], [Falconer, 65] and more efficient block decision feedback equalisers (BDFE), discussed in [Jorgenson, 69]. In both cases these algorithms take a block of symbols and treat the detection process as a joint optimisation problem (as opposed to the DFE symbol-by-symbol approach). Further performance improvements can be realised by adapting the equaliser based on FEC corrected symbols.

3.2.9 Forward Error Correction (FEC) Coding

The majority of practical modems make use of FEC to provide acceptable bit error rates. Essentially these all employ the transmission of additional parity bits calculated

from the information bits to be transmitted. This reduces the useful throughput but increases robustness. This section aims to provide a brief introduction to the subject and indicate the general performance that can be obtained. Error control coding is a large subject and for detailed information in this evolving field the reader is urged to consult one of the large numbers of texts on the subject (e.g. [Lin, 70]).

A code word of ' n ' bits is formed from ' k ' information bits and $n-k$ parity bits. The code rate, i.e. the proportion of information bits in a code word and therefore its efficiency, is k/n . The number of bit errors in a code word that can be corrected is essentially determined by the 'distance' between possible code words and is clearly related to the code rate. The principal classes of FEC can be broadly categorised as 'block' codes (e.g. Reed Solomon codes, Bose-Chaudhuri-Hocquenghem codes) and 'convolutional' codes. Different codes have different properties. For example Reed-Solomon codes have an ability to correct small bursts of errors whereas convolutional codes that have poor burst errors have a much greater capability to correct independent (random) errors. A FEC code may either be utilised alone or, where additional robustness is required, codes may be concatenated (thus potentially harnessing the benefits of different codes).

The decoding process may be either '*hard decision*', where decoding is based on symbol decisions made in the demodulator, or, on '*soft decisions*', where the demodulator provides the decoder with a numeric confidence for all its decisions. This additional information can be put to good use to determine a maximum likelihood decoding. This is now commonly done by forming a time series graph of all possible received symbol combinations in a code block (a trellis) and then using the Viterbi algorithm to determine the most likely sequence of originally transmitted symbols.

Recently, a new class of codes, the so-called '*Turbo codes*' have been discovered [Berrou, 53]. These are constructed as concatenated component codes interspersed with interleavers. By utilising iterative, soft decoding employing a 'soft input-soft output' (SISO) decoder performance approaching to within a fraction of dB of the Shannon bound is possible with sufficient iterations.

The performance curves for a number of different FEC schemes, operating in AWGN, are presented in Figure 3-13 [Proakis, 14], [Burr, 51].

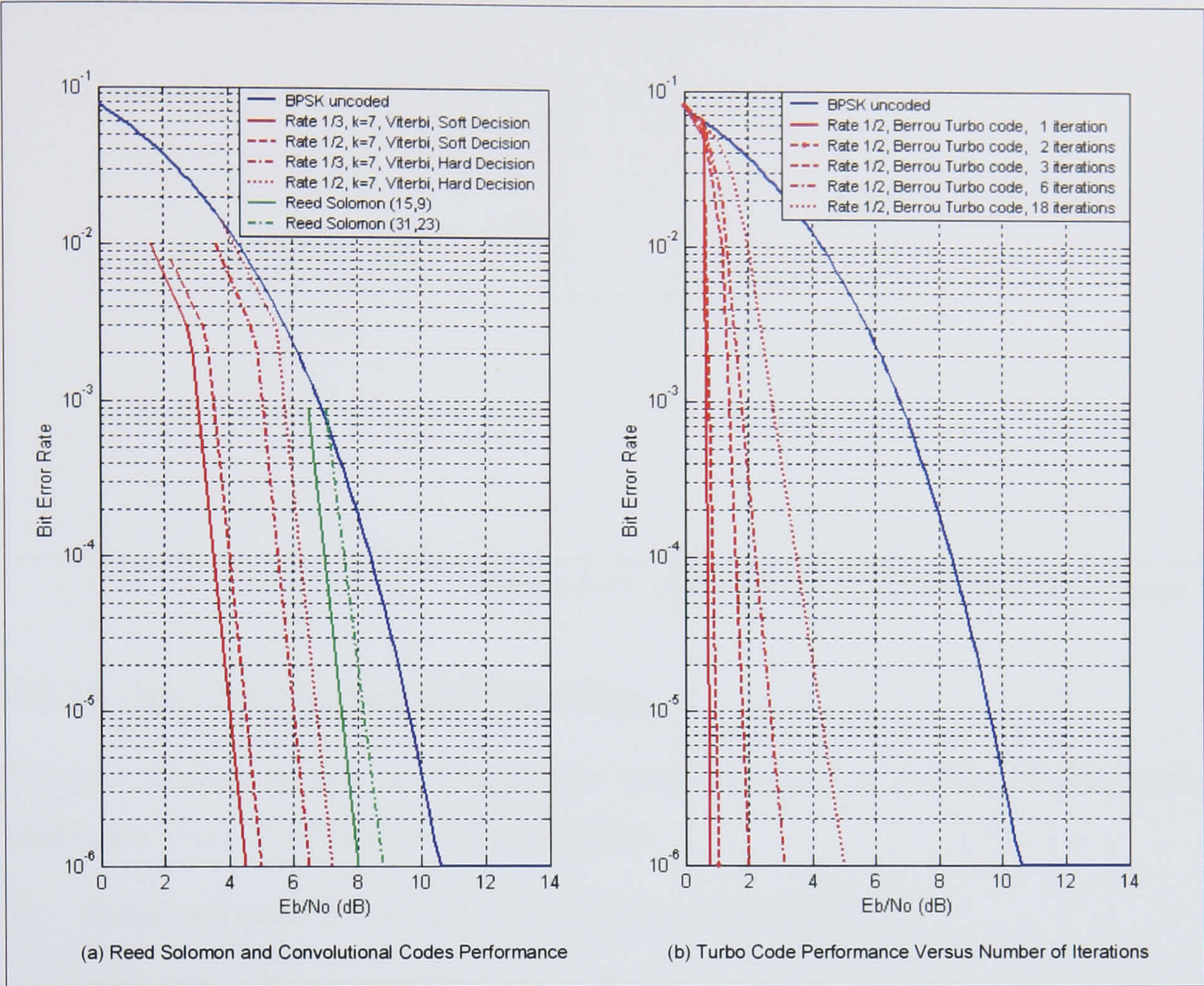


Figure 3-13 Performance of Various Forward Error Correction Codes

3.2.10 Interleaving

Practical FEC codes, whilst powerful for correcting information streams containing statistically independent (random) errors, have a poor ability to correct large bursts of errors such as might occur on a slowly fading channel. Interleaving is a process of scrambling the order of the symbols to be transmitted typically using a block (illustrated in Figure 3-14) or convolutional interleaver [Proakis, 14]. The interleaver ‘depth’ is chosen to allow it to overcome the expected fade duration; for HF this may be several seconds. Following de-interleaving at the receiver, a burst of errors becomes a number of random errors which the FEC can hopefully correct. The act of multiplexing a coded data stream onto a number of carriers for a parallel tone waveform inherently provides some protection from frequency selective fading and narrowband interference. However, an interleaver will still generally be used to overcome flat fading.

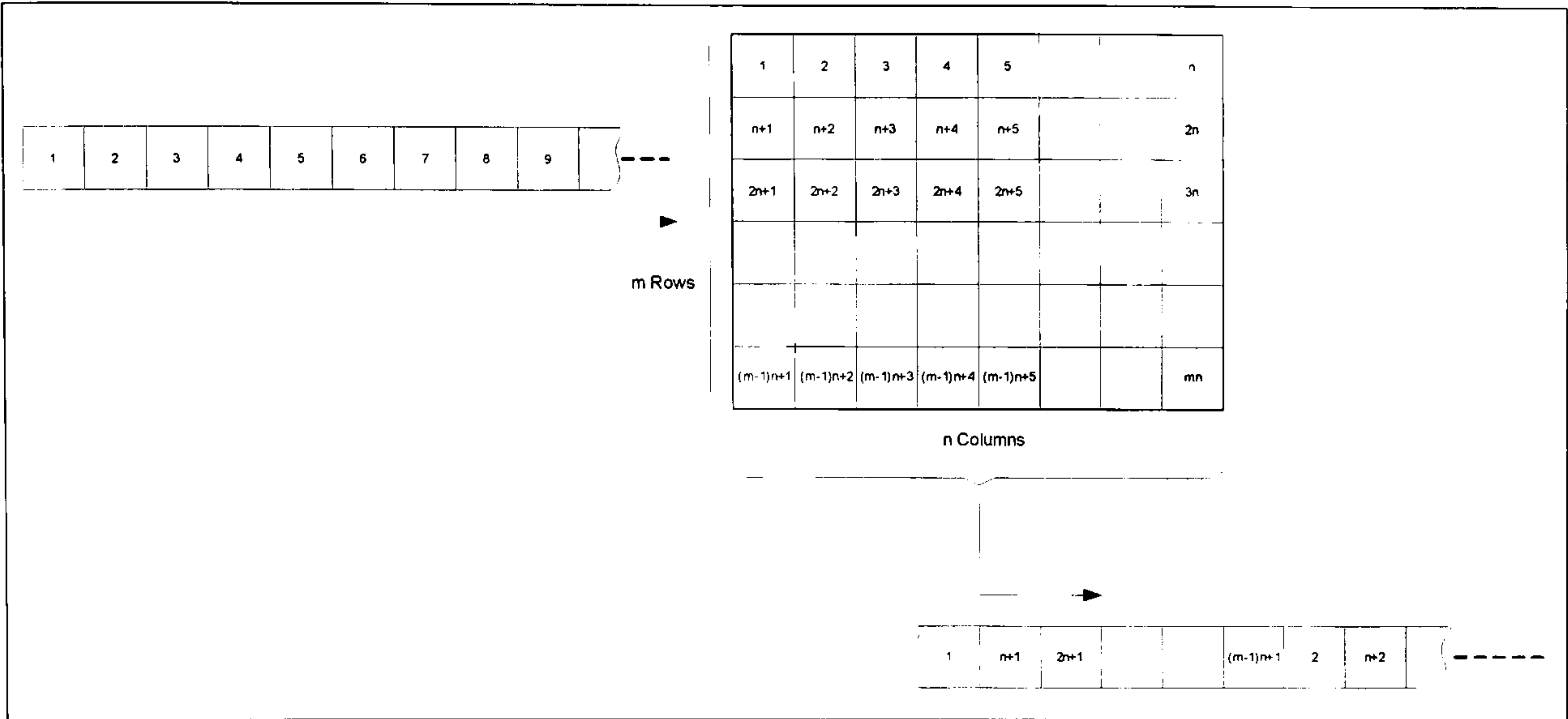


Figure 3-14 Operation of an $(m \times n)$ Block Interleaver

3.2.11 Synchronisation and Tracking

Practical modem receive implementations must overcome a number of additional challenges. Specifically, they need to be able to:

- Detect and acquire a transmission (initial synchronisation);
- Determine and correct for Doppler shift on the transmission; and
- Continue to track the signal being received correcting for Doppler shift and modem clock drift.

3.3 MIL-STD-188-110A - a Serial Tone HF Data Communications Waveform

This section concludes the discussion of modem techniques by introducing a modern HF waveform employing many of features discussed. MIL-STD-188-110A (MS-110A, [US DOD, 62]) is a serial tone waveform providing throughputs of 300 to 2400 bps with FEC and 4800 bps un-coded. There is also a highly robust 75 bps mode based on in-band spread spectrum. MS-110A is based on the use of convolutional coding, interleaving and adaptively equalised 8-PSK modulation format. The structure of the waveform is illustrated in Figure 3-15.

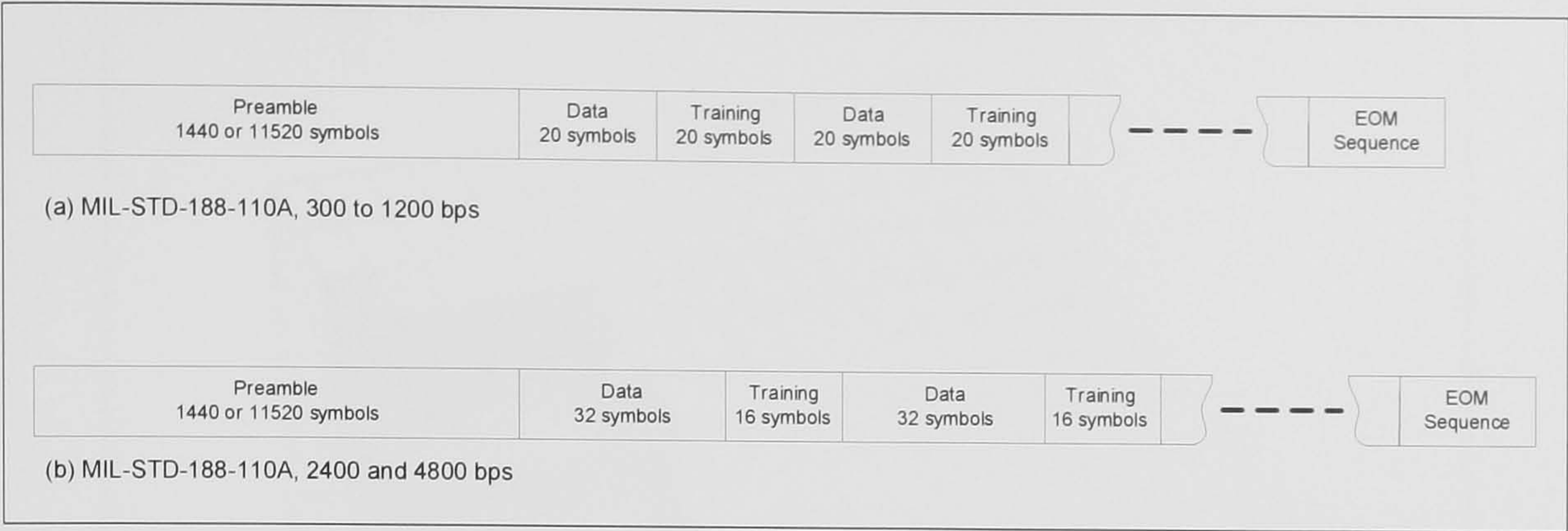


Figure 3-15 Structure of MIL-STD-188-110A waveform

At all data rates the modem transmits at 2400 symbol/s in a bandwidth of 2.7 kHz. At data rates up to 1200 bps the training phase is 8.3 ms long and repeated at a rate of 60 probes/s. These numbers indicate the modem’s ability to tolerate multipath and Doppler spread respectively [Brakemeier, 71].

The waveform FEC depends on data rate (see Table 3-1). It utilises a matrix block interleaver with three depths: zero (bypassed), short (0.6 s) and long (4.8 s). It also supports auto-baud; the ability for the receiver to automatically identify the data rate and interleaver settings of a transmission from information in the pre-amble.

Data Rate	Bits Per 8-PSK Symbol	Effective Code Rate	FEC
150	1	$\frac{1}{8}$	Convolutional Code, Rate $\frac{1}{2}$, k=7, repeated 4 times
300	1	$\frac{1}{4}$	Convolutional Code, Rate $\frac{1}{2}$, k=7, repeated 2 times
600	1	$\frac{1}{2}$	Convolutional Code, Rate $\frac{1}{2}$, k=7
1200	2	$\frac{1}{2}$	Convolutional Code, Rate $\frac{1}{2}$, k=7
2400	3	$\frac{1}{2}$	Convolutional Code, Rate $\frac{1}{2}$, k=7
4800	3	1	Un-coded

Table 3-1 Modulation/Coding Parameters for MIL-STD-188-110A

Figure 3-16 shows a constant BER plot [Arthur, 72] of a measured commercial modem’s performance envelope over a range of multipath and Doppler spread conditions for BER=10⁻³. As can be seen the modem essentially operates reliably with ~10 dB SNR to Doppler spreads of ~6 Hz and multipath of ~6 ms. Beyond either of these limits the performance quickly deteriorates. Regions of SNR≥40 dB indicate where the BER requirement could not be met irrespective of the available SNR and indicates the performance limits of the waveform/equaliser.

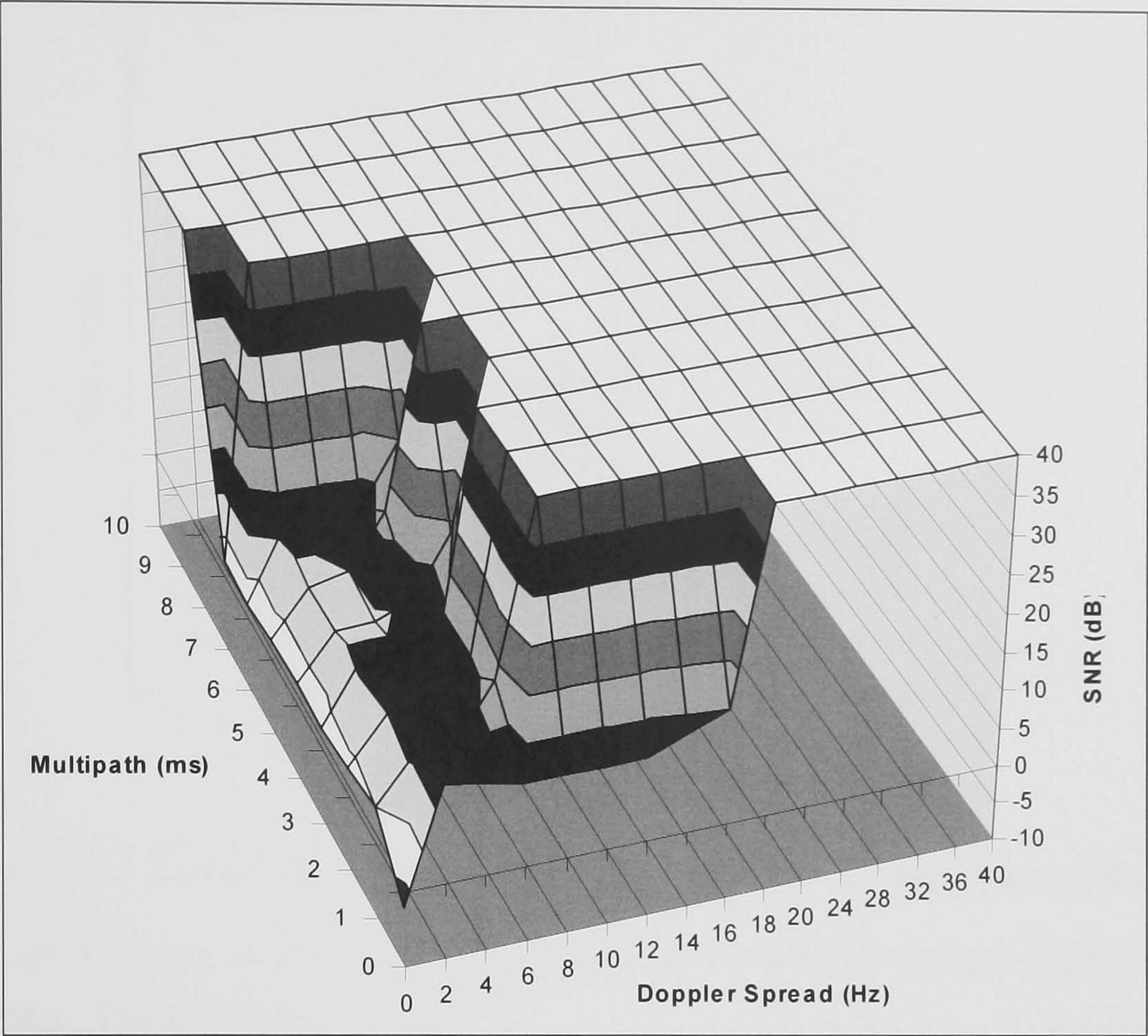


Figure 3-16 Measured Performance of 1200 bps MIL-STD-188-110A Modem (BER=10⁻³)

3.4 High Data Rate HF Communications

Figure 3-17 summarises the current (2001) state of progress that the international HF research community has achieved in developing HF waveforms and modems with increased throughputs (and includes work presented in this thesis). For many years users relied almost wholly on un-coded 75-300 baud FSK waveforms for HF data communications. Only in the last ten years have more capable modems become available supporting Skywave data rates up to 2.4 kbps using sophisticated equalised waveforms and FEC. NATO and the US have recently completed work which has led to the standardisation of modems with data rates of up to 9.6 kbps [NATO, 73]. All of the aforementioned waveforms operate in the standard 3 kHz bandwidth ITU HF allocations.

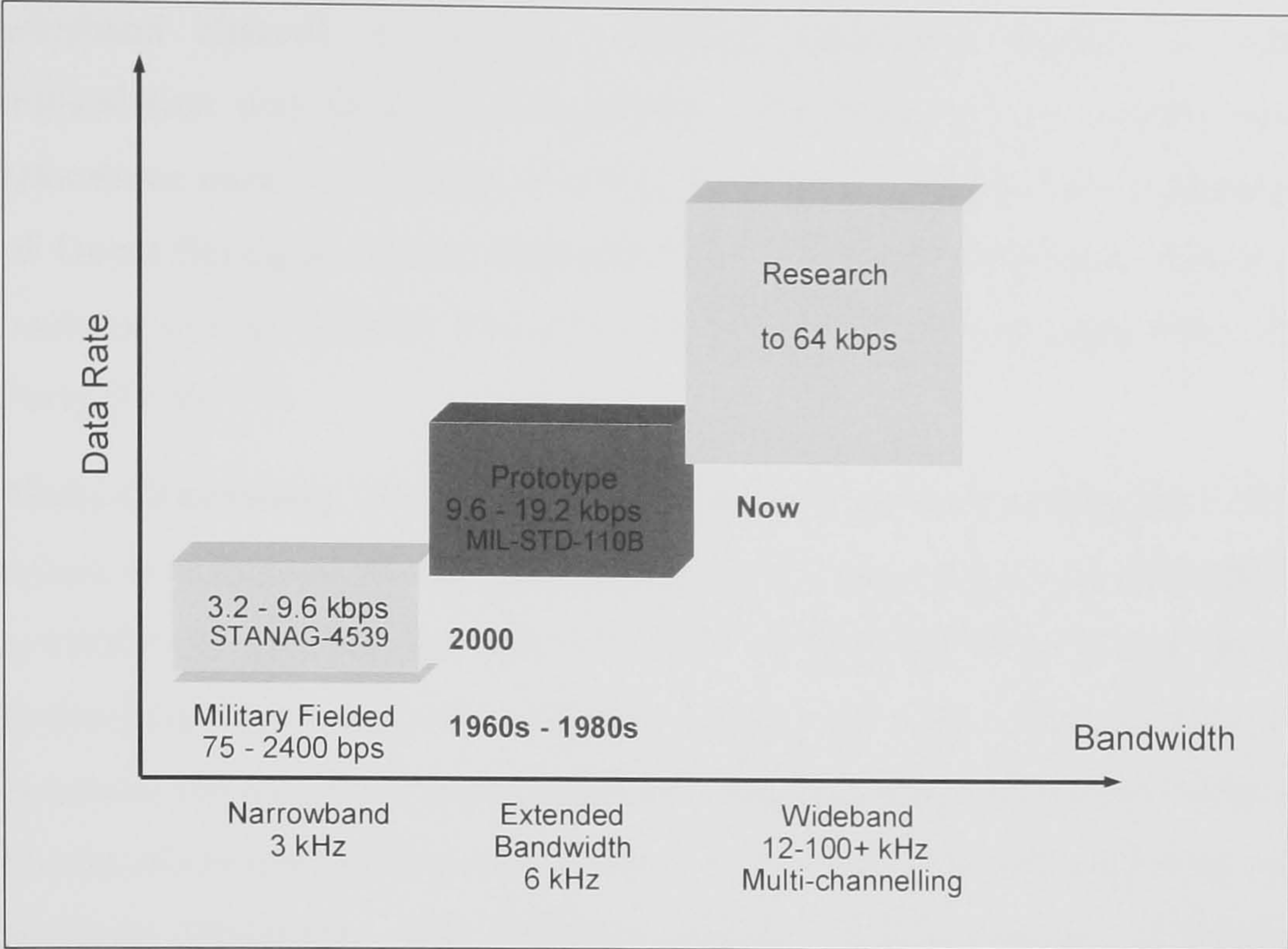


Figure 3-17 Current Progress in Development of HF Data Communications (to 2001)

There are a number of potential technical directions that can be explored to increase HF data rates. These include:

- Waveforms with higher efficiency** – The latest generation of HF waveforms are already highly sophisticated and make extensive use of new and recently developed waveform processing (e.g. DFE and DBFE equalisers) and FEC techniques (e.g. Turbo codes). Whilst there are likely to be further improvements in this area large throughput gains are unlikely to be realised in the near future.
- Diversity Techniques** – Use of spatial, frequency or polarisation diversity is a well known technique to improve robustness and therefore the potential for increased throughput. Recent work has shown that, with the use of space-time coding techniques [Burr, 74], throughput is constrained by the number of uncorrelated transmission paths that are present in the propagation medium. Diversity implementations require the use of multiple antenna apertures as well as multiple transmitter and/or receiver channels.
- Wideband Waveforms** – It may be expected that throughput can be increased in proportion to the contiguous occupied bandwidth [Shannon, 52] given that the waveforms employed are capable of performing adequately in the wideband HF channel. Therefore an improved understanding of the characteristics of the

wideband channel is required. Further, equipment capable of wideband transmission and reception is required. For practical use suitable spectrum allocations must be obtained. Previous work has investigated the implementation of Direct Sequence Spread Spectrum (DSSS) techniques [Dixon, 75] to HF by workers such as Milsom [Milsom, 24], Van der Perre [Van der Perre, 76] and Perry [Perry, 77].

- **Multi-Channelling (use of non-contiguous narrowband channels)** – A related option is to increase throughput by splitting the data stream to be transmitted into a number of parallel channels and then transmitting these over a number of (potentially) non-contiguous channels [Jorgenson, 78]. This aims to provide increased bandwidth through the use of non-contiguous narrowband channels and has the advantage that it is more likely to be practical given the regulatory need for spectrum allocations. This technique, whilst it requires the use of transmission and reception equipment with multiple channels, may potentially utilise existing narrowband modems. However, there is potential for increased efficiency by adaptively exploiting differences and diversity between the narrowband channels in use.

It can be concluded from the above that the principal opportunities for increasing HF data communications rates require the use of wider contiguous bandwidths or multi-channel approaches.

3.5 Summary

This Chapter has introduced some of the key technologies used to implement data communications modem waveforms. Waveforms for narrowband HF data communications have been discussed and some techniques applicable to wideband, high throughput communications introduced. In the next Chapter a new, high throughput (16 kbps), extended bandwidth (6 kHz) modem is introduced. This modem employs many of the techniques introduced here including: robust error correction, interleaving, adaptive equalisation and high order modulation schemes to provide a data rate of 16 kbps over HF channels. In Chapter 7 a new wideband, multi-channel digital transceiver (software radio) capable of supporting wideband and multi-channel operation is presented. One of its intended uses is an experimental software modem platform to develop and experiment with new data transmission techniques.

Chapter 4.

A High Data Rate Modem for Extended Bandwidth Channels

Considerable effort has been expended in recent years to increase data rates over narrow band HF channels as the demand for improved throughput over HF to support a variety of user applications increases. Until recently, state-of-the-art modems, incorporating waveforms such as MIL-STD-188-110A [US DOD, 62] and STANAG 4285 [NATO, 79] have had realistic limits of ~2400 bits per second (bps) over HF sky-wave circuits. With improvements in digital signal processing and modem technology (especially the development of high performance equalisers and improved error control coding techniques) high data rate waveforms, such as those included in the forthcoming MIL-STD-188-110B [US DOD, 2] (formerly specified in Annex G of draft STANAG 5066 [NATO, 81]), are becoming practical. Potential applications include high throughput HF data networking and range extension for line-of-sight V/UHF radio links.

This chapter describes a novel high data rate (HDR), 16 kbps prototype modem operating in an extended bandwidth of 6 kHz¹. The data rate was selected for compatibility with extant line-of-sight radio communications systems and the operating bandwidth chosen to allow conventional independent side-band (ISB) HF radios to be utilised. Results from HF simulator measurements and on-air testing of the modem are presented. The performance limitations of such high data rate modems will be discussed leading to an identification of the range of applications for which they can be expected to be used reliably. Finally a number of alternative extended bandwidth HDR waveforms are introduced and their performance compared with that of the high rate 3 kHz waveforms now being standardised.

¹ The initial concept for these extended bandwidth modem waveforms was the author's. The waveforms implemented are based on a new generation of narrowband waveforms proposed for Annex G of draft STANAG 5066. The implementation of both these 'Annex G' waveforms and the new extended bandwidth variants was undertaken by Bob Johnson and Mark Jorgenson of CRC. The simulator tests, on-air trials work and analysis are all the author's own. This collaboration allowed the work presented in this chapter to be completed in a period of just some 12 weeks.

4.1 Waveform and Modem Processing Description

Two 16 kbps waveform variants were developed and implemented on Pentium PCs running the QNX™ [QNX, 80] real time operating system. An inexpensive sound card was used to provide the audio interface to the radio. The 16 kbps modem waveforms used in this study are developments of the high data rate waveforms specified in Annex G of STANAG 5066. The new waveforms have been designed to exploit the 6 kHz of bandwidth available in some HF channel allocations. Like the Annex G waveforms, they are serial tone waveforms which have been designed to be as efficient as possible to achieve high throughputs

One of the 16 kbps variants uses the 6 kHz channel bandwidth as a contiguous single side-band (SSB) while the other has been designed for use with ISB radios and operates in an independent upper/lower side-band configuration. The only significant difference between the two implementations is in the final modulation stage. The 6 kHz SSB implementation uses a single 3300 Hz sub-carrier modulated at 4800 symbols/s while the ISB implementation employs a modulation rate of 2400 symbols/s which is applied to two ISB sub-carriers, each centred at 1800 Hz within their respective audio side-bands. The ISB implementation takes the data stream at the output of the interleaver (or codec if no interleaver is employed) and alternately passes bits to 16-QAM symbol generators for each of the sub-carriers.

The frame structure used by both the SSB and ISB waveforms is shown Figure 4-1. An initial 240 symbol preamble is followed by 48 blocks of alternating data and known symbols. Each data block, consisting of 282 16-QAM data symbols, is followed by a mini-probe consisting of 31 symbols of known data. After 48 blocks, a 204 symbol subset of the initial preamble is reinserted to facilitate late acquisition ('sync-on-data'), Doppler shift removal and sync adjustment.

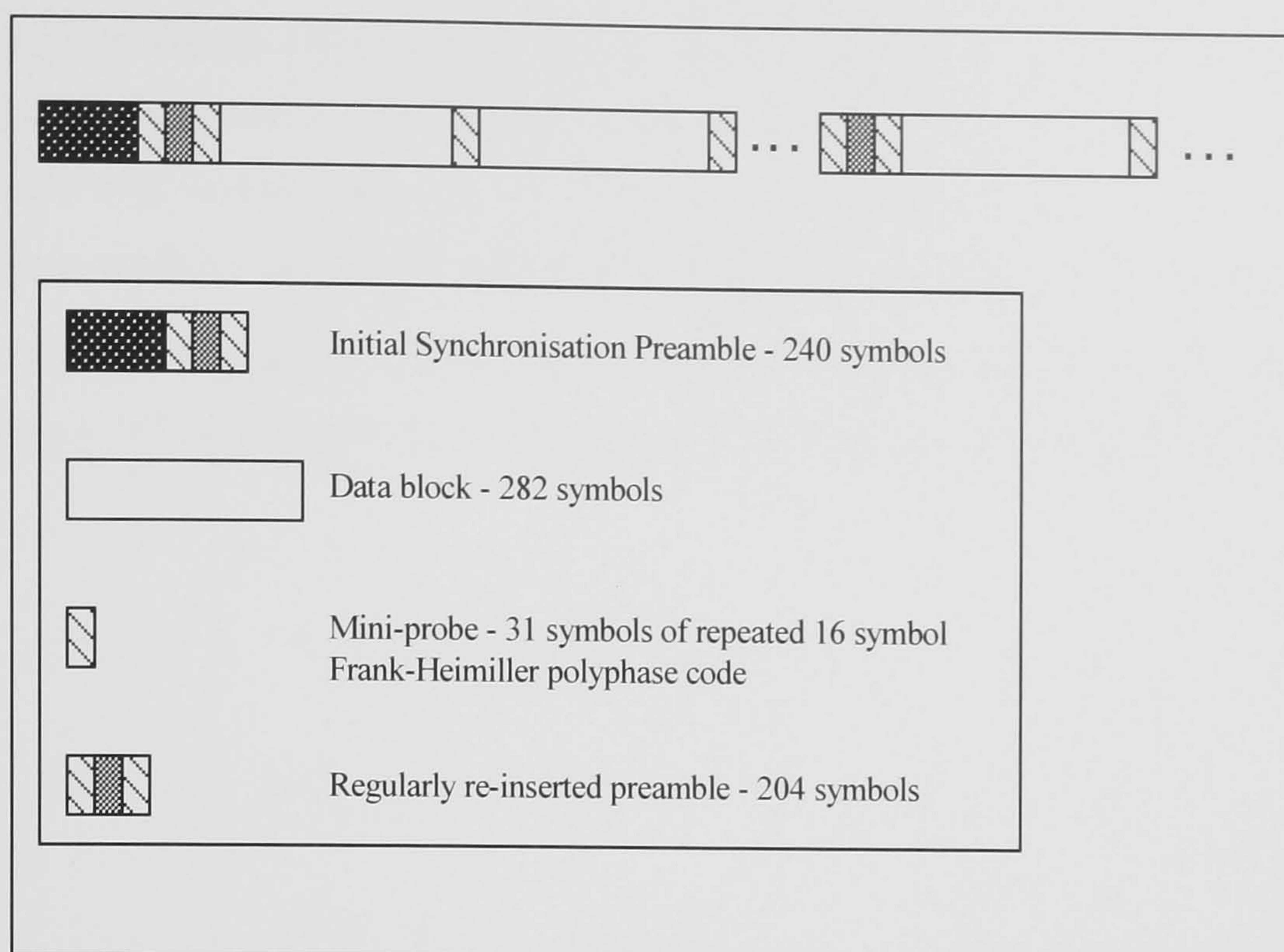


Figure 4-1 16 kbps Modem Waveform Structure

The data blocks, using the 16-QAM constellation points shown in Figure 4-2, are very long to provide the efficiency required for high data rates. The 16-QAM constellation used has been designed to provide a good peak-to-average ratio while retaining the good Gray-coding properties of the traditional square 16-QAM constellation.

The probe segments, which follow each of the data blocks, consist of known symbol sequences ([Frank, 66], [Heimiller, 67], [Frank, 68]) chosen for their good correlation properties, and are long enough that they can be used to derive channel estimates independent of the user data. The forward error correction coding employed, termed a hyper-code (HC), is a proprietary, high rate, iterated block-code which offers performance comparable to that obtained with turbo-codes. An alternative version using the rate $\frac{1}{2}$ constraint length 7 convolutional codec employed in STANAG 4285, punctured to rate 15/16, has also been investigated, but offers poorer performance than that obtained with the proprietary code. In both cases, a convolutional interleaver with selectable delays of approximately 0.1s (short) or 6.5 s (long) can be employed. Alternatively, a no interleaving option is also available.

As a consequence of the common waveform structure used in both implementations, the ISB variant offers roughly twice the delay spread handling capability of the SSB variant while providing approximately half the Doppler spread resistance. This occurs as a result of 2400 baud versus 4800 baud on-air signalling rates. With this waveform, the

ISB implementation offers a delay spread handling capability of the order of slightly more than 5 ms, which is comparable with most current serial tone implementations. Alternate SSB waveforms could be designed which would increase the delay spread handling capability of the SSB variant while reducing its Doppler spread tolerance.

The modem incorporates an advanced adaptive equaliser developed by Jorgenson [Jorgenson, 69] to compensate for multipath and fading imparted by the HF channel.

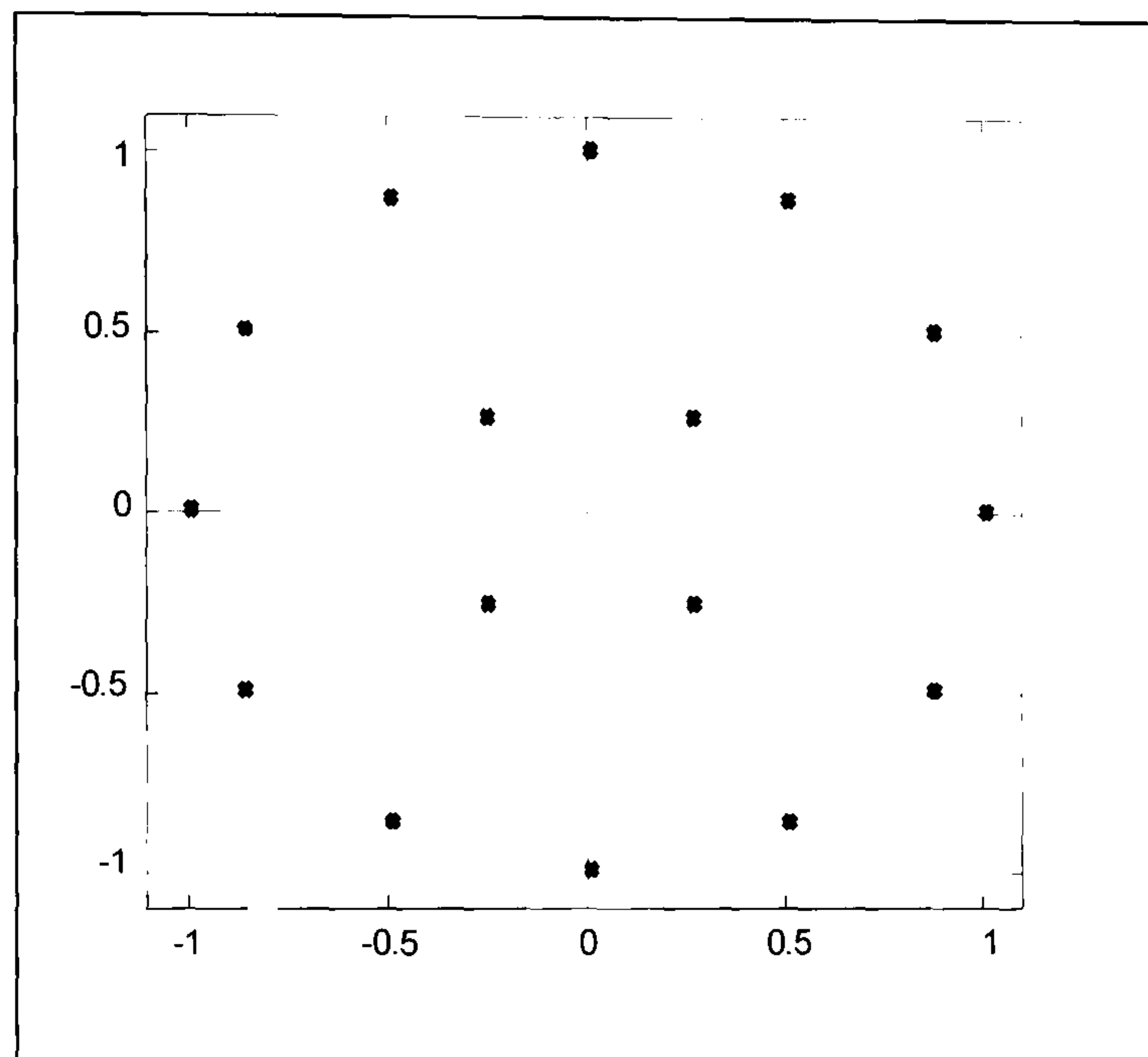


Figure 4-2 *Modified 16-QAM Constellation Employed in the 16 kbps Modem*

4.2 16 kbps Modem Performance

4.2.1 Performance Characterisation using an HF Simulator

The performance of the 16 kbps modem was characterised using a validated Watterson type HF simulator as described in ITU-R F.1487 [ITU, 13] and [Willink et al, 82] operating at baseband. A special modem test mode was used in which a known data sequence was generated in the transmitting modem and the resulting BER calculated at the receiving modem. The simulator used had a maximum input bandwidth of 6 kHz which made it suitable for testing the SSB modem variant. For reasons of practicality the ISB modem was tested using two independent simulators with the same path parameters set on each. The Gaussian fading and noise applied to each sideband was therefore the same but uncorrelated in time. Software was written by the author (in the C language) to control both the simulator and the modem in order to automatically

characterise the modem BER over a wide range of SNR, Doppler spread and multipath conditions using the test set up shown in Figure 4-3.

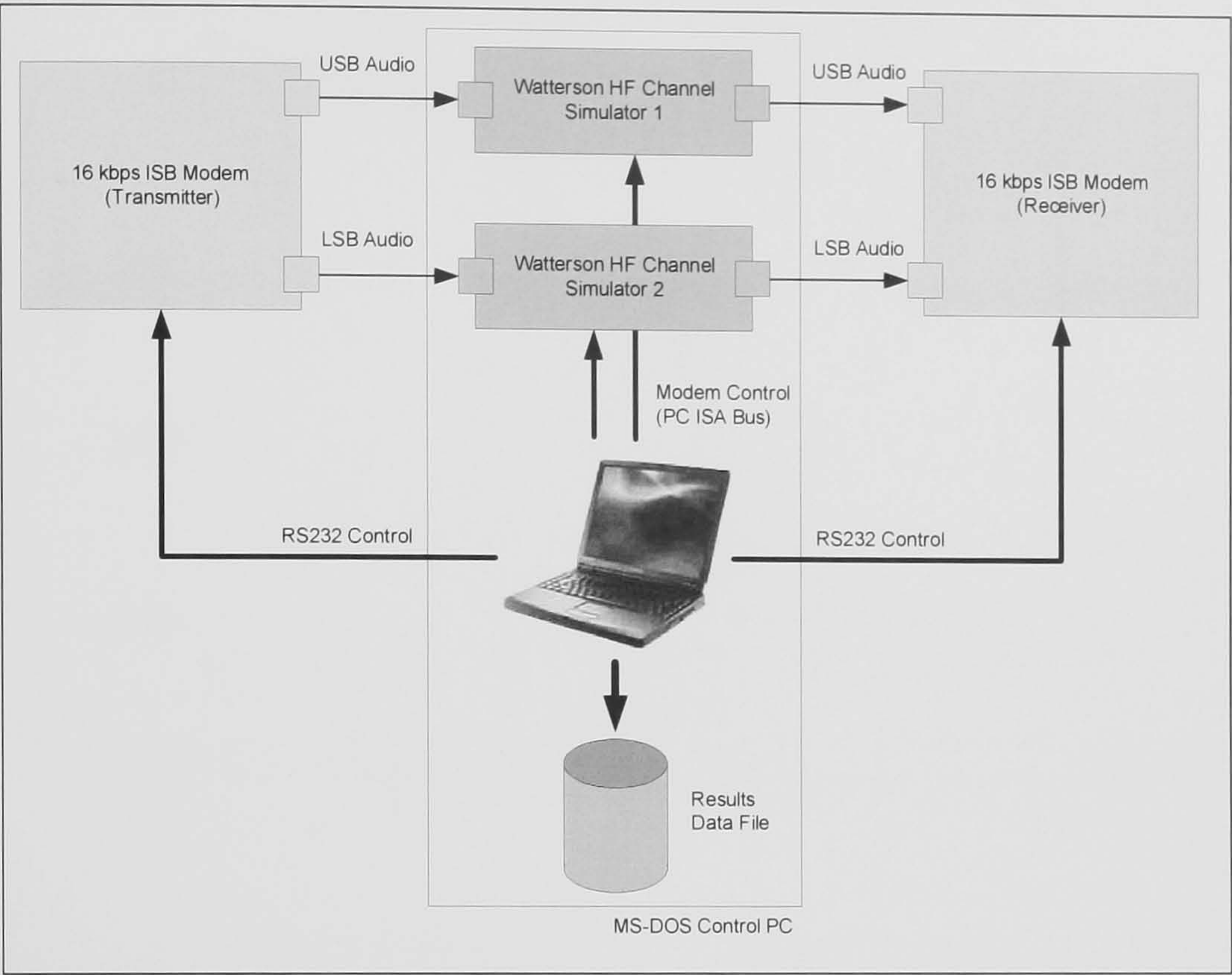


Figure 4-3 16 kbps Modem Laboratory Characterisation

All the results presented are given in terms of signal to noise ratio (SNR) in a 6 kHz bandwidth unless explicitly stated otherwise. The Rayleigh fading imposed by the simulator has a Gaussian spectral profile and is specified in terms of the (2σ) double-sided fading bandwidth.

The modem's bit error rate (BER) performance was measured under a number of standard channel conditions with a number of modem configurations: HC code (zero, short and long interleaving), convolutional code (zero and long interleaving) and uncoded (zero interleaving). Figure 4-4 shows the performance of the ISB modem in a non-fading Gaussian noise channel, and Figure 4-5, that in a flat fading (single mode with 1 Hz Doppler spread) channel. The performance in a CCIR Good channel (two equal power modes with a relative time difference of 0.5 ms and 0.1 Hz fading imposed on each) and in a CCIR Poor channel (two equal power modes with a relative time difference of 2 ms and 1.0 Hz fading imposed on each) are depicted in Figure 4-6 and Figure 4-7 respectively. The multipath in a CCIR Poor channel is beyond the capability of the SSB variant and results in an irreducible bit error rate.

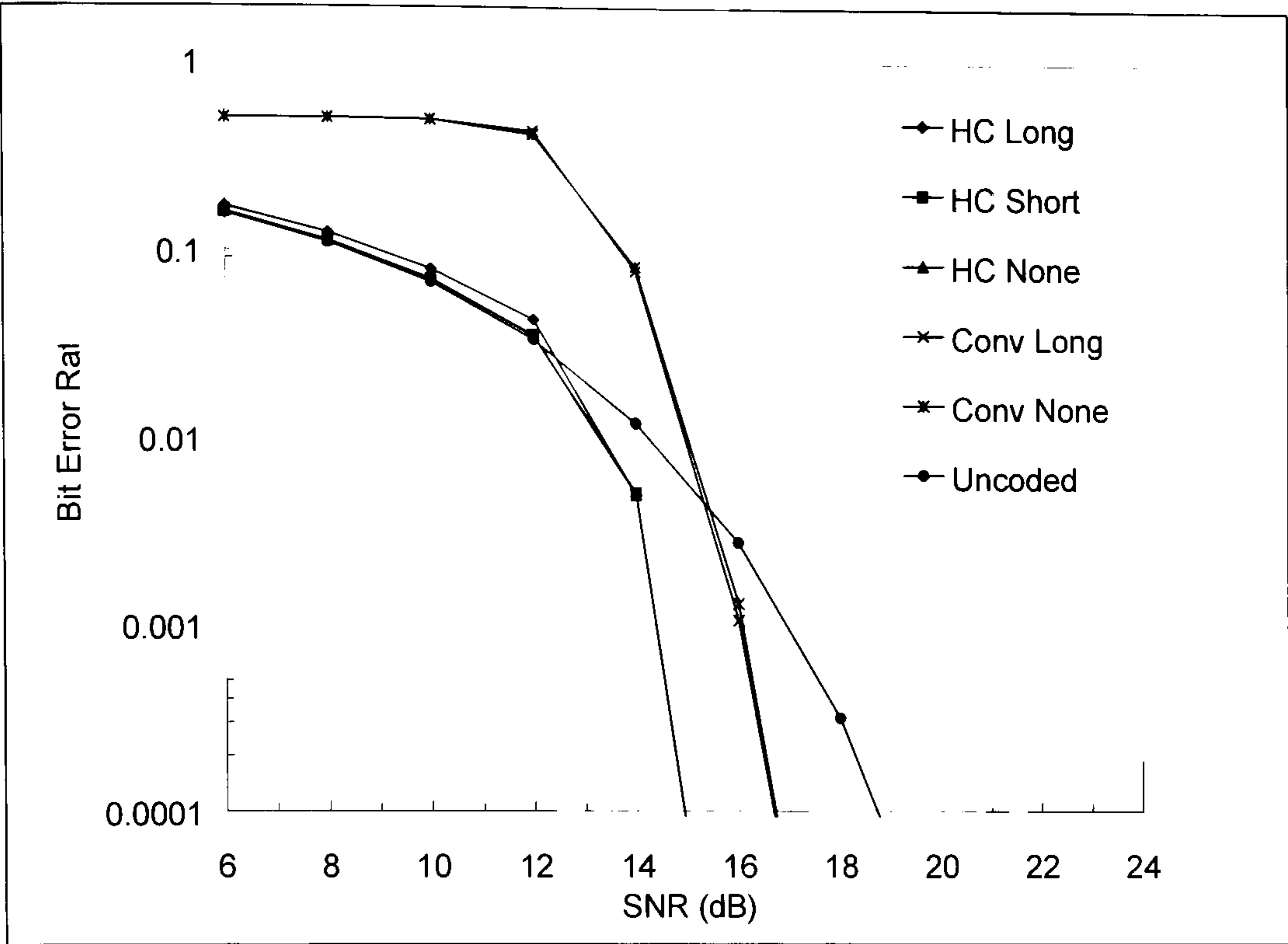


Figure 4-4 16 kbps ISB Modem Performance in a Gaussian Noise Channel.

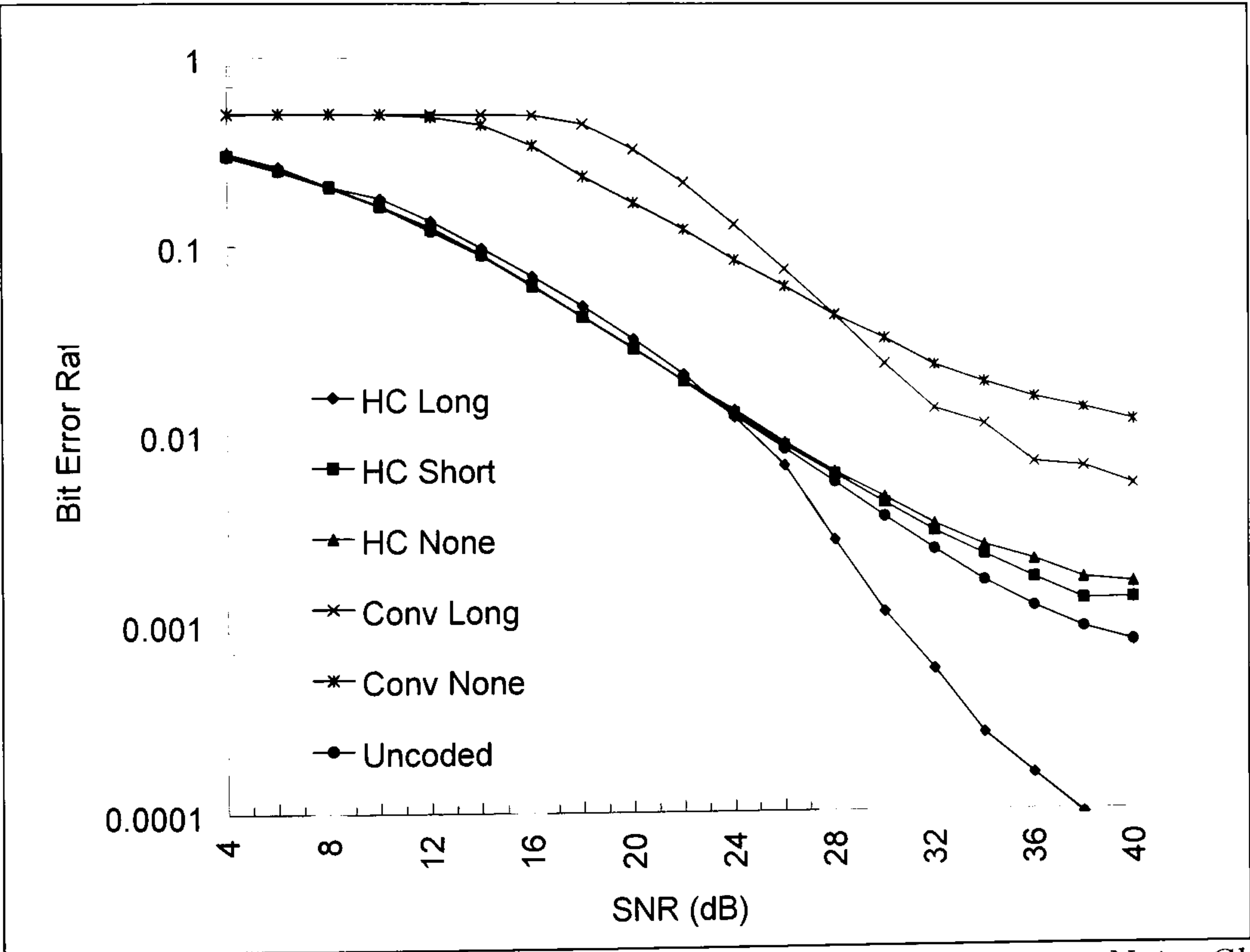


Figure 4-5 16 kbps ISB Modem Performance in a Flat Fading Gaussian Noise Channel

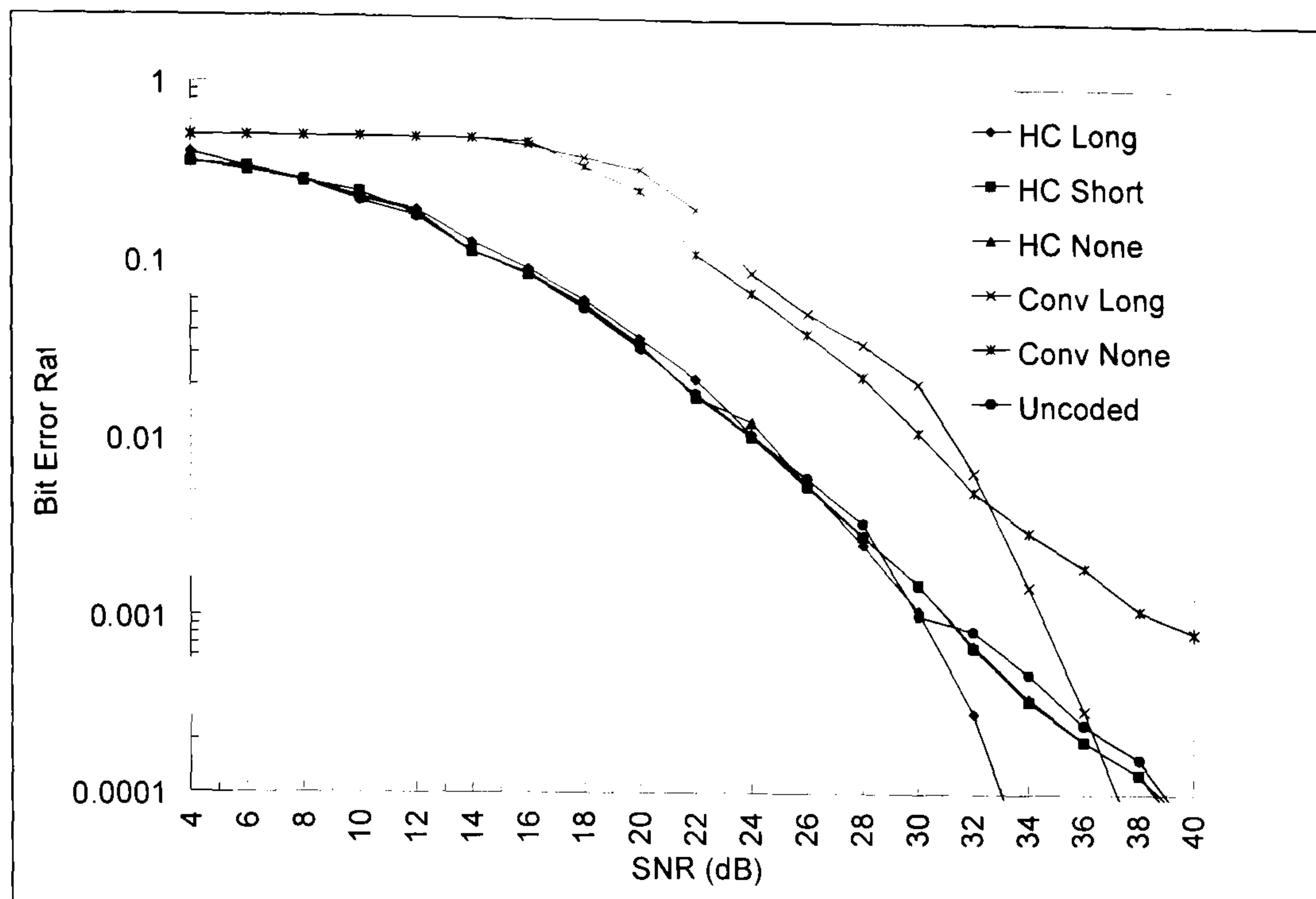


Figure 4-6 16 kbps ISB Modem Performance in CCIR Good Channel

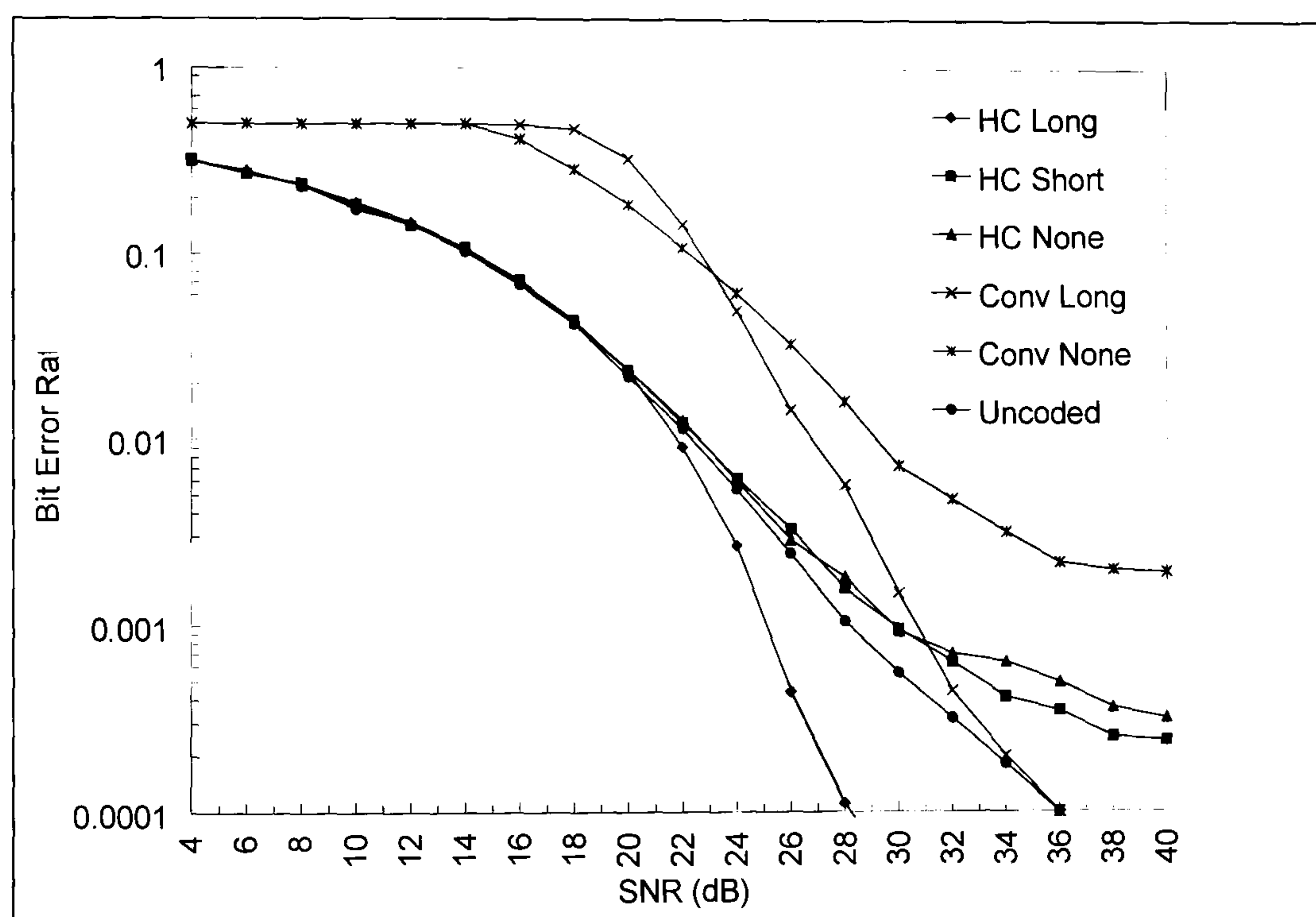


Figure 4-7 16 kbps ISB Modem Performance in CCIR Poor Channel

The operating envelope of the ISB and SSB modem configurations is illustrated in the constant BER plots [Arthur, 72] in Figure 4-8 and Figure 4-9. The achieved performance can be compared with that of the MIL-STD-188-110A 4800 bps single tone waveform in Figure 4-10 (chosen for its high data rate in 3 kHz) and the STANAG 4285 2400 bps waveform in Figure 4-11 (chosen for its similarity in structure to that of the 16 kbps modem). These four plots are normalised to give a SNR with a noise bandwidth of 3 kHz for constant BER of 10^{-3} .

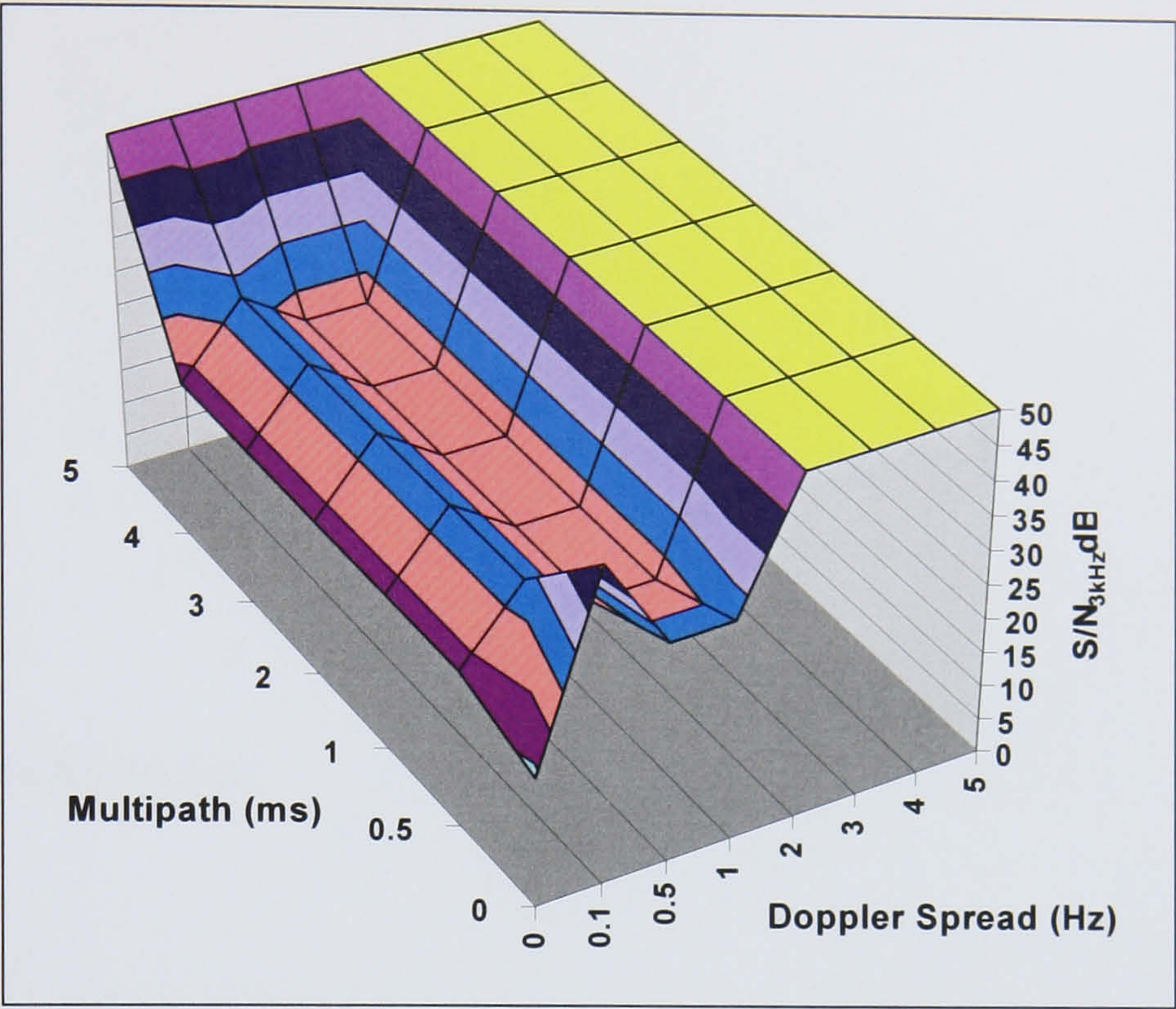


Figure 4-8 Constant BER Surface for 16 kbps ISB Modem (HC codec, long interleave).

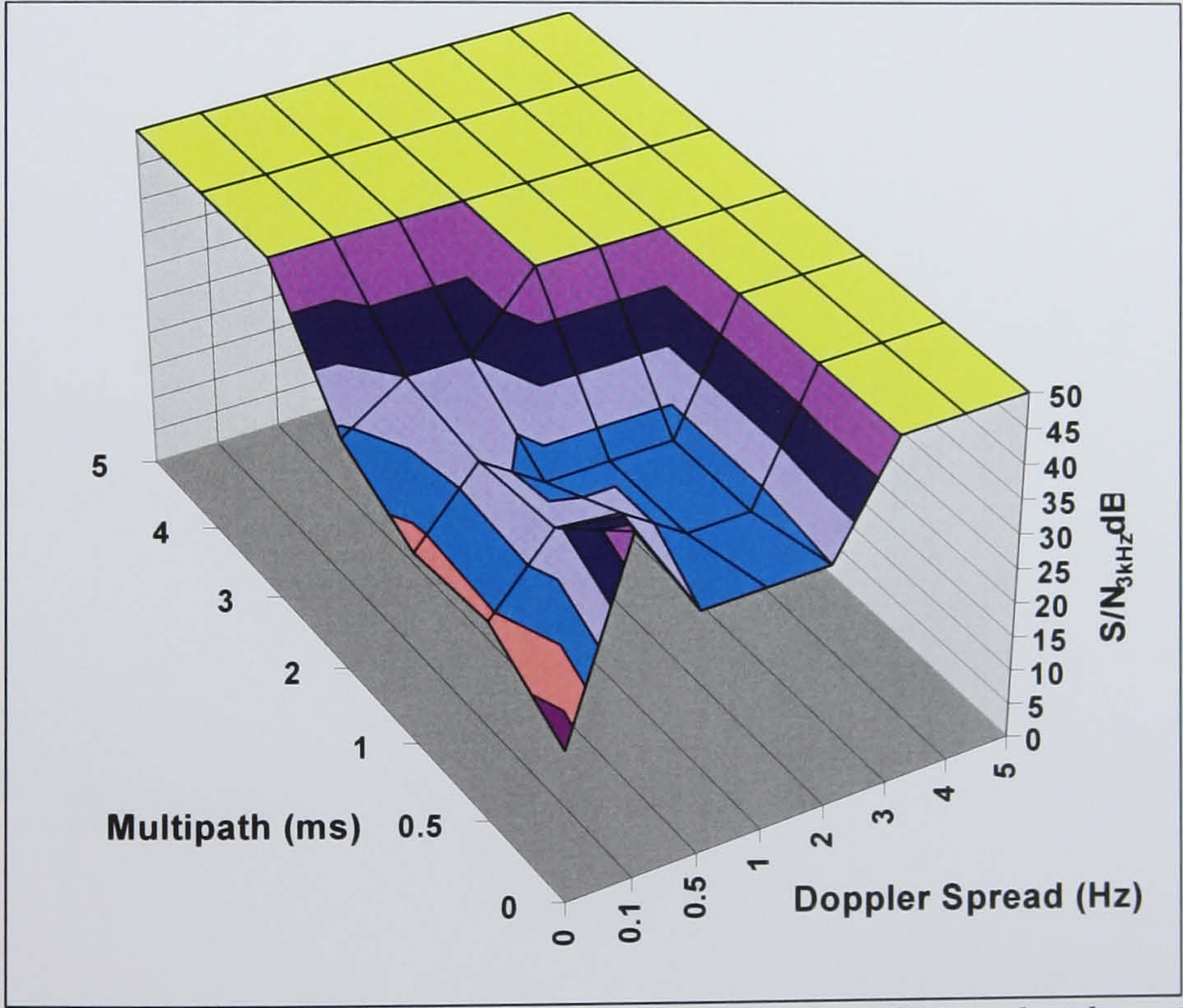


Figure 4-9 Constant BER Surface for 16 kbps SSB Modem (HC codec, long interleave).

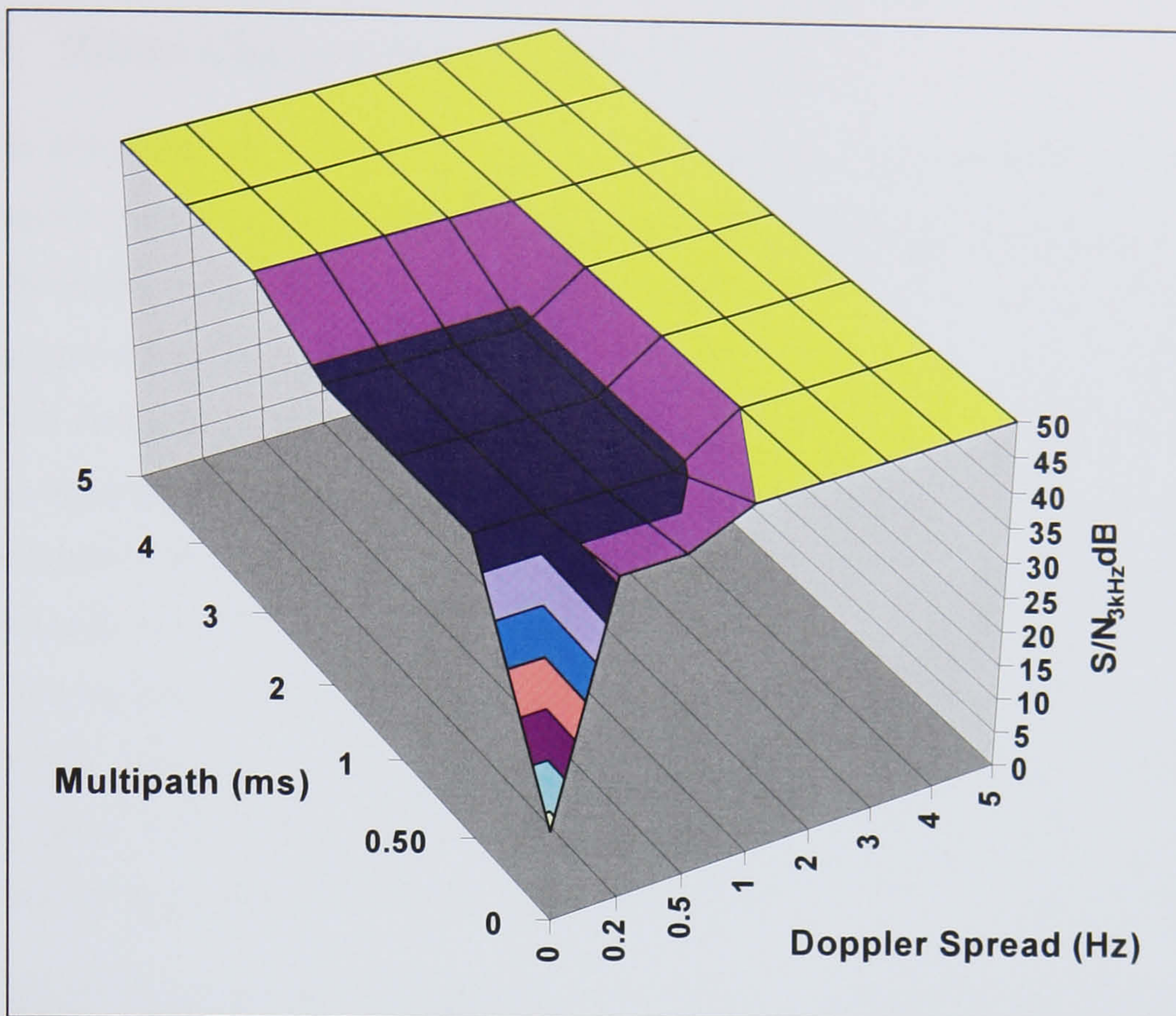


Figure 4-10 Constant BER Surface for 4800 bps MIL-STD-188-110A Modem (uncoded)

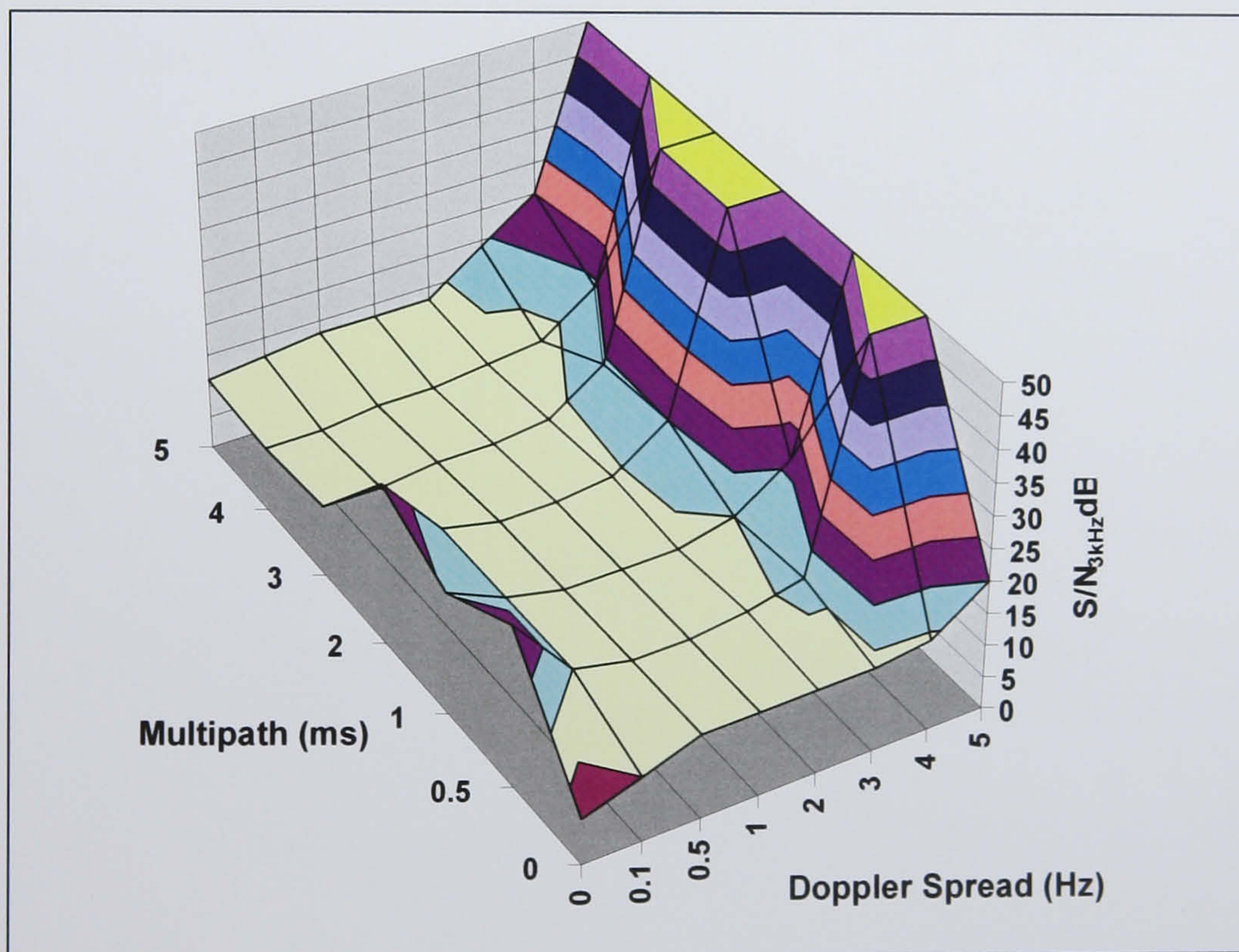


Figure 4-11 Constant BER Surface for 2400 bps STANAG 4285 Modem (convolutional coder, long interleave).

4.2.2 Rician Channel Performance

The HF simulator test results in Figure 4-12 (plotted for a constant BER of 10^{-2} , two same power modes; one non-fading, one with 1 Hz Doppler spread applied and 2 ms between the modes), show that the 16 kbps modem performance increases markedly for Rician type channels (i.e. where there is a non-fading propagation mode in addition to Gaussian fading modes). Such channels occur most frequently at HF when a surface wave component is present. The range achievable using surface wave communications is significantly influenced by the surface conductivity, and is generally at its largest for uninterrupted sea paths. Link budget calculations have been made using ITU surface wave propagation loss curves [ITU, 6]. Even using pessimistic figures for local interference, sea state, etc, the calculations indicate that near error free operation at ranges up to 400 km should be readily achievable in a maritime environment using conventional omni-directional antennas and transmitter powers of the order of 400 W.

Previous generations of modems (particularly parallel tone types) designed for surface wave applications are intolerant of sky-wave components and perform poorly when they are present. The 16 kbps experimental modem is not degraded by the existence of multiple modes within its operating region.

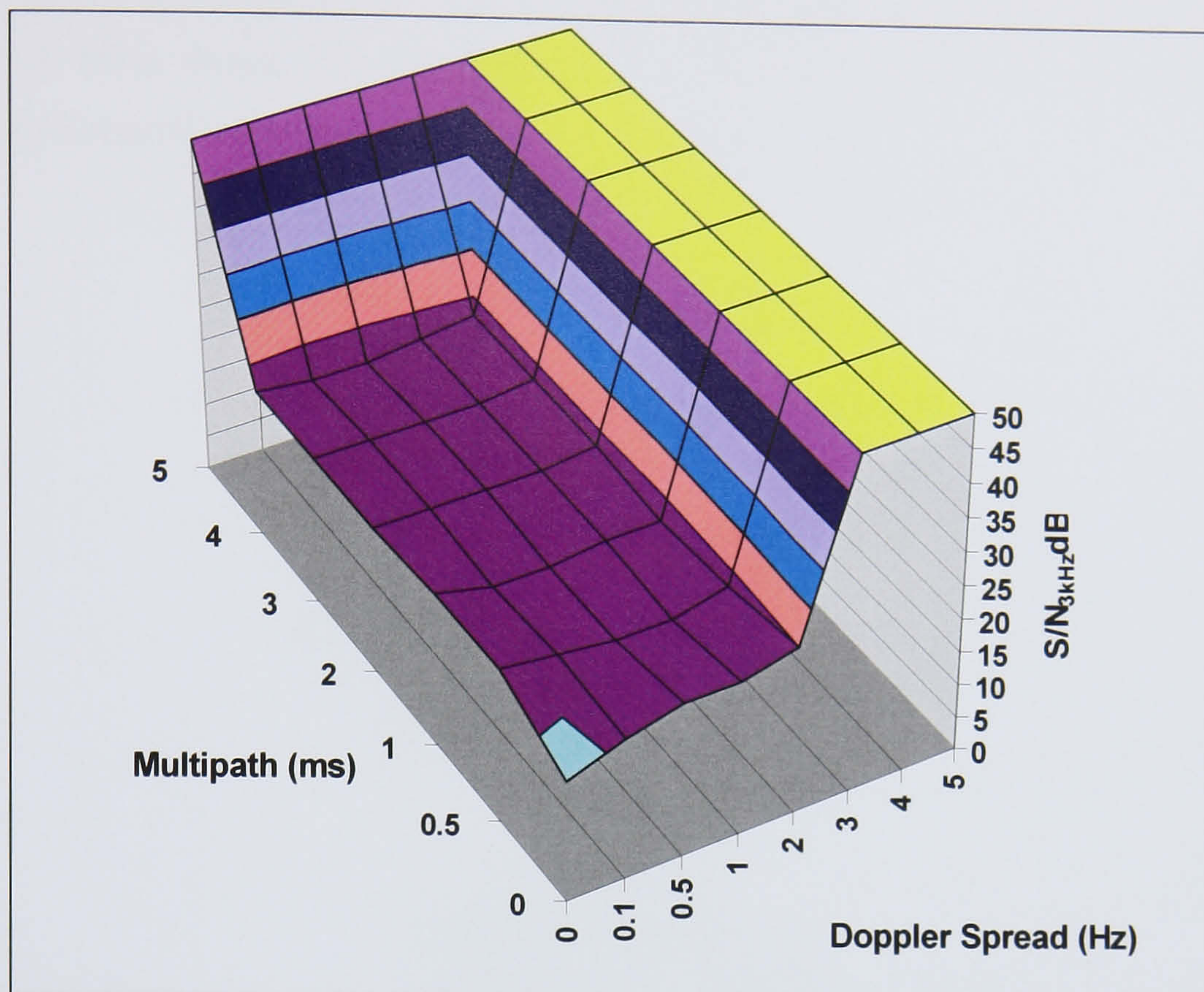


Figure 4-12 Constant BER Surface for 16 kbps ISB Modem using HC Codec and Long Interleave under Rician Channel Conditions

4.3 On-air Trials

4.3.1 Experimental Configuration

Trials were conducted over a 170 km, predominantly East-West, path from DERA Cobbett Hill (Cove Radio) to Malvern in the UK. At the transmit site a 10 kW ISB transmitter (generally operated at ~2 kW) was utilised with a wide-band fan dipole antenna. At the receive site (Malvern) a simple tactical 'droopy' dipole antenna fed a Marconi H2550 digital receiver, operated with independent automatic gain control (AGC) for each sideband and configured to have a fast attack and medium (~0.5 s) decay time. Only the ISB configuration of the modem was tested on-air, principally because it was the configuration that provided the combination of multipath and fading tolerance appropriate to the path.

The on-air trials were automated, being synchronised at each end using Navstar Global Positioning System (GPS) satellite time sources, such that a number of modem configurations and traffic types (BER measurements, file transfer and image transfer)

could be repeatedly exercised. Two frequencies were utilised; 4.8 MHz during the day and 2.8 MHz during the night changing at dawn and dusk in accordance with propagation predictions obtained from ICEPAC [Hand, 85].

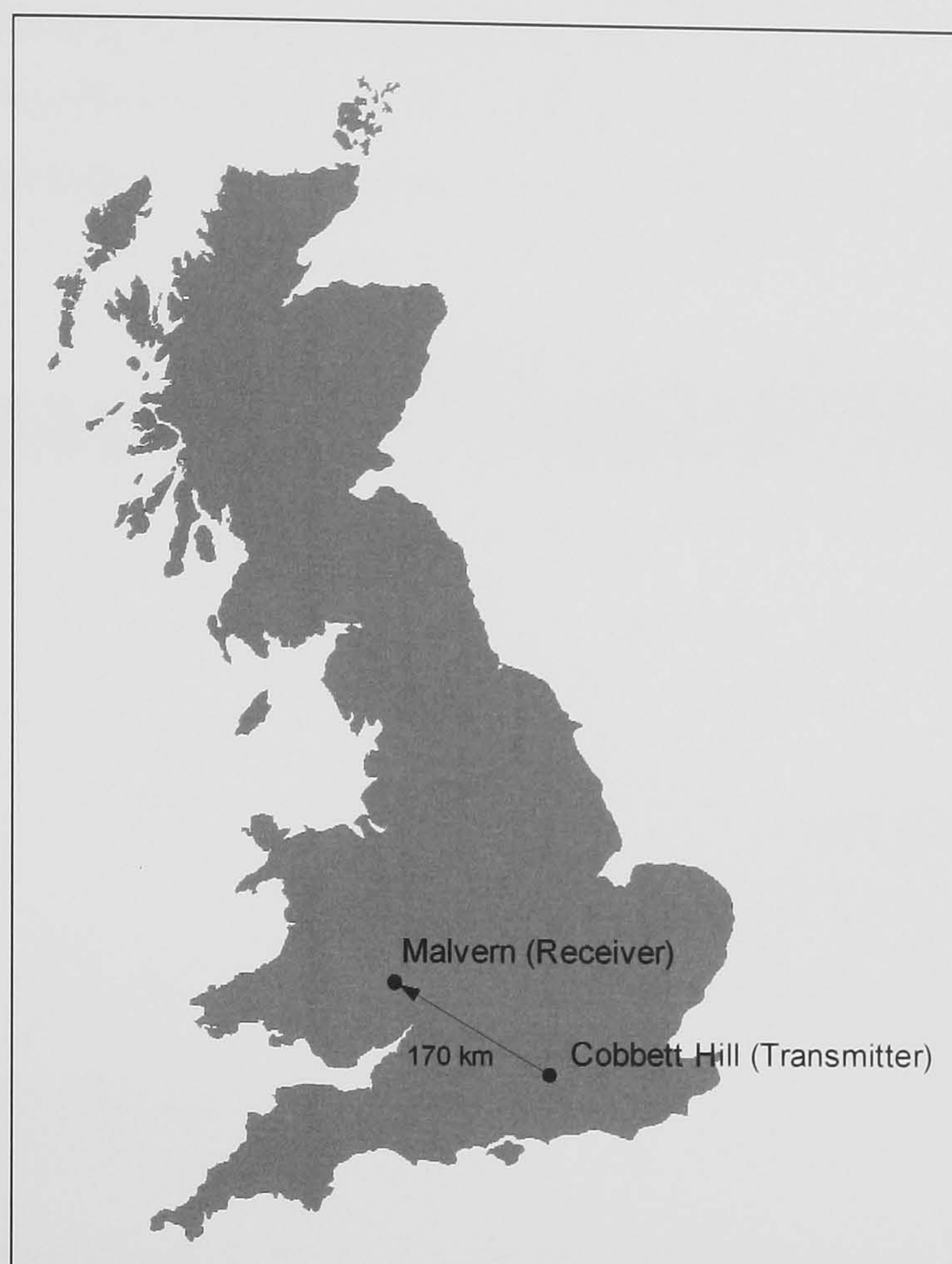


Figure 4-13 Configuration for 'On-Air' 16 kbps Modem Experiment

4.3.2 Results of On-Air Tests

Trials data was collected over a five day period in May 1998 on the Cobbett Hill to Malvern path using the ISB modem with the HC codec and both long and short interleaving. A transmitter power of 2 kW was used, being representative of the maximum power generally available on point-point HF links. The data was analysed in one kilobyte blocks (~ 0.5 s) and the BER calculated. Figure 4-14 shows a diurnal plot of the overall average BER over the trial (all modes). The modem provided error rates below 0.1 for in excess of 80% of the day, only performing worse than this during the night-time period. This performance should allow the modem to be used for some digital voice applications (see section 4.6.4) where high error rates can be tolerated.

An inspection of ionograms collected during the trials period, showed that the principal propagation modes present were single and multi-hop F region returns with occasional, short lived, periods of E-region reflections. Ionospheric support was often limited to a very narrow band of frequencies, especially at night (often < 0.5 MHz), and this has probably had a significant impact on the night-time results. Some form of automated frequency management could be expected to significantly improve the achieved results.

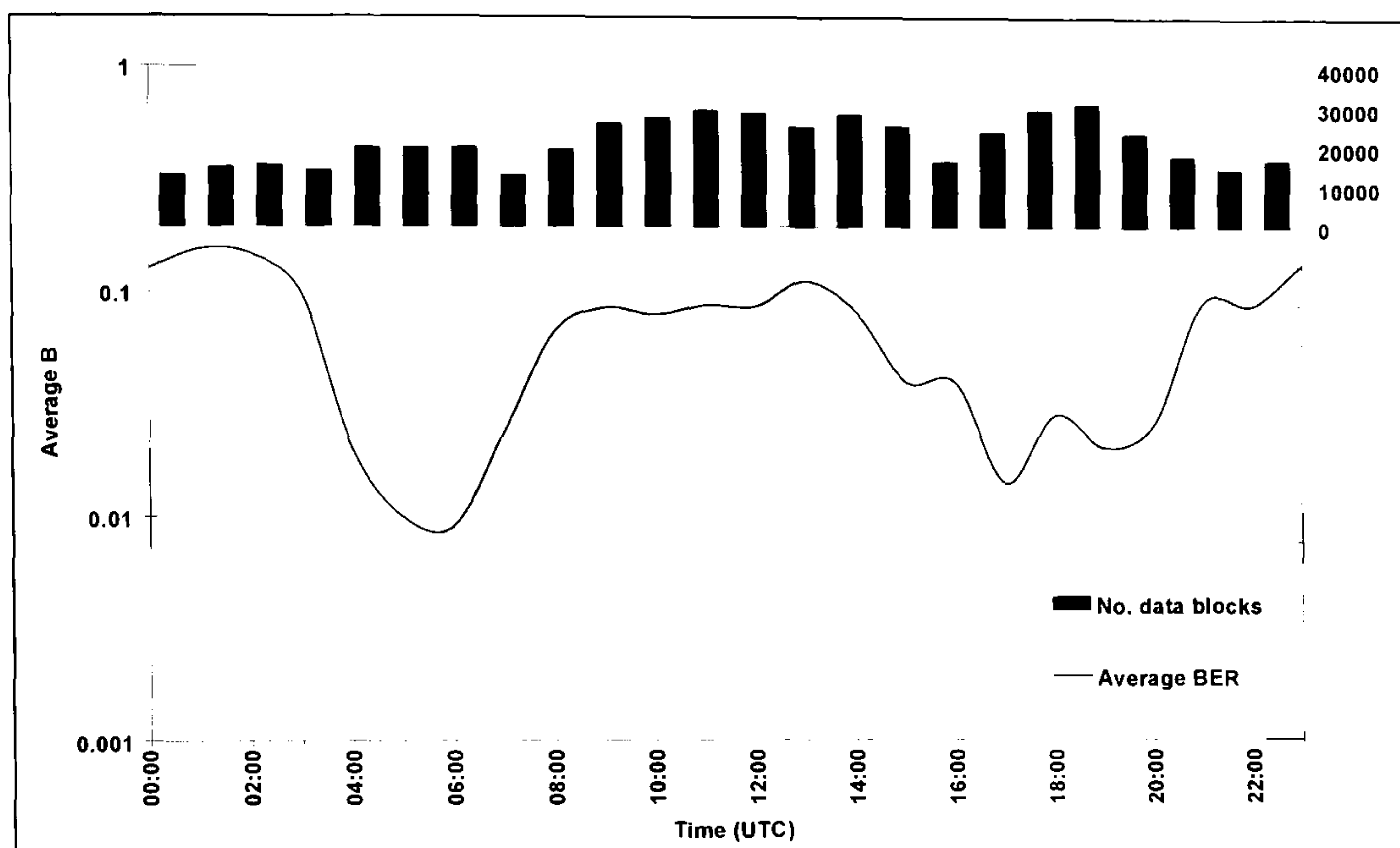


Figure 4-14 Hourly Average BER between Cobbett Hill and Malvern using 16 kbps ISB Modem with HC Codec (histogram shows number of data points in the data set).

The data, analysed in terms of kilobyte frame (block) delivery statistics, is summarised in Figure 4-15. The plots show the percentage of frames delivered at better than or equal to the stated BER. Over a 24 hour period 32% of all received frames were delivered error free while the figure rose to 43% taking just the day-time results (0400 to 1900 UTC). The results show that the modem, in its current form, could not be reliably used for continuous 16 kbps data communications (assuming an acceptable BER criterion of $\leq 10^{-3}$). It would, however, be able to support high throughput communications when conditions allow, particularly if used within an automatic repeat request (ARQ) system employing an effective automatic data rate change mechanism.

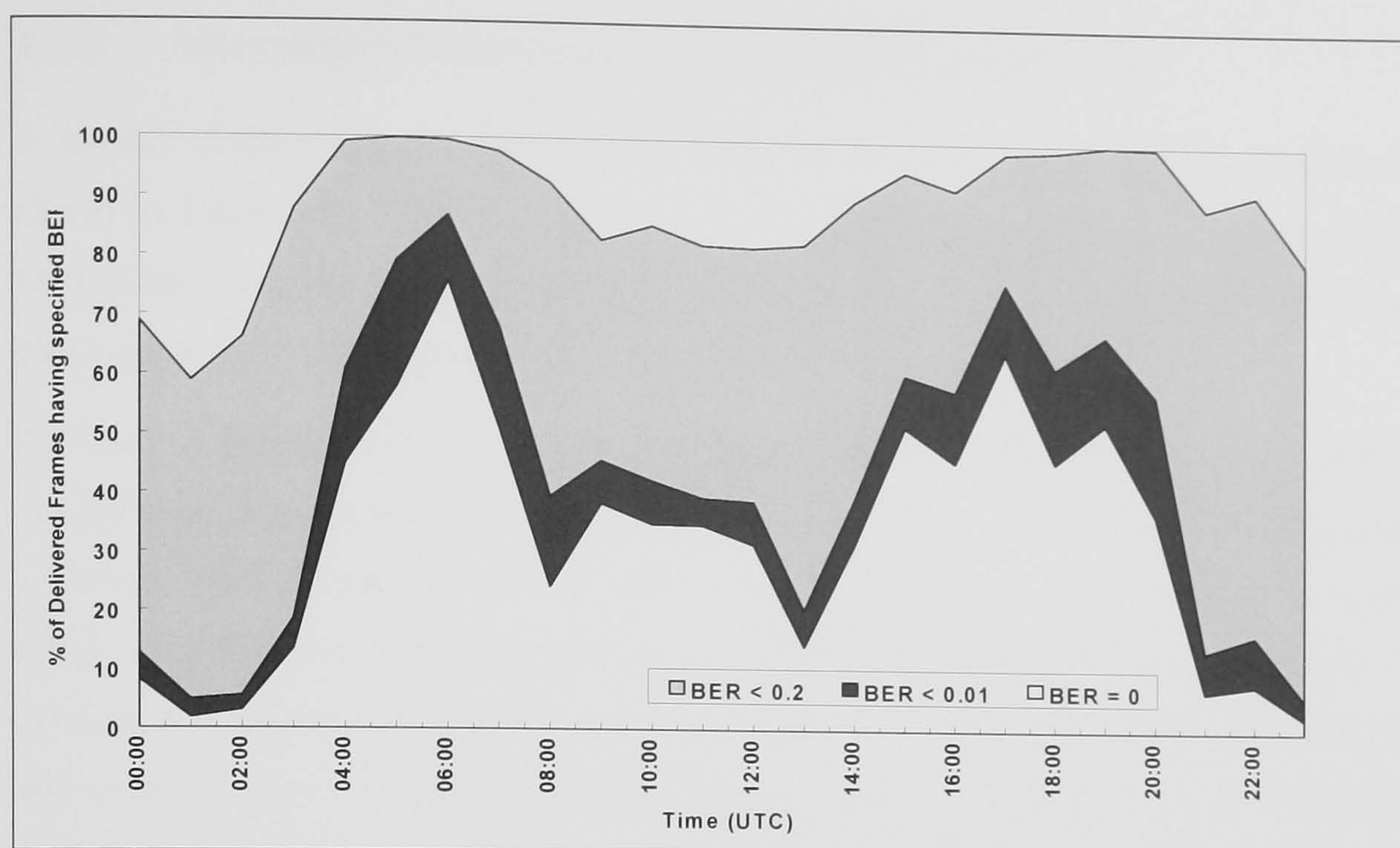


Figure 4-15 Diurnal Kilobyte Frame Delivery Statistics between Cobbett Hill and Malvern using 16 kbps ISB Modem with HC Codec.

4.4 Potential Improvements to the Experimental 16 kbps Modem

Some particular limitations of the 16 kbps modem as tested are known to exist:

- No interference excision was incorporated and so the performance in the presence of co-channel interference was significantly impaired. The incorporation of interference excision (e.g. adaptive tone excision [Darbyshire, 83] or sophisticated techniques such as those based on cyclo-stationarity [Burley, 84]) would be expected to significantly improve performance.
- The modem initial synchronisation and preamble was short (~ 0.1 s) and the modem's initial synchronisation performance consequently weak. This was clearly demonstrated when file transfers were attempted - often the first part of a file was missed while the remainder was received with few errors. A longer initial synchronisation would readily cure this problem.
- The short interleaving option included in the modem was optimised for low latency applications (such as digital voice applications). It has been shown to provide little benefit over the non-interleaved mode and would benefit from being replaced with an interleaver of at least one second duration to provide increased robustness for data communications.

4.4.1 Alternative Extended Bandwidth HDR Waveforms

A number of alternative waveforms with different data rates have also been considered (listed in Table 4-1). These are all waveforms designed to work in a nominal 6 kHz bandwidth using ISB HF radio equipments. In order to provide acceptable performance these waveforms make use of HC iterated forward error correction codes.

It should be noted that the higher data rate modes, those that make use of the 256-QAM constellation in particular, are very susceptible to non-linearities in HF transmitters and receivers. This is because the waveforms are of a multi-level nature and so accurate relative amplitude control from symbol to symbol is important. The non-linearities of concern include the radio system filters, the transmitter automatic level control (ALC) and receiver AGC. It has been found that operating receiver's AGC in the slow (or 'voice') mode where the AGC has a fast attack (several milliseconds) and slow decay (2 to 4 s) is normally acceptable. The transmitter ALC has proven to be more problematic, as in many designs, it cannot be (fully) disabled. A number of modern, generally digital, transmitter drive units have been shown to provide good performance.

User Data Rate (kbps)	Waveform (Data-Training Ratio)	Modulation	Code Rate
32	330-30	256-QAM	0.913
28.8	288-31	256-QAM	0.837
19.2	250-31	64-QAM	0.758
16	282-31	16-QAM	0.938
14.4	288-31	16-QAM	0.837

Table 4-1 Extended Bandwidth 6 (3+3) kHz HDR Waveforms

4.5 Comparison of Extended Bandwidth Modem Performance

Figure 4-16 and Figure 4-17 illustrate the performance achieved by these alternative HDR extended bandwidth modem waveforms [Jorgenson, 86]. For comparison the performance of the 3 kHz bandwidth MIL-STD-188-110B 9.6 kbps modem has also been plotted in Figure 4-16. As expected, the SNR required to support a given data rate is significantly reduced when the transmission bandwidth is allowed to increase.

The performance of these modems is such that they could be expected to perform satisfactorily on surface wave and mixed mode (Rician) propagation paths. Successful

sky-wave operation may be possible for the lower rates when the links are suitably engineered (appropriate radio path, antennas and transmitter powers etc).

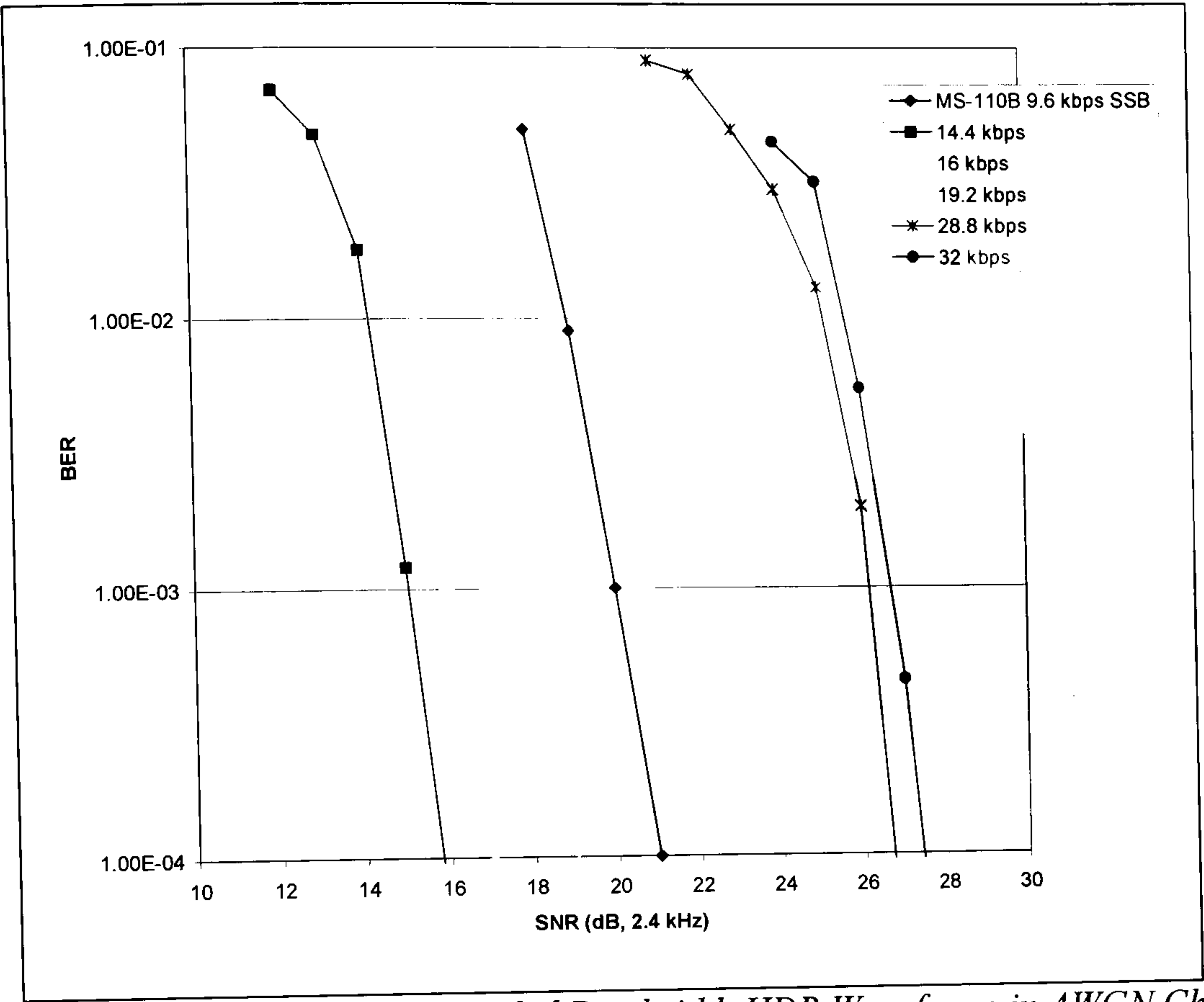


Figure 4-16 Performance of Extended Bandwidth HDR Waveforms in AWGN Channel

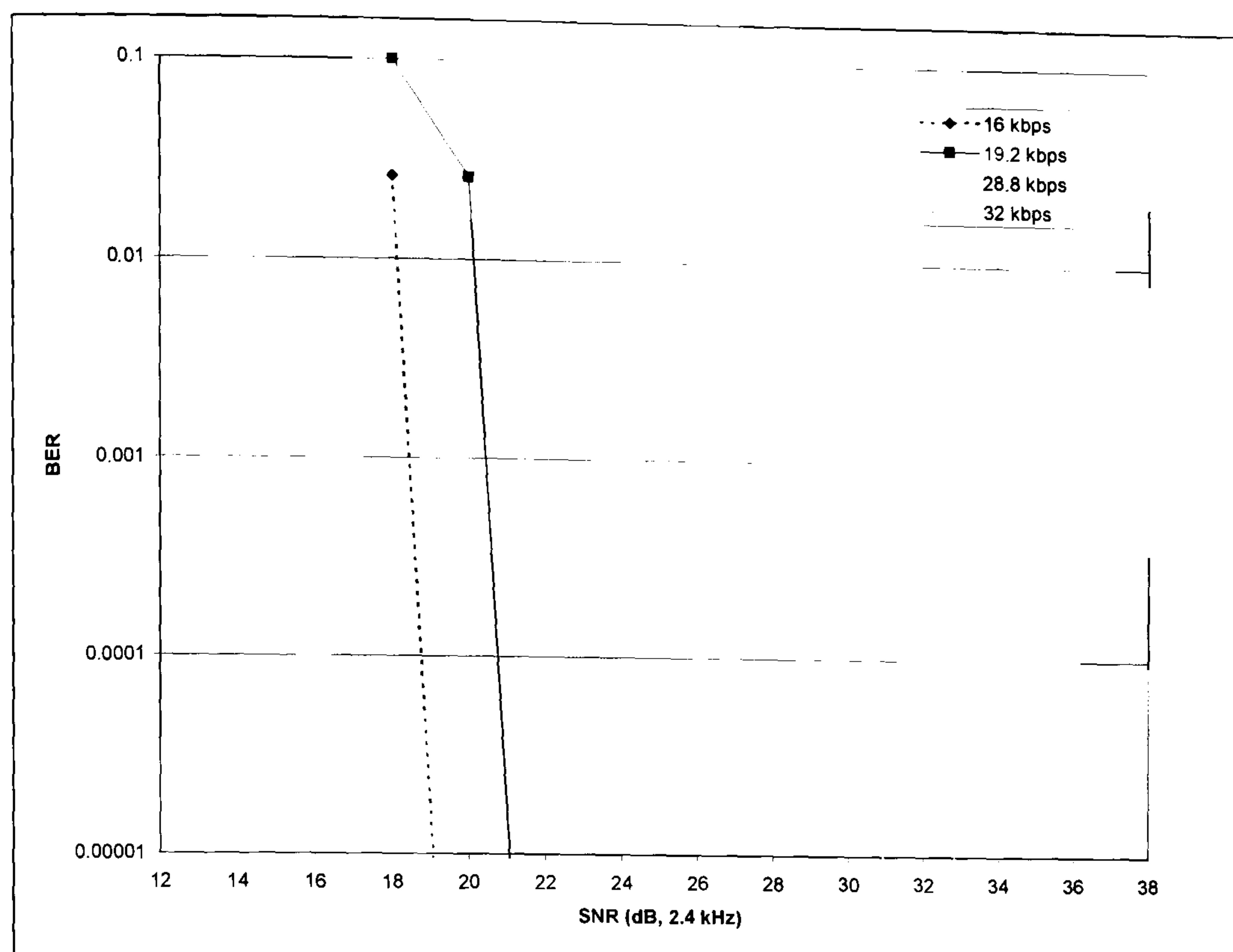


Figure 4-17 Performance of Extended Bandwidth HDR Waveforms in a Rician Fading Channel (one non-fading and one -6 dB Gaussian fading mode).

4.6 Application of Extended Bandwidth HDR Modems

4.6.1 Data Communications and Networking

The results of laboratory testing and trials of the new modem waveforms described in this chapter have shown that they may be used over benign channels where adequate received SNR can be achieved. The waveforms could be used effectively within an adaptive system employing ARQ alongside other more robust alternatives to maximise throughput under favourable conditions. The most likely application are for links that are predominantly over surface wave or Rician paths. Calculations indicate that high availabilities should be possible over distances up to ~ 400 km on sea paths suggesting uses such as high throughput BLOS HF maritime data communications, data links and inter-networking.

4.6.2 Digital Broadcasting

The potential data rates of the experimental waveforms that have been considered may be suitable for use in high quality digital HF broadcasting. They offer an alternative

high-performance serial tone waveform technology to the OFDM waveforms presently being standardised for systems such as DRM.

4.6.3 Image Transmission

A good application for high data rate HF modems is the transmission of imagery. Pictures (of the order of 160 Kbytes when compressed) were successfully transmitted using robust HF image compression and coding techniques [Chippendale, 87] and the 16 kbps modem in ~90 s.

4.6.4 Range Extension for Line-of-Sight Radio Networks

A possible application of high data rate HF modems is for providing beyond line-of-sight (BLOS) range extension to V/UHF tactical communications networks (e.g. tactical military networks). Often, these existing links are relatively high BER bearers and therefore the traffic that uses them is appropriately resilient. An example is continuously variable slope delta-modulation (CVSD, [Proakis, 14]) vocoders that are able to operate acceptably with BERs up to ~20%. The use of 16 kbps HF for extending existing CVSD networks, while not an optimal technical solution, obviates the need for trans-coding between CVSD and low data rate vocoders such as LPC-10 [NATO, 88] which is, of itself, a technically challenging task.

4.6.5 Maritime Situation Awareness

Having established that extended bandwidth HDR modems can be expected to operate well in a maritime propagation environment one possible application is a high throughput system to allow the sharing of situation awareness data between platforms. Traditional military systems achieve this at HF using NATO Link-11 which has a throughput of ~2.2 kbps whilst line-of-sight systems, such as NATO Link 16, provide minimum throughputs of in excess of 16 kbps. There are also many civil applications.

4.7 Standardisation of Extended Bandwidth HDR HF Modems

The work presented here made a direct contribution to the standardisation of high throughput modem waveforms for extended bandwidths (i.e. 6 kHz ISB) in MIL-STD-

188-110B [DOD, 2]. This standard is a major new release of an internationally applied HF modem interoperability standard.

4.8 Chapter Summary

This chapter has described a novel high data rate 16 kbps prototype HF modem. Unlike extant HF modems designed for operation in standard 3 kHz allocations it operates in an extended bandwidth of 6 kHz (either contiguous SSB or ISB). The ISB variant employs an architecture that exploits signal diversity between the sidebands. Results from HF simulator measurements and on-air testing of the modem have been presented. The performance limitations of such high data rate modems have been discussed suggesting they have application to surface wave and benign HF Skywave channels. The work presented contributed to the standardisation of higher throughput waveforms for use in fielded communications applications and demonstrated the value in exploiting wider bandwidths for HF radio applications. The following chapters present new work on digital HF radio architectures capable of supporting wideband and multi-channel transmission and reception.

Chapter 5.

On the Specification and Design of Digital HF Radios

For many years multi-conversion super-heterodyne receiver designs have been dominant in high performance radio communication systems (particularly at HF). Recently, with the development of affordable high performance analogue-to-digital converters and digital signal processing (DSP) technology, intermediate frequency digitisation has become increasingly popular [Wepman, 89]; [Brannon, 90]. Sophisticated implementations, having increasing proportions of the radio/modem functionality in programmable devices (programmable logic devices (PLDs) and DSP processors), are commonly termed software defined radios (SDRs). The ultimate goal is the true software radio [Mitola, 91] in which the signal captured at the antenna is digitised and processed entirely digitally in programmable devices. Technology in this field is developing rapidly. In reality there is almost a continuum of possible receiver implementations that range from conventional analogue implementations to true software radios. The essential features of these different classes of receiver is summarised in Figure 5-1.

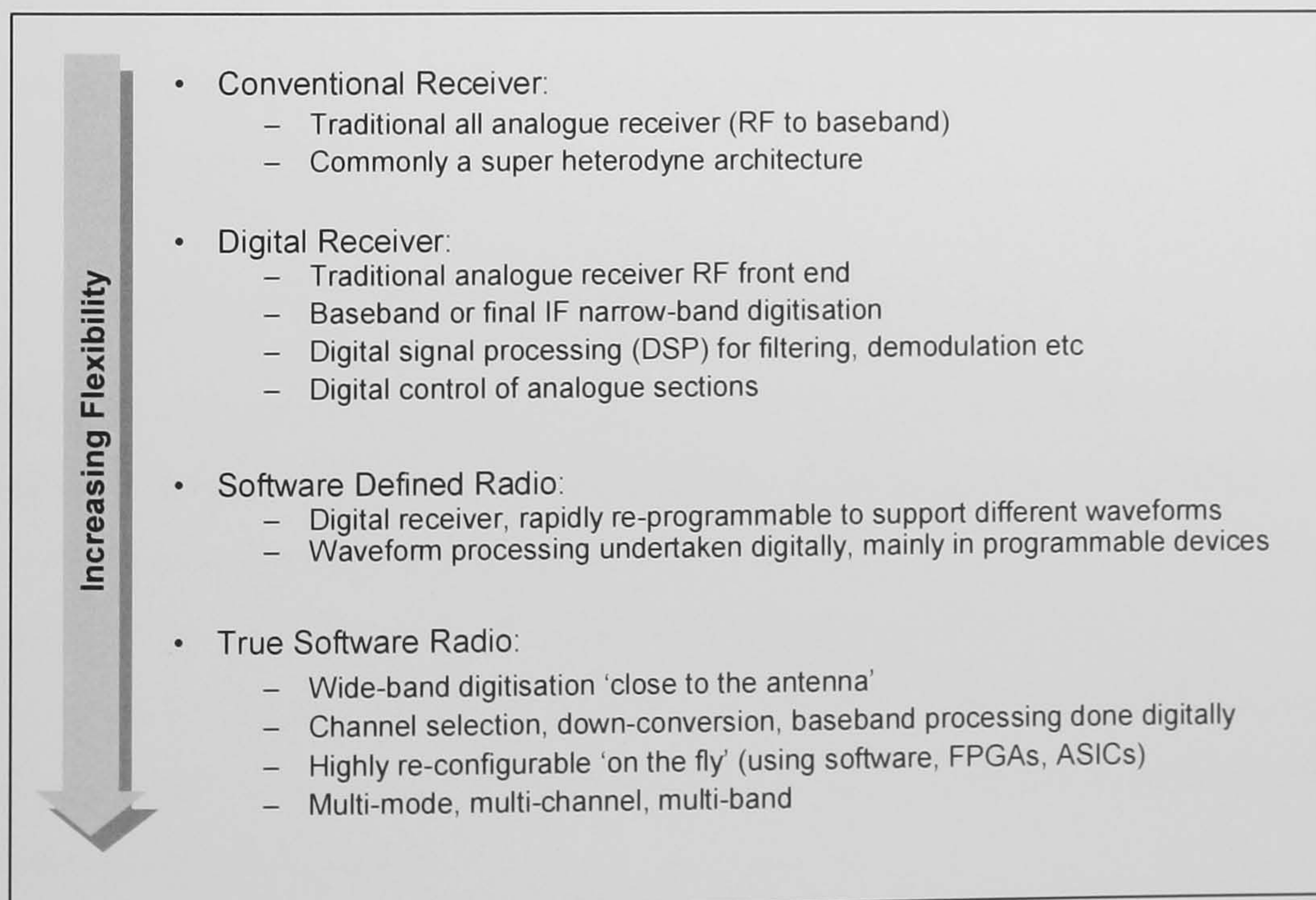


Figure 5-1 From Conventional Analogue Receiver to Software Radio

Work presented in the previous chapter identified the need for radios capable of wideband and multi-channel operation to support higher throughput HF communications. This chapter provides a brief résumé of the technology developments that are making software radios possible. The relative merits of a number of possible wideband receiver architectures are considered. Performance requirements for an HF receiver, as dictated by the HF environment and the intended application, are studied in some detail. Results of work to characterise a high performance single channel conventional super-heterodyne HF receiver are presented in Appendix C to help establish the current ‘state-of-the-art’. The work described in this Chapter presents a new whole-band digitisation approach, applicable to HF, where the whole band (2-30 MHz) is digitised and DSP algorithms are used to select, down-convert and demodulate signals of interest. Potential benefits of such an approach include:

- reduced complexity and lower component count;
- simultaneous reception of multiple signals;
- programmable channel bandwidth (support for wideband channels);
- software re-configurability; and
- potential for high performance.

The predicted characteristics of a practical implementation of such a receiver are investigated in detail. Finally, an alternative wideband architecture employing a single conversion is proposed and the predicted complexity/performance compared with the direct sampling approach.

5.1 Applicable Technology Developments

Traditionally, a great deal of new radio communications technology was a result of research in support of military requirements. However, new developments are increasingly a result of the rapid progress being made to support the commercial sector. In particular, the rapid growth of the personal communications systems (PCS) industry with its need to rapidly develop and field new multi-standard base-stations and small, low-cost handsets is of note. Examples of the critical technologies that are enabling new radio architectures include:

- High performance analogue-to-digital converters (ADCs) and digital-to-analogue converters (DACs);
- Low-cost digital up-converters (DUCs) and digital down-converters (DDCs) in the form of application specific integrated circuits (ASICs);
- High speed, high capacity RAM based field programmable gate arrays (FPGAs) and sophisticated development tools;
- High performance general purpose DSP devices;
- Improved RF devices (e.g. Monolithic Microwave Integrated Circuits, MMICs); and
- New families of devices (e.g. miniature electro-mechanical structures, MEMS).

5.2 Wideband Digital Radio Architectures

There are a number of basic architectures applicable to HF receivers and also a number of hybrids. These primarily include super-heterodyne receivers, direct conversion (zero-IF) receivers, single conversion (sub-harmonic) IF-sampling receivers and direct sampling wideband digital receivers. Each of these are considered in turn.

5.2.1 Conventional Super-Heterodyne Receivers

The architecture of a typical three conversion super-heterodyne (superhet) receiver is depicted in Figure 5-2. Signals applied to the antenna input are first filtered to remove out-of-band components (known as pre-selection). They are then mixed with a tuneable synthesised local oscillator signal to a common first intermediate frequency (e.g. 81.4 MHz in an HF receiver). The selected signal is filtered, generally using crystal or mechanical filters, to the maximum channel bandwidth the receiver is designed to handle. Amplification, controlled by an automatic gain control (AGC) circuit, is applied. The signal is then mixed to a 2nd IF frequency (e.g. 1.4 MHz in an HF receiver) where there is a further AGC amplifier and filtering to the final required bandwidth. The final mix produces the baseband output signal. Narrow-band digital receiver hybrids may employ final IF or baseband digitisation.

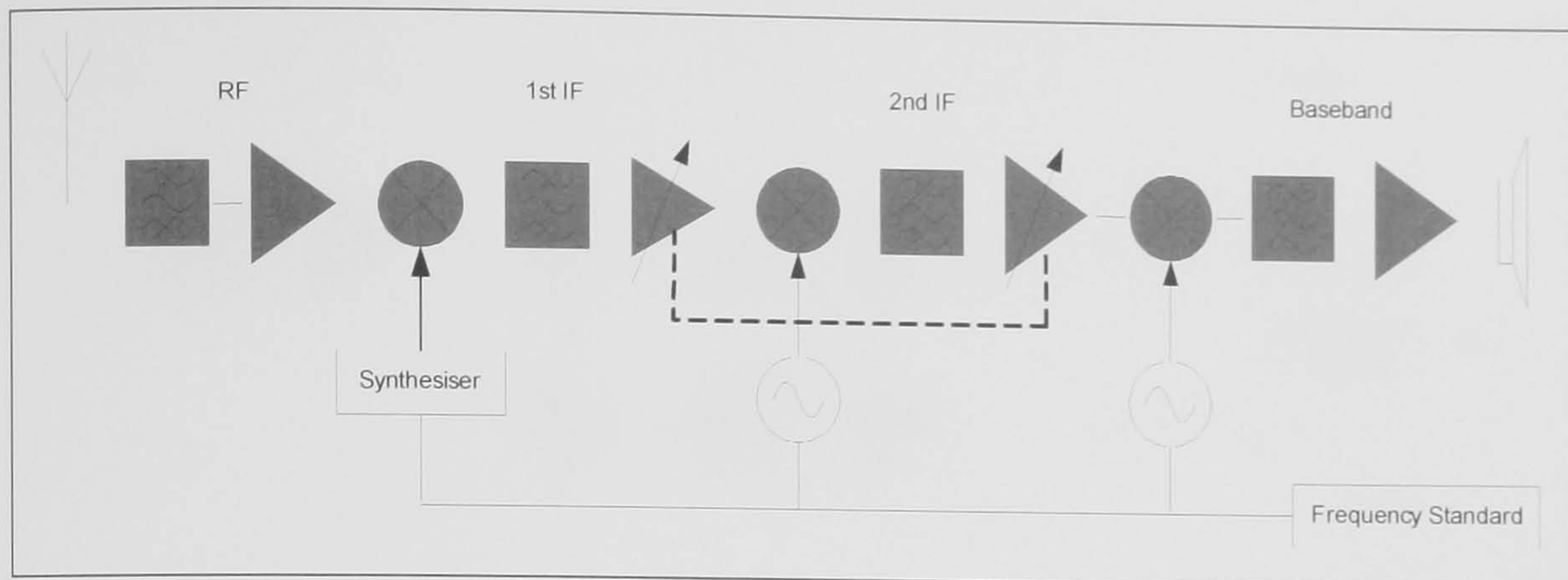


Figure 5-2 A Super-Heterodyne Receiver Architecture.

Multiple IF stages are used because it is difficult to provide sufficient selectivity (≥ 110 dB) and gain (up to 100 dB) at any single frequency without signal leakage occurring. A high quality (typically synthesised) tuneable local oscillator (LO) is required to allow tuning to the frequency of interest in addition to fixed LOs for the subsequent mixing stages. In order to prevent frequency errors all the local oscillators are normally phase locked to a single frequency standard. In most designs, limited dynamic range at each stage necessitates the use of a complex AGC system to preserve receiver performance. Whilst excellent performance can be achieved, these types of receiver are generally limited to receiving a single (normally narrowband) channel at any one time, are challenging to design and have a high component count.

5.2.2 Direct Conversion (Zero-IF) Digital Receiver

In the direct conversion ('Zero IF') receiver a quadrature mixer is used to convert the signal directly to complex baseband where it can be amplified and digitised (Figure 5-3). In theory this process results in perfect cancellation of the image signal. The potential advantages of this architecture include low complexity in the signal chain, simple filtering requirements and easier image suppression than in the superhet. However for HF use, a direct conversion receiver requires a high quality synthesiser capable of tuning over close to four octaves (2-30 MHz) and providing accurate quadrature outputs. Such a synthesiser is complex and offsets potential simplifications achieved elsewhere. Further, performance is critically dependent on the balance achieved within the quadrature mixer; normally implemented as a single hybrid component (including the 90° phase shifter). Any amplitude or phase imbalances will result in imperfect cancellation of the image.

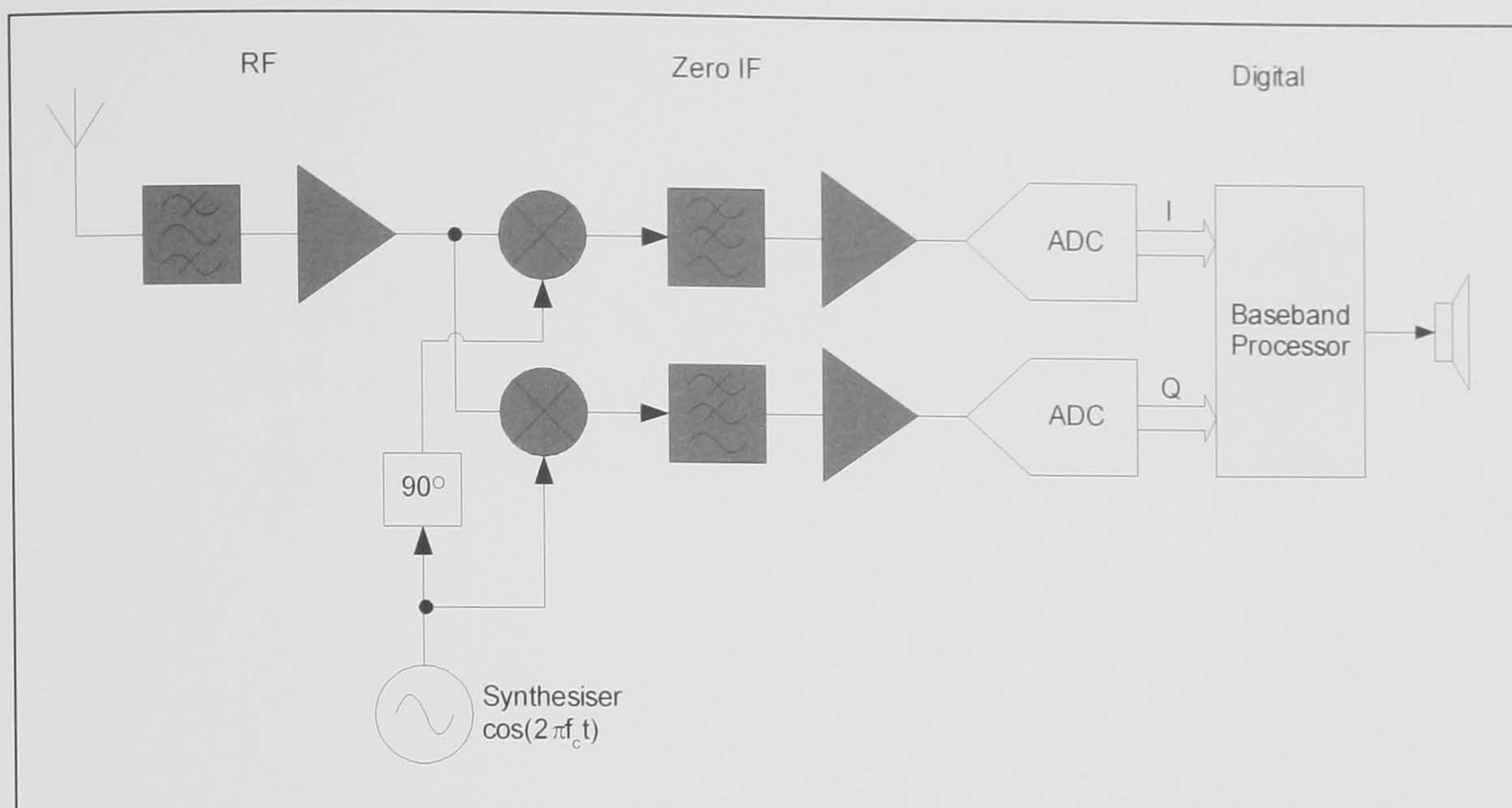


Figure 5-3 Direct Conversion 'Zero IF' Receiver Architecture

It can be shown [Razavi, 92] that the image suppression (image rejection ratio, IRR) provided by a mixer with an amplitude magnitude unbalance ε and a phase deviation of θ from 90° is given by:

$$IRR = 10 \log_{10} \left(\frac{1 - 2(1 + \varepsilon) \cos \theta + (1 + \varepsilon)^2}{1 + 2(1 + \varepsilon) \cos \theta + (1 + \varepsilon)^2} \right) \text{ dB} \quad (5-1)$$

The implications of even small imbalances in amplitude and phase are demonstrated in the plot of IRR in Figure 5-4. Good, commercially available, quadrature mixers might typically guarantee an amplitude/phase balance of 0.1 dB and 1° respectively. This only provides ~ 40 dB of rejection. This is a particular problem for use at HF frequencies where the image frequency may well be in-band.

Another particular problem is the so-called DC offset. This can occur due to amplitude offsets in the ADCs. It can also occur due to LO or strong signal breakthrough which results in self-mixing and hence a DC component [van Rooyen, 93; Beach, 94], which lies right in the centre of the wanted complex baseband signal.

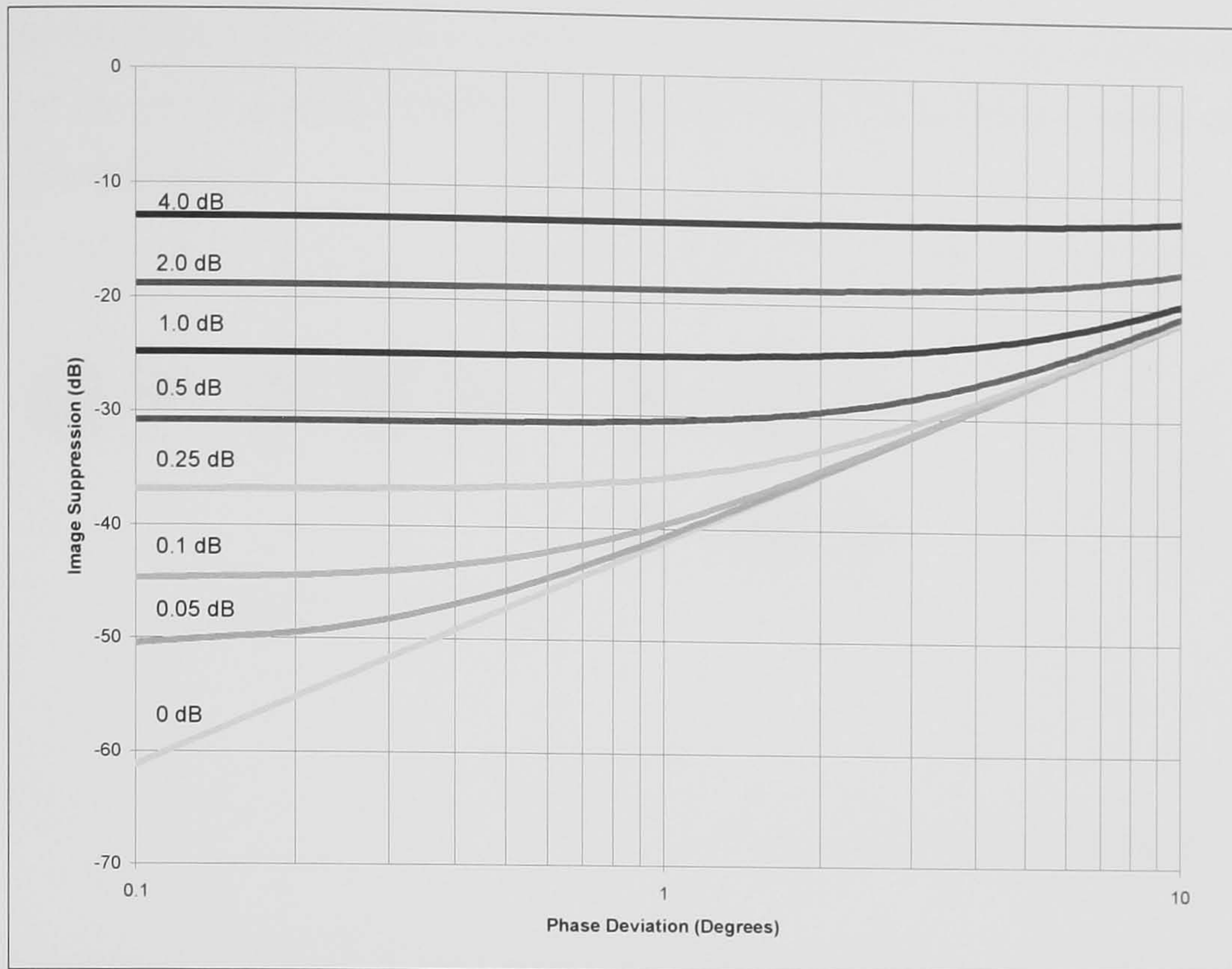


Figure 5-4 Image Suppression in a Quadrature Mixer Due to Amplitude and Phase Imbalance

Correction techniques [e.g. Yuanbin, 95] can be applied to correct both the DC offset and mixer imbalance using a reference signal to measure the error and then to apply a correction to the IQ signal once digitised. However it remains difficult to ensure perfect cancellation, particularly across wide bandwidths. The problem of DC offset correction is further exacerbated when receiver (or environment) motion causes a time dependency requiring continuous adaptation.

Practical direct conversion receivers have been demonstrated at HF. They are, however, fundamentally single-channel narrowband receivers.

5.2.3 Super-Heterodyne Receiver with Zero-IF Conversion

A hybrid HF receiver architecture (Figure 5-5) has been proposed by Coy *et al* [Coy, 96]. This employs a conventional tuned synthesiser and heterodyne mixing stage to reach a 1st IF where a roofing filter selects the signal to be received. A fixed quadrature down-conversion stage, followed by quadrature digitisation is used to provide the required selectivity. This narrowband architecture has the advantage that whilst the same IQ balance problems exist as in the direct-conversion receiver they are easier to overcome because only a single narrowband IF-frequency needs to be considered. A

high performance digital receiver based on this architecture has been implemented by Coy and shown to give good results. However, it is fundamentally a single channel, narrowband receiver.

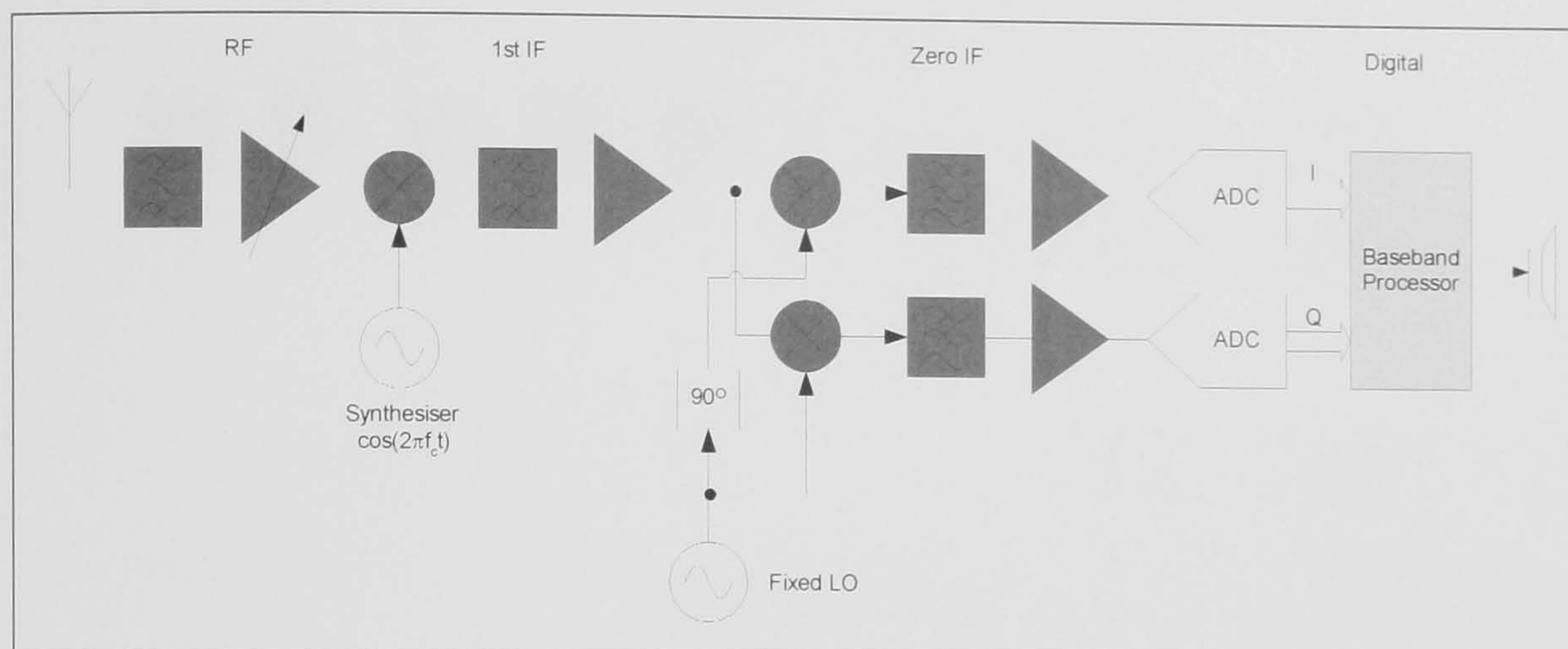


Figure 5-5 Super-heterodyne with Zero-IF Stage

5.2.4 Single Conversion IF-Sampling Receiver

Another possible architecture is a hybrid of the superhet receiver which relies on a single conversion followed by filtering and bandpass sampling (sub-sampling) of the IF to directly down-convert the IF to baseband. In a wideband multi-channel receiver the ADC may be followed by a bank of digital receivers to recover a number of wanted channels (Figure 5-6).

The choice between single or multiple conversion is primarily related to the need to provide high selectivity and to reject mixer images. In a receiver with narrowband sampling multiple conversions will generally be required, requiring a tuneable LO. In a wideband receiver capable of whole-band digitisation, since both the pre-selector filter (before the mixer) and IF filter can be used to provide the required selectivity ahead of the ADC single conversion is sometimes possible. In this case a single, fixed LO can be employed.

At least one conversion is required in higher frequency receivers (currently UHF and above) because the ADC analogue bandwidth is limited and so prevents direct band-pass sampling at the signal frequency. If this architecture were to be used for an HF receiver with a single up-conversion its only potential advantage over a direct sampling approach (discussed next) is that the majority of the RF gain can be applied at an IF frequency chosen to ensure amplifier harmonics will fall out-of-band. Disadvantages

include the additional analogue circuitry required (LO, mixer and filter) and the associated non-linearities that they introduce.

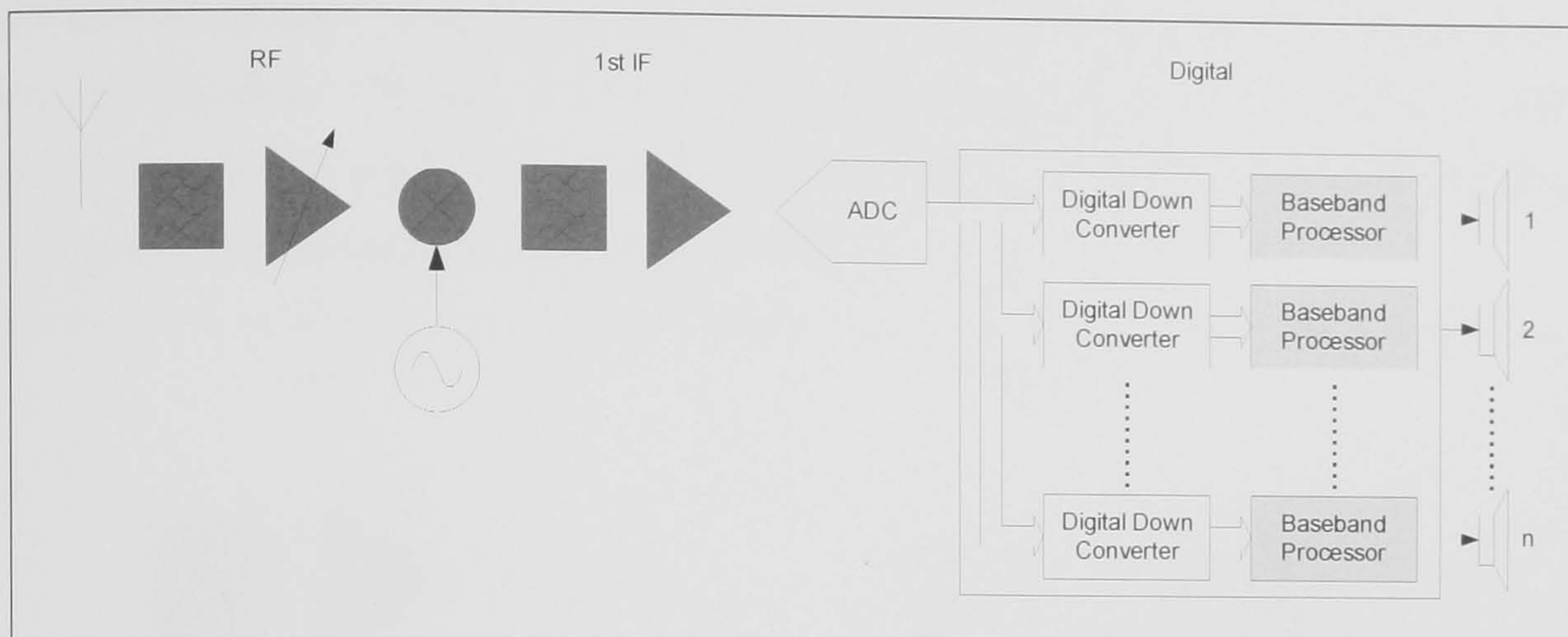


Figure 5-6 Single Conversion IF-Sampling Receiver

5.2.5 Direct Sampling Wideband Digital Receiver

A direct sampling digital receiver digitises the RF input signal directly (using a high dynamic range ADC) and then processes these signals digitally (Figure 5-7). The antenna input feeds a filter which acts as a pre-selector and as the anti-aliasing filter for the receiver digitiser. This is followed by an RF amplifier with digitally controlled gain. As will be shown later, the overall dynamic range requirements of an HF receiver are so large (~140 dB) that it exceeds that of any currently practical ADC devices (typ. 90+ dB). The gain control is therefore required to ensure that, in a changing signal environment, the receiver's instantaneous dynamic range is maximised but that the ADC is never saturated. In a narrowband receiver AGC action is continual, primarily tracking the power of the wanted signal (which in a fading channel can result in additional unwanted modulation on the received signal). In this wideband architecture the adaptation is in response to the total energy present in the band (i.e. many uncorrelated signals). It would therefore be expected, in most circumstances, to require adaptation at a much slower rate (possible on the timescale of minutes or longer).

To capture the whole HF band (2-30 MHz), the ADC digitisation rate would have to be in excess of 60 mega-samples-per-second (MSPS). All subsequent processing can be done in the digital domain including signal selection (filtering), frequency translation (down-conversion) and sample rate decimation. The high processing rates of these functions indicate that they should be implemented in (programmable) DDC ASICs or

possibly PLDs. An arbitrary number of channels can then be extracted by using multiple DDC functions fed from the single ADC. Great flexibility over reception frequencies (fixed, sweeping or hopping), channel bandwidths, digitally applied gain, etc are possible. Finally, as in all the other architectures, general purpose DSP processors may be used for the relatively low rate baseband signal processing (including functions such as signal demodulation, AGC etc).

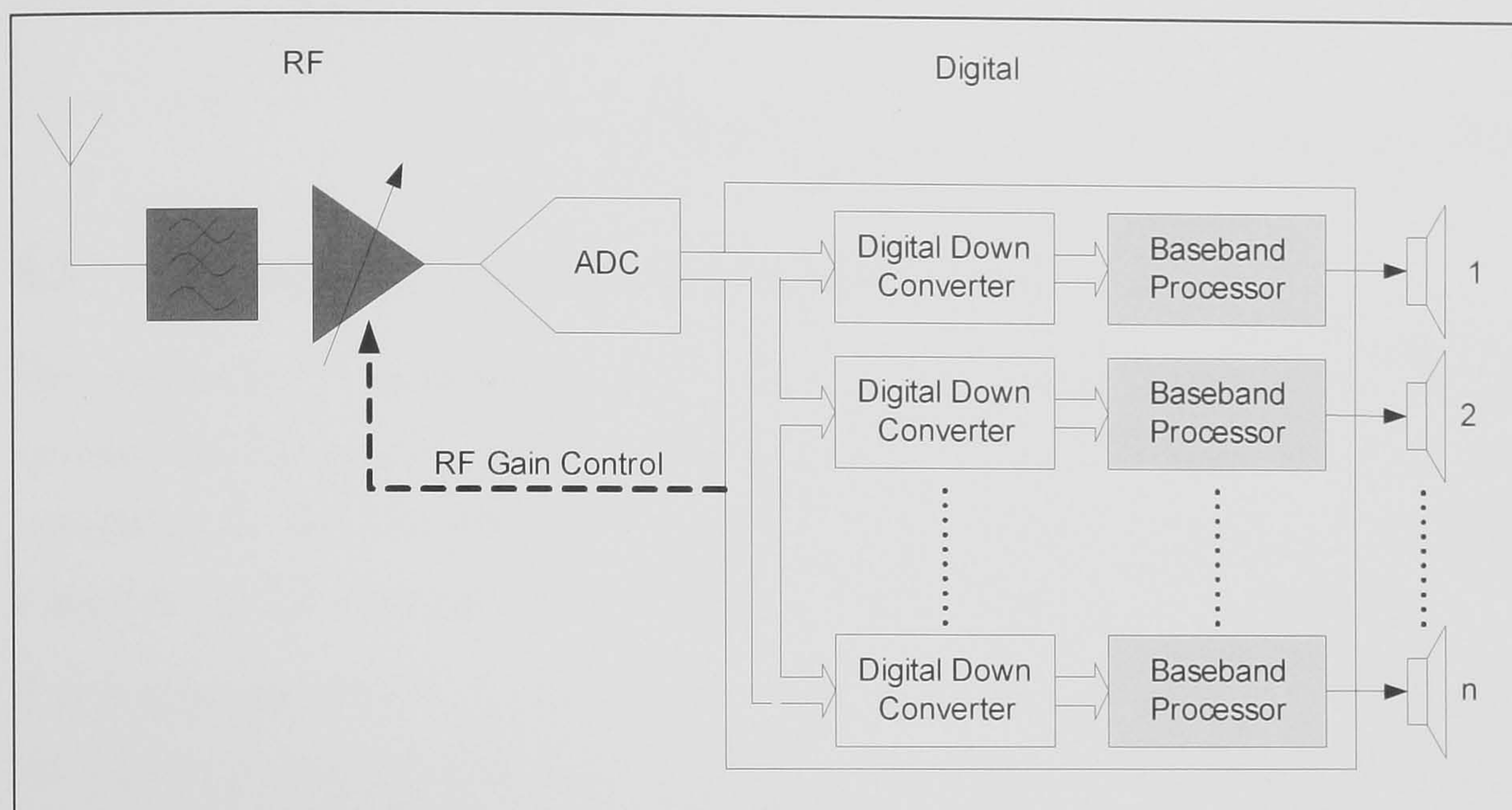


Figure 5-7 Block Diagram of a Wideband HF Digital Receiver

An investigation of component technology and, in particular, ADCs and DDC ASIC implementations suggest that a high performance HF receiver with this architecture may be practical for the first time. This thesis will go on to consider an HF receiver design with this architecture in much greater detail. In the next chapter results are given for a prototype receiver of this type.

5.2.6 Architecture for a Wideband Digital Transmitter Exciter

A complimentary, wideband, direct sampling architecture can be contemplated to implement a multi-channel digital transmitter. Complex baseband signals are fed to DUCs. The DUC output, interpolated up to a sampling rate appropriate for the RF output frequency, is applied to a digital-to-analogue converter (DAC). The resulting RF signal is amplified to allow it to drive (excite) a suitable power amplifier (PA). A high roll-off filter is used as a re-construction filter to remove DAC harmonics (aliases).

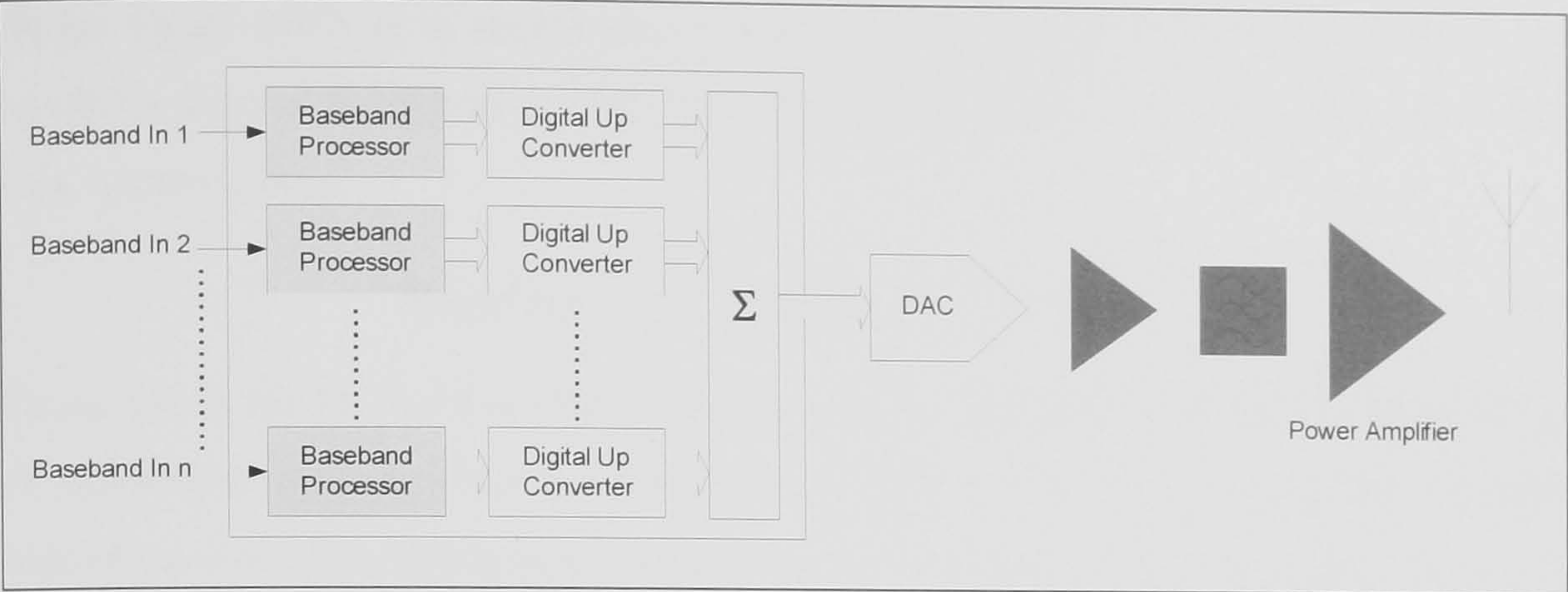


Figure 5-8 Block Diagram of a Wideband Digital Transmitter

5.3 HF Receiver Performance Requirements

The performance requirements of HF receivers are largely governed by the HF environment and are investigated in the following sub-sections. These are compared with the performance provided by a typical high quality conventional receiver providing a baseline against which new HF software radio implementations can be evaluated.

The performance characteristics of a commercial high performance super-heterodyne HF receiver [Racal, 104] have been measured to provide a comparison against which alternative architectures can be assessed. The measurements and results are described in Appendix C.

5.3.1 Sensitivity

The sensitivity of a receiver is a measure of the weakest signal that can be satisfactorily received and demodulated. This is often related to the limiting equivalent thermal noise power at the input of the system [Fisk, 97], given by:

$$Thermal\ Noise\ Power = 10 \log_{10}(kTB) \quad dBW$$

(5-2)

where

- k is Boltzmann’s constant (1.38×10^{-23} J/K);
- T is the system temperature in degrees Kelvin; and
- B is the system bandwidth in (Hz).

Noise figure (NF) is a standardised measure of a system's noise level above the available thermal noise power. For a standard temperature, T_0 , of 290 K the noise floor of a system is thus:

$$\text{NoiseFloor} = NF + 10\log_{10} B - 174 \quad \text{dBm} \quad (5-3)$$

Reception in the HF band is often externally noise limited due to galactic, atmospheric or man-made noise. This is illustrated in Figure 2-10 which shows the effective contribution of these different noise sources, above thermal, in the HF band.

In order to always be externally noise limited an HF receiving system, located at a quiet receive site and operating at the higher end of the band, should have a noise figure of ≤ 16 dB. This is equivalent to a noise floor of -158 dBm/Hz or a -113 dBm signal providing 10 dB SNR in a standard 3 kHz bandwidth. As can be observed from the graph, at HF this is a limiting condition and, in many cases (e.g. at lower frequencies), poorer overall receive system sensitivity can be tolerated. However, it should be noted from a practical point of view that additional receiver sensitivity may still be useful to overcome losses ahead of the receiver such as in the antenna¹ and antenna feed.

5.3.2 Large Signal Handling (De-sensitisation and Blocking Dynamic Range)

Traditional receiver designs make use of RF AGC circuits to maximise sensitivity whilst preventing large signals causing saturation which would result in non-linear operation and the generation of spurious products. Operation in the presence of strong signals generally necessitates a reduction in RF gain and therefore sensitivity. A receiver's strong signal handling (also termed de-sensitisation or blocking performance) is a measure of its ability to contend with large un-wanted signals whilst continuing to receive a weak wanted one. Blocking dynamic range (BDR) is defined as the difference between the receiver noise floor and the off-channel signal power that must be present at the input of a receiver to force it to reduce its RF gain and therefore its sensitivity.

¹ Particularly for electrically small passive antennas such as short whips.

A study undertaken by Lott et al [Lott, 98] measured the total signal energy present in the HF band (2-30 MHz)¹. This gave integrated signal powers between a day time minimum of $80 \text{ dB}\mu\text{Vm}^{-1}$ and a peak night time maximum of $120 \text{ dB}\mu\text{Vm}^{-1}$. For an antenna with an effective electrical height of 1 m these powers are -27 dBm and +13 dBm respectively. This suggests that an ideal HF receiver, with a noise figure of 16 dB (-158 dBm/Hz noise floor) should provide a BDR of >170 dB. In actual fact, because signal and more particularly noise levels are generally higher at night [ITU, 27] a reduced BDR can normally be tolerated. A high performance, super-heterodyne receiver was measured (see Appendix C) as having a BDR of 148 dB.

The largest typical signal powers that a receiver may be subjected to due to a single emitter may be determined by considering the power received from a close-by transmitter – i.e. one within ground-wave range². The received power is given by:

$$P_R(\text{dBm}) = P_T(\text{dBm}) + G_T(\text{dB}) + G_R(\text{dB}) - L(\text{dB}) \quad (5-4)$$

where:

P_T is transmit power;

G_T is the effective transmit antenna gain;

G_R is the effective receive antenna gain; and

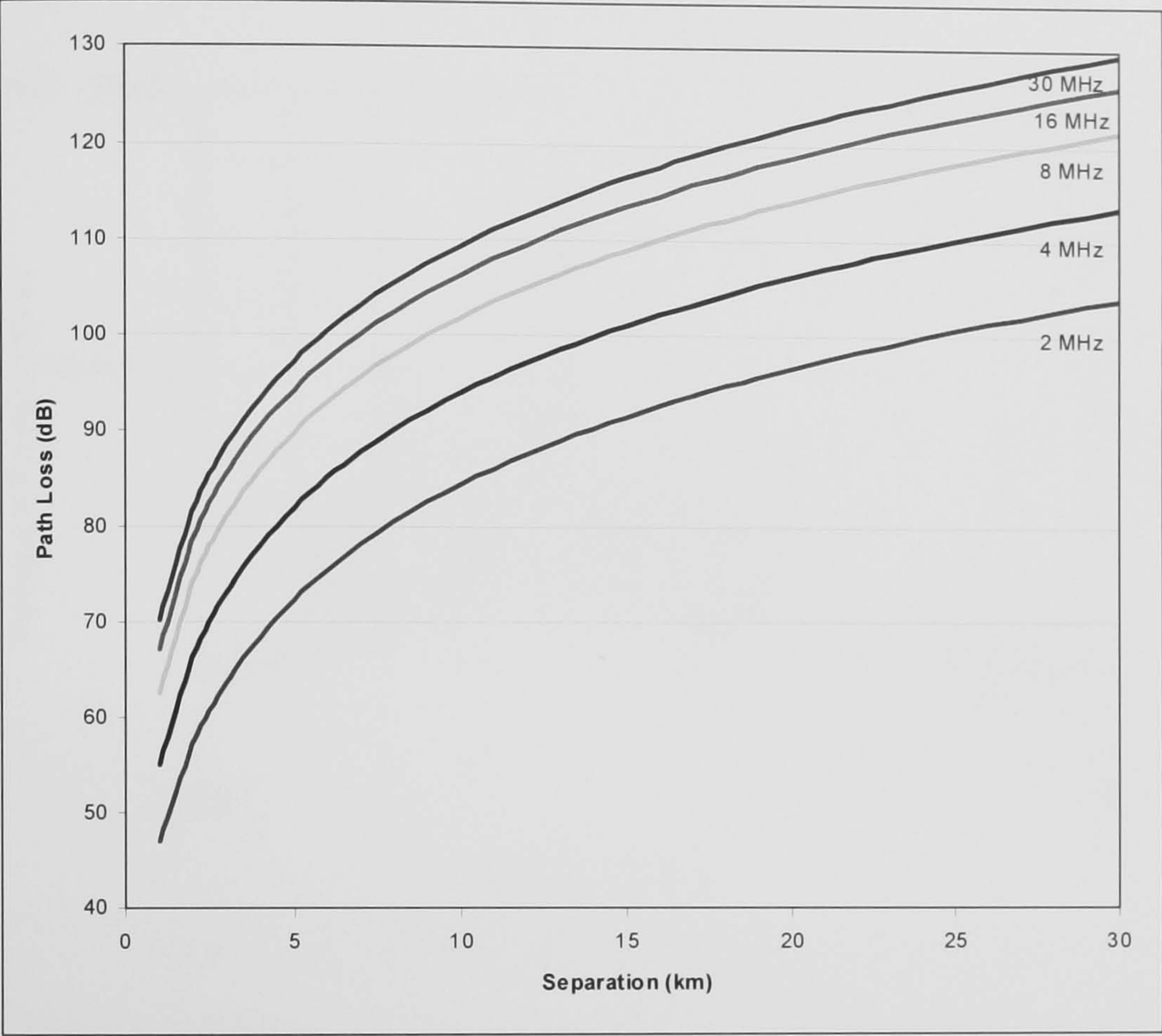
L is the propagation path loss.

Figure 5-9 is a plot of ground wave path loss (transmitter-receiver isolation) versus separation distance for a range of frequencies within the HF band. It was generated using GRWAVE [ITU, 6]. For a powerful 500 kW (+87 dBm) 2 MHz transmitter

¹ Lott's work directly measured the total power in the HF band using a band-pass filter and true RMS power meter connected to a broadband HF antenna. His measurements were made using large Wullenweber circularly disposed antenna arrays (CDAAs) located in Europe and the Pacific.

² This excludes the gratuitous case of a co-located (co-sited) transmitter. When co-sited simultaneous operation (SIMOP) is required, this must be treated as a special case in which co-operative working measures, such as the use of SIMOP filters (on both transmitter system and receiver) and enforced minimum frequency separations must be applied.

feeding the equivalent of an isotropic antenna¹ the path loss graph indicates that at 25 km the worst case signal received using an isotropic antenna would be no greater than -15 dBm. At higher frequencies or with additional attenuation due to terrain masking, substantially lower receive signal powers will be observed.



Propagation over smooth, medium-dry ground ($\sigma=0.001$ S/m, $\epsilon=15$), vertical polarisation, Tx antenna height=30 m.

Figure 5-9 Path Loss versus Separation Distance

A wideband receiver must be capable of simultaneously receiving both these strong signals and weak signals close to the noise floor. This ability is the instantaneous dynamic range of the receiver. Assuming a maximum signal power of -15 dBm this implies an instantaneous dynamic range of 143 dB for a receiver with NF=16 dB. Assuming that the signals are both modulated (which is highly likely) then, for NF=16 dB and a 3 kHz bandwidth, this equates to a dynamic range of 108 dB (-123 dBm to -15 dBm).

¹ Large antennas such as horizontally polarised curtain arrays with large peak gains (~20 dB) are widely used by broadcasters. However, the combination of much reduced gain at low elevation angles and the rapid attenuation of horizontally polarised ground wave signals means that, at the shorter ranges being considered here, the worst case is probably best represented by considering vertically polarised emissions from an isotropic antenna.

As a counter-poise to the extreme situations discussed above, Figure 5-10, is a plot of the power measured across the HF band using a spectrum analyser [GEC, 99] illustrating typical signal power distributions. It can be seen that in this snapshot the highest power signal only reaches -35 dBm.

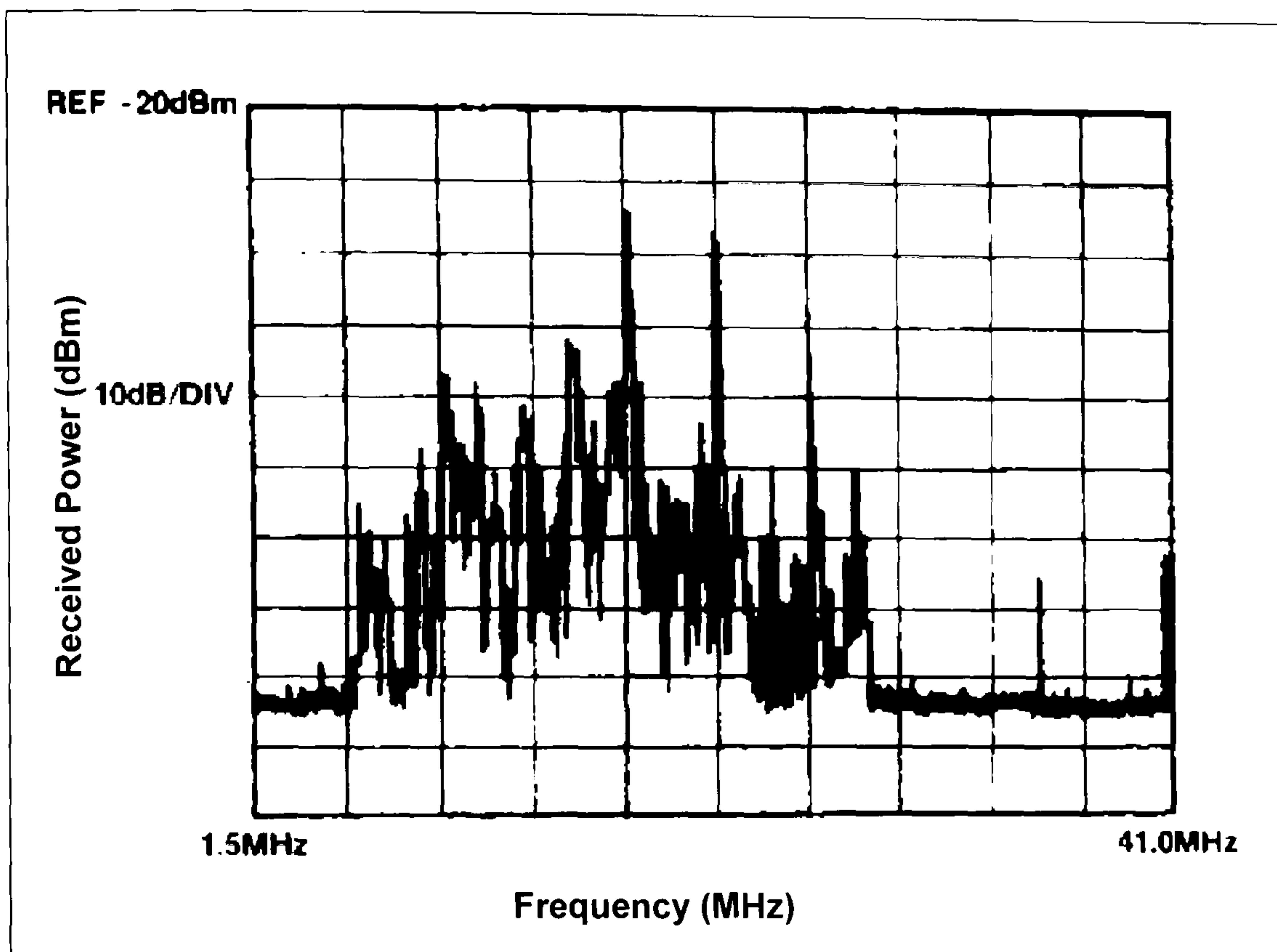


Figure 5-10 Snapshot of Measured Signal Power in HF Band [GEC, 99]

Large signal strengths at the input of a receiver can also be generated by nearby (co-sited) transmitters. When receive antenna gain is taken into consideration peak powers as high as +20 dBm may be present at the input of an HF receiver in extreme co-site cases. When increased blocking performance is needed (e.g. where co-site operation is required) sub-octave band-pass filters (also known as simultaneous operation, SIMOP, filters) may be employed. These provide additional selectivity at the receiver front end, preserving sensitivity in the selected sub-band and reducing interference (which could cause blocking) and inter-modulation distortion due to other frequencies. In a wideband digital receiver sub-octave filtering, whilst it would have the same benefits, has the great disadvantage that it removes the receiver's ability to simultaneously receive signals from frequencies across the whole HF band.

5.3.3 Selectivity

Selectivity is a measure of a receiver's ability to reject signals outside of the frequency range of interest. In a conventional superhet design this takes two forms. A (pre-selector) filter is used to reject all out-of-band signals (images) that could be mixed to the same first IF frequency as the wanted signal. Such a filter has been measured to provide 110 dB rejection in a high quality conventional HF receiver (see Appendix C). Note that this filter is analogous to the anti-aliasing filter required in a wideband direct sampling receiver. In each IF stage of a traditional receiver design narrow-band crystal or mechanical filters are used to reject signals outside the channel of interest. An aggregate selectivity of ≥ 110 dB is typical (Figure 5-11). A significant disadvantage of these filters, especially for some data communications waveforms, can be the large group delay variations due to the sharp transitions required for good selectivity. In a digital receiver the required selectivity is provided by digital filtering which can utilise linear phase filter structures.

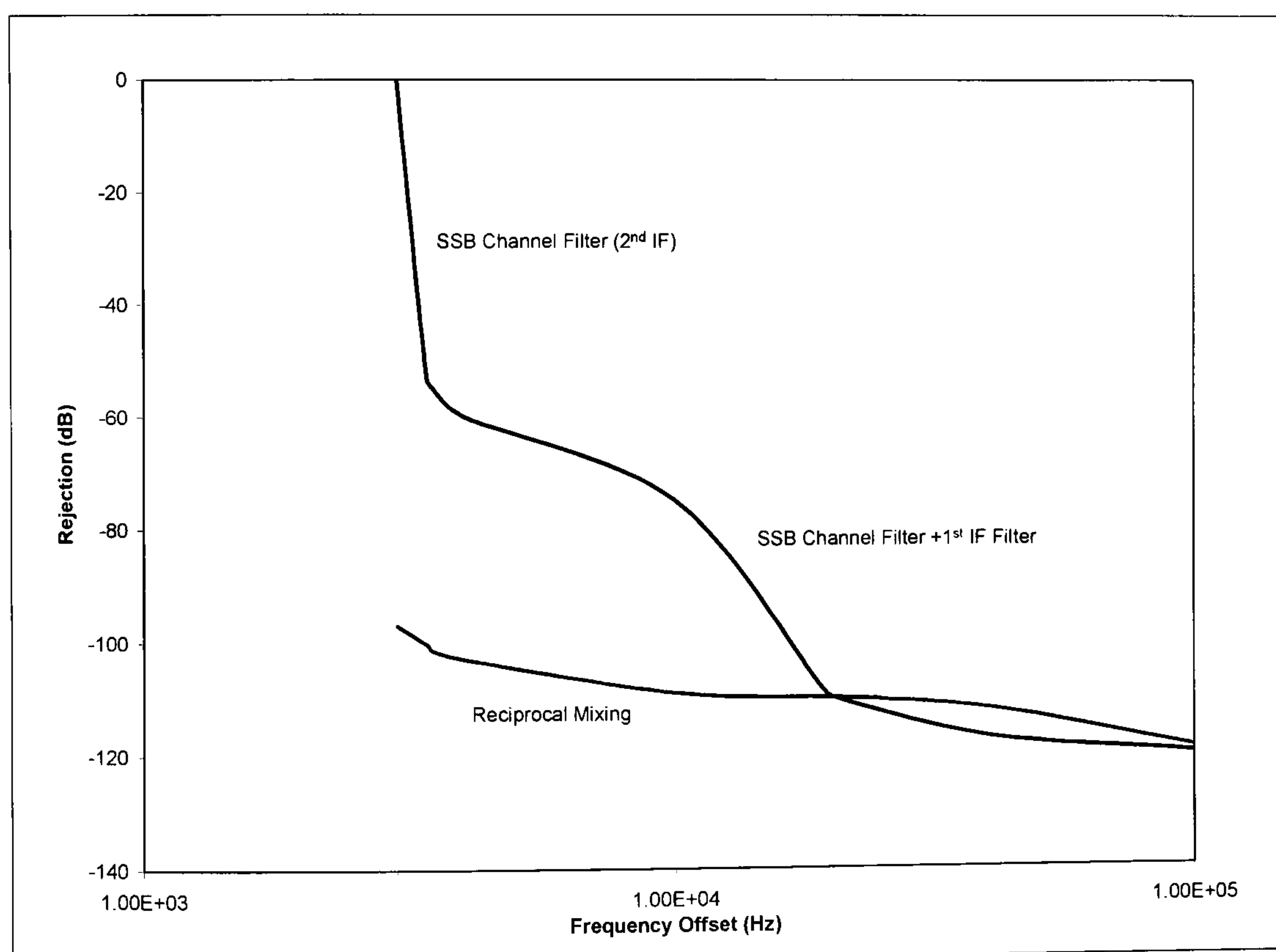


Figure 5-11 Typical Narrowband Superhet HF Receiver Composite Filter Characteristics [after Pearce, 100]

In a receiver employing frequency translation another limitation is due to reciprocal mixing (Figure 5-12). This is where the finite phase noise of the LO signal causes strong signals that are close in frequency to a weak wanted signal to be mixed into the

receiver pass-band (Figure 5-11). Values for phase noise in a high performance HF receiver first local oscillator are given later in Table 5-1.

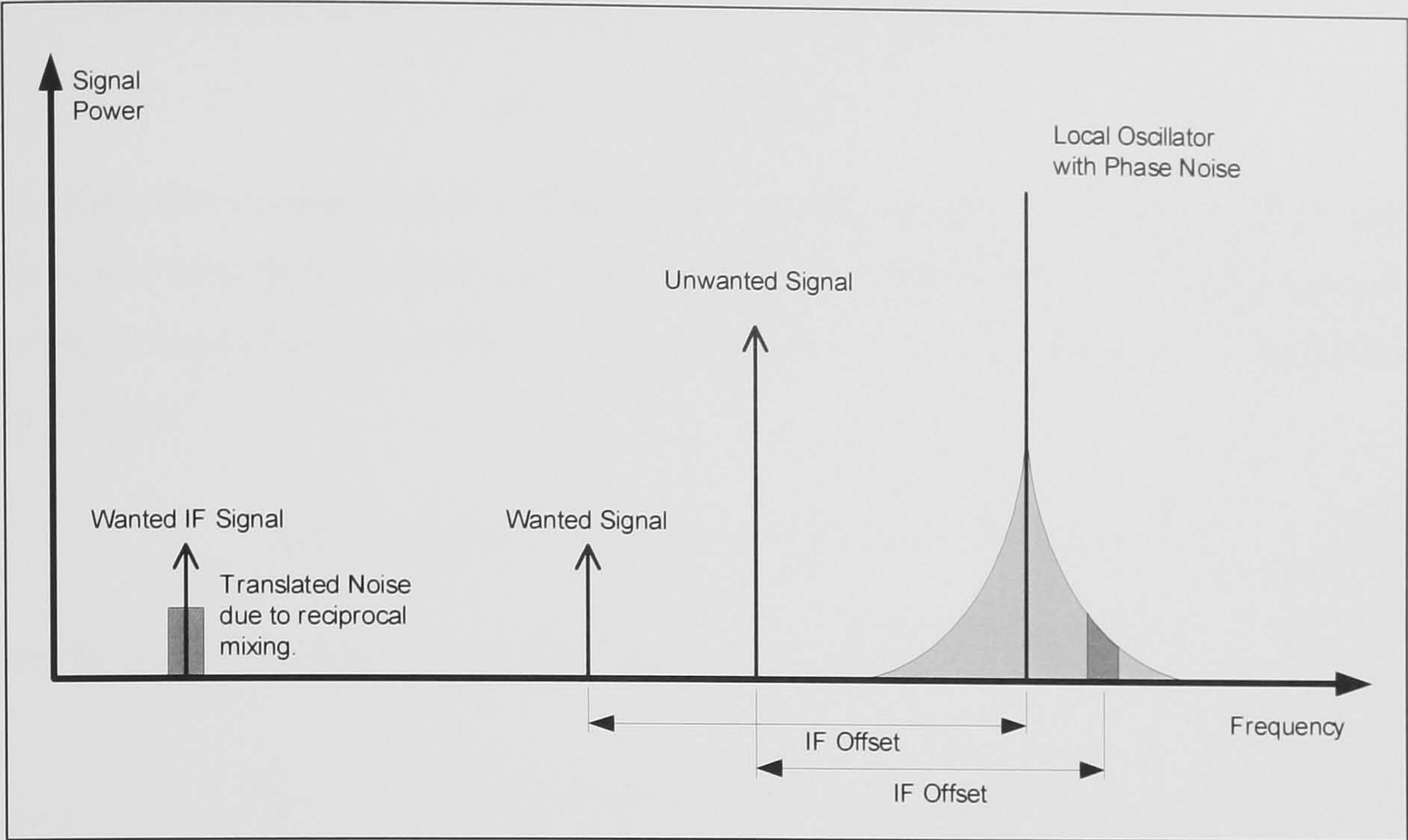


Figure 5-12 Reciprocal Mixing in a Receiver with Frequency Translation

5.3.4 Inter-Modulation Products, Harmonic Suppression and SFDR

When two tones with frequencies f_1 and f_2 ($f_2 > f_1$) are applied to a non-linear device, inter-modulation distortion (IMD) signals are generated [Fisk, 97]. The most significant are the second order products ($2f_1, 2f_2, f_1 \pm f_2$) and third order products ($3f_1, 3f_2, 2f_1 - f_2$ and $2f_2 - f_1$). The third order inter-modulation distortion (IMD) products, are of particular concern because they increase by 3 dB for every decibel increase in the level of the test tones. The input referenced third order intercept point ($IP3_{IN}$) is the notional input signal level at which the IMD products are at the same level as the outputs produced by the wanted tones. High quality conventional HF receivers have an $IP3_{IN}$ of $\geq +20$ dBm (+30 dBm is considered excellent). By measuring the IMD (dBc), produced by two equal power input tones of power P_{IN} (dBm), $IP3_{IN}$ can be determined (see Appendix D and [Kundert, 101]):

$$IP3_{IN} = \frac{1}{2} IMD + P_{IN} \text{ dBm} \tag{5-5}$$

Many manufacturers specify IMD performance in terms of the third intercept point referenced to the output of the device: $IP3_{OUT}$. Where the gain of a receiver is G , the intercept point referenced to the input and output of a receiver are related:

$$IP3_{IN} = IP3_{OUT} - G \quad (5-6)$$

Spurious free dynamic range (SFDR) is commonly defined as the signal input range from the noise floor to the largest signal level that will not generate 3rd order spurious products above that noise floor. In an analogue receiver SFDR can therefore be defined as follows:

$$SFDR = \frac{2}{3} [IP3_{IN} - 10 \log_{10} B - NF + 174] \quad dB \quad (5-7)$$

and the maximum spurious free input signal level, P_{MAX} :

$$P_{max} = \frac{1}{3} [2IP3_{IN} + 10 \log_{10} B + NF - 174] \quad dBm \quad (5-8)$$

A 3 kHz bandwidth receiver with a 14 dB NF and +25 dBm $IP3_{IN}$ thus has a SFDR of 100 dB.

During the practical work undertaken for this thesis the importance of 2nd order IMD performance, which is often ignored, became increasingly clear. They are an important consideration in HF equipments (as opposed to higher frequency systems) because the products can fall in-band where they may not be able to be subsequently filtered out (e.g. in a receiver front end). Amplifiers or mixers in conventional receivers, protected by narrowband filters, are largely immune to these 2nd order products because the signals that would interact to cause them are sufficiently removed in frequency that they are rejected by filtering. Hence they may have high 2nd order intercept points ($IP2_{IN}$). However components subject to wideband signals, such as front-end RF amplifiers and the first mixer in a receiver are vulnerable to producing 2nd order IMD products and harmonics that may fall within the bandwidth of the selected receive frequency. $IP2_{IN}$ is given by (see Appendix D):

$$IP2_{IN} = P_{IN} + IMD \quad dBm \quad (5-9)$$

The relative impact of 2nd and 3rd order IMD products has been analysed using equations (5-5) and (5-9). Figure 5-13 shows the level of IMD products generated by

two input signals as a function of the input signal level for a range of $IP2_{IN}$ and $IP3_{IN}$. The graph demonstrates the importance of considering both $IP2_{IN}$ and $IP3_{IN}$ to achieve an acceptable overall level of performance. High performance HF receivers will typically have $IP2_{IN} \geq +60$ dBm ($>+70$ dBm is considered excellent).

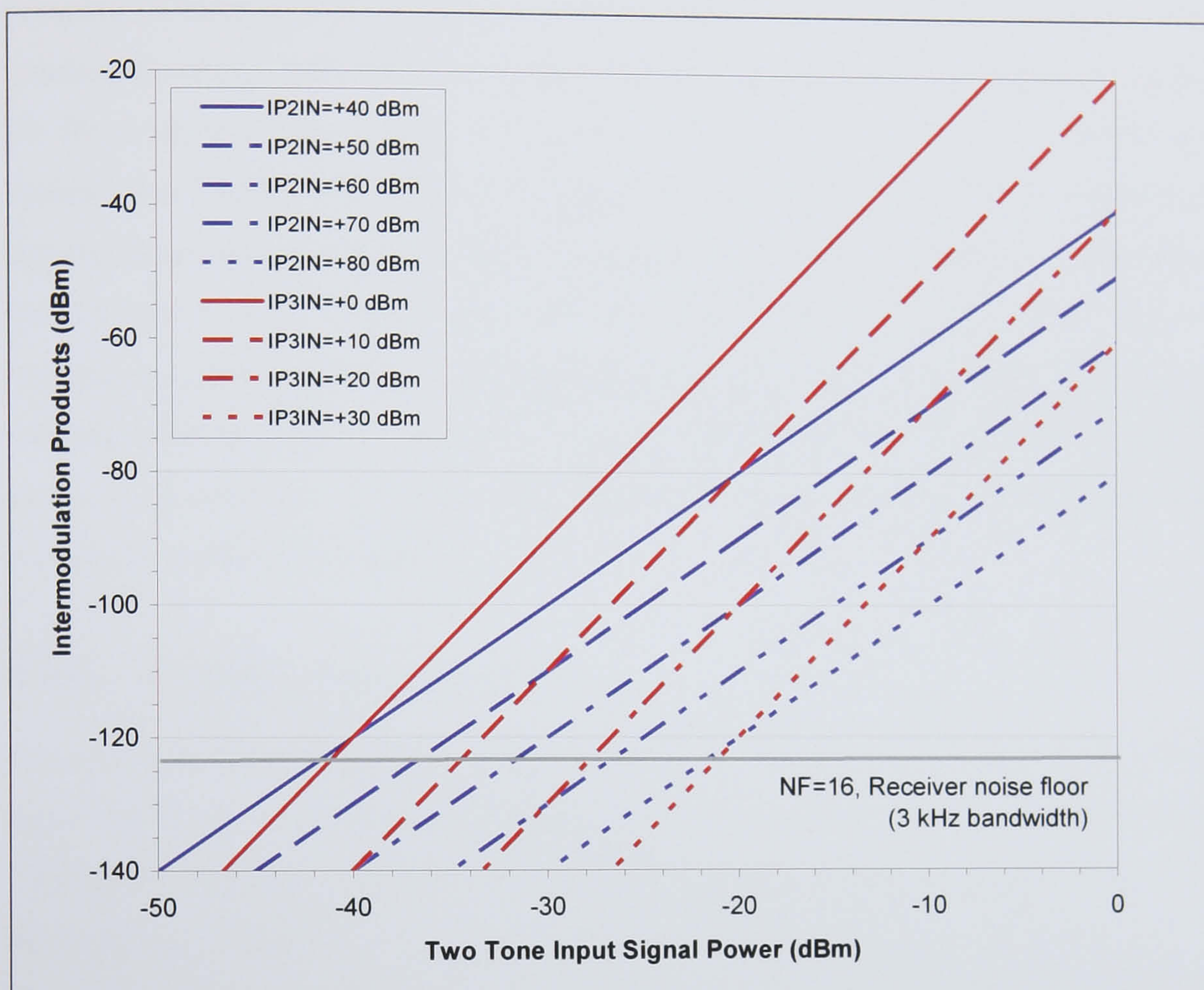


Figure 5-13 2nd and 3rd Order Intermodulation Product Levels versus Two Tone Input Power

Harmonic suppression (particularly of 2nd and 3rd order harmonics) is also particularly important within the front-end of an HF receiver. This is because the HF band spans almost four octaves and so harmonics of signals up to 15 MHz will fall in-band. The requirements for harmonic suppression are equivalent to those for IMD. The extent to which harmonics are suppressed is very much a function of circuit design. For example components such as amplifiers may be designed to provide effective 2nd harmonic cancellation (e.g. using a push-pull architecture [Dye, 102 p114] or linearisation techniques).

5.3.5 Practical Impact of Receiver Intermodulation Products

The discussion above has focused on the level of IMD product suppression achievable within receivers. The impact of intermodulation products on practical communications requires some further consideration. Given a particular receiver performance, the presence of harmful IMD products can be shown to be a probabilistic function of the number of signals in the HF band with sufficient power to generate them and whether the frequencies of those signals are such that a product will be in-band of the wanted transmission [Miller, 103]. Given sufficient information on the occurrence statistics of signals (frequency, power) in the HF band, such an argument can be used to determine the required dynamic range for an acceptable probability of being IMD free. The HF occupancy studies undertaken by Gott [e.g. Gott, 30] may be applicable for such an analysis although it is not clear whether measurement data on the strength of signals above a threshold of 100 $\mu\text{V/m}$ (the highest threshold available in their published occupancy models) was retained.

5.3.6 Spurious Signal Products

In addition to IMD, receivers are also subject to other internally generated spurious signals such as unwanted mixer products, local oscillator leakage, harmonics etc. Typical receiver specifications call for >99% of 3 kHz channels to be free of spurious above the noise floor.

5.4 HF Transmitter Performance Requirements

A signal to be transmitted must be adequately filtered to constrain its bandwidth: this is typically specified such that >99.9% of the power is contained in the allocated bandwidth (e.g. [ITU, 105], [NATO, 106]). Unwanted emissions (IMD, harmonics etc) must also be minimised. Typical (minimum) requirements are for harmonic outputs to be -40 dBc and IMD -65 dBc. Wideband noise generated in the transmitting system must be kept to a sufficiently low level such that it does not compromise the sensitivity of nearby receivers. A typical 500 W power amplifier might have a gain of 40 dB which is sufficiently large that even thermal noise at its input would result in a transmitter noise power of -134 dBm/Hz (-99 dBm in 3 kHz). In situations where a

multi-channelling HF transmitter exciter feeds a wideband power amplifier (PA) little or no additional filtering can be applied and PA specifications are particularly onerous.

5.5 A Direct Sampling Digital HF Receiver

The following sections presents a novel direct sampling wideband digital HF receiver architecture and analyse the performance that a practical implementation may be expected to provide. The next chapter presents measurements made on a prototype receiver, constructed as a part of a wideband digital transceiver which is presented in Chapter 7. This chapter concentrates on the characteristics and likely attainable performance. Figure 5-14 is a diagram of the architecture investigated. The following sections consider the performance of each of the key components of the receiver and then its overall performance.

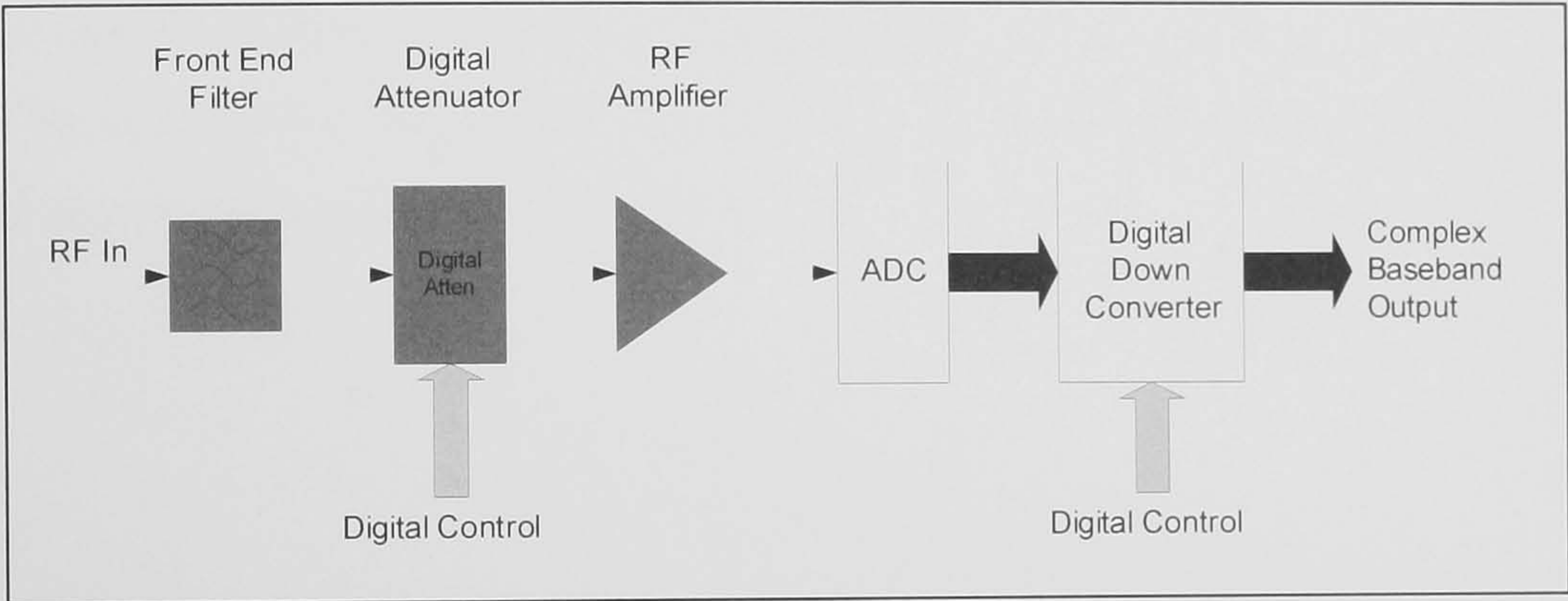


Figure 5-14 Wideband Direct Sampling Digital Receiver

5.6 Front End Filter

The front-end filter provides the direct sampling digital receiver with the required high order Nyquist filtering to prevent aliasing. It also provides secondary lightning protection and protection from over-voltage and over-current.

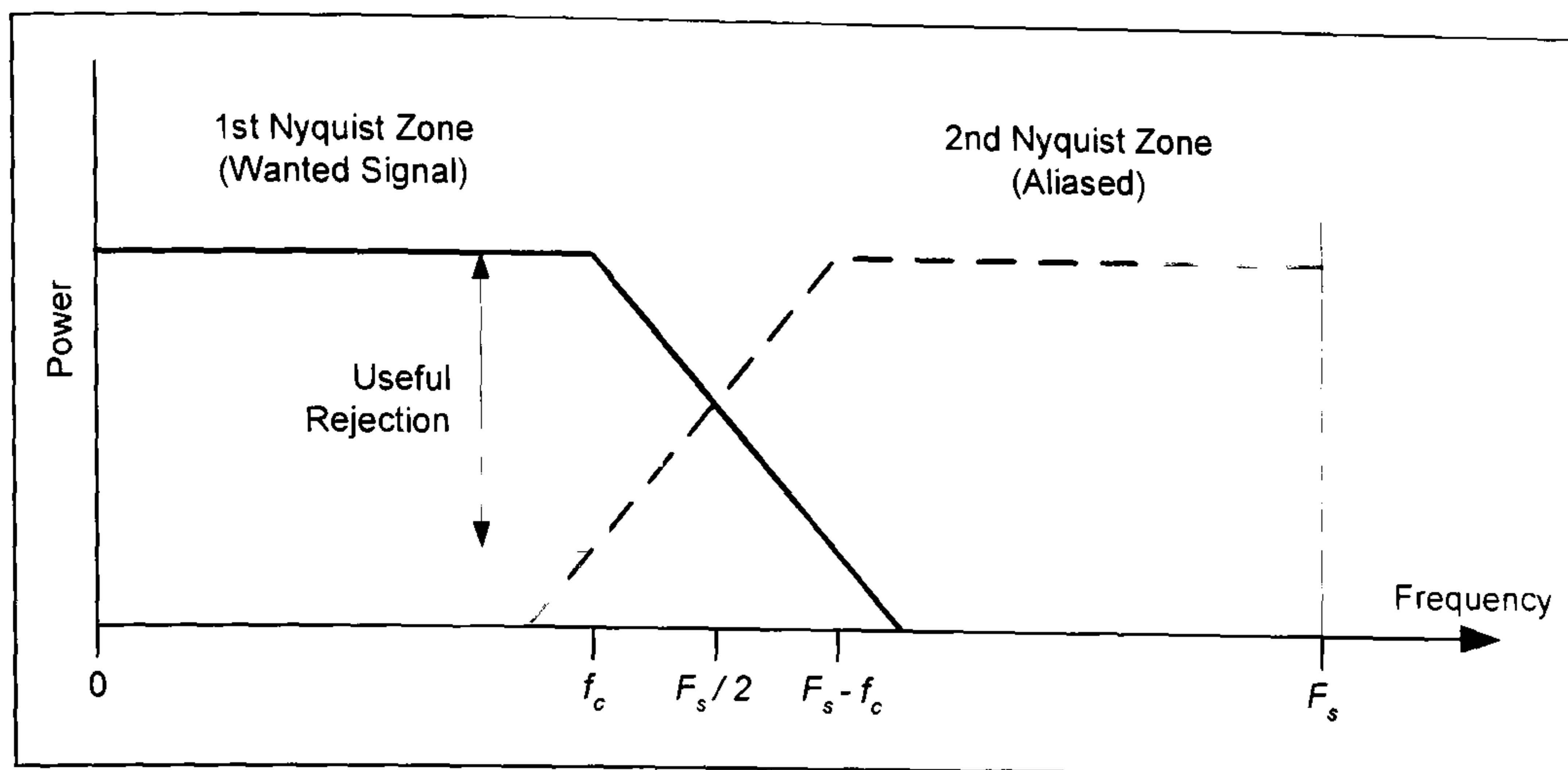


Figure 5-15 Front End Anti-Aliasing Filter Performance Requirement

The choice of filter cut-off frequency is made such that, taking the filter's transition region into consideration, no signals beyond the cut off frequency will cause in band aliasing (illustrated in Figure 5-15). If the normalised transition ratio of the filter (lowest stop-band frequency divided by highest pass-band frequency) is ω , and making use of the symmetry of the aliasing process, then the relationship with the maximum unaliased receiver frequency, f_c , is given by:

$$\omega = \frac{f_{STOP}}{f_{PASS}} \leq \frac{F_s - f_c}{f_c} \quad (5-10)$$

where

F_s is the digitiser sampling rate.

The minimum acceptable filter performance is therefore given by:

$$\omega = \frac{F_s}{f_c} - 1 \quad (5-11)$$

The low pass filter is required to ideally provide 120 dB of attenuation for signals outside the operating band in order not to limit the receiver's performance. Whilst this is an apparently challenging requirement it is essentially the same requirement as that of the image reject filter in a conventional narrowband HF receiver. However, limitations in the maximum sampling rate of the ADC may impose an additional requirement to achieve a narrow transition band which is challenging to implement.

5.7 Digitally Controlled RF Amplifier

The digitally controlled RF amplifier is required to provide sufficient gain to match the received signal dynamic range with that of the ADC. It will be shown (in the next section) that the dynamic range obtainable from currently available ADCs is insufficient to fully meet the needs of an ideal HF receiver. This limitation is analogous to the blocking performance in conventional narrowband receivers and it will be shown that comparable (indeed equal) performance to a high quality narrowband receiver can be achieved.

The RF amplifier in a wideband receiver must have a noise figure low enough to provide the required receiver sensitivity and sufficient linearity to provide acceptable harmonic and IMD suppression. Harmonic and 2nd order IMD is a particular concern for HF receiver front-ends as, being multi-octave, many of these products will fall in-band. The proposed architecture employs a digitally controlled RF attenuator followed by a fixed gain amplifier. At HF the insertion loss of the attenuator ahead of the amplifier can be tolerated and has a number of advantages. In a strong signal environment, where the signal may have to be attenuated in any case (to match the ADC dynamic range), increasing front-end attenuation reduces IMD and harmonic products (increasing the effective receiver intercept points).

5.8 Analogue-to-Digital Converter (ADC) Performance

The performance that a wideband digital receiver can achieve is highly dependent on the performance of the digitiser (ADC). This section considers the key characteristics that determine achievable digitiser performance and summarises work done to quantify the performance that can be achieved in a practical wideband digital HF receiver implementation.

The Analog Devices AD6644 [Analog, 107] is a new, high performance ADC with 14-bit precision and a maximum sampling rate of 65 MSPS. This device has been used in the prototype digital receiver presented in the next chapter. The following analysis and discussion of practically achievable digitiser performance is illustrated using information on the AD6644's characteristics.

5.8.1 ADC Signal-to-Noise Ratio (SNR) Performance

When an analogue signal is sampled by a digitiser with finite quantisation intervals it can readily be shown that the achievable signal-to-quantisation noise ratio (SQNR) is given by [e.g. Proakis, 108 p37]:

$$SQNR(dB) = 10 \log_{10} \left(\frac{3}{2} \cdot 2^{2N} \right) = 1.76 + 6.02N \quad (5-12)$$

where N is the number of ADC bits. For a 14-bit converter, such as the AD6644, this gives $SQNR \approx 86$ dB which is a theoretical bound on ADC SNR. The maximum SNR that a practical ADC device can achieve is principally limited by its analogue noise performance, dynamic non-linearities (DNLs) in the conversion process and sampling clock aperture jitter. Equation (5-12) can be modified to include their impact [Analog, 107]:

$$SNR(dB) = 1.76 - 20 \log_{10} \left[\left(\frac{2\sqrt{2}b_{RMS_{noise}}}{2^N} \right)^2 + (2\pi F_A t_{jrms})^2 + \left(\frac{1+\varepsilon}{2^N} \right)^2 \right]^{\frac{1}{2}} \quad (5-13)$$

where

F_A is the analogue input frequency;

t_{jrms} is the ADC sampling clock aperture jitter;

ε is the average DNL of the ADC (~ 0.41 for AD6644);

$b_{RMS_{noise}}$ is the equivalent RMS thermal noise in ADC LSBs (~ 1.2 for AD6644); and

N is the number of ADC bits.

The SNR of the ADC can be easily converted into an equivalent noise figure:

$$NF_{ADC}(dBm) = P_{Fullscale}(dBm) - SNR(dB) - 10 \log_{10} \left(\frac{F_S}{2} \right) + 174 \quad (5-14)$$

where

NF_{ADC} is the ADC noise figure; and

$P_{Fullscale_{RMS}}$ is the ADC full scale input power.

5.8.2 ADC Noise Performance and Noise Figure

Equation (5-12) gave a bound on achievable SQNR determined purely by the number of ADC quantisation intervals (SQNR \approx 86 dB for a 14-bit converter). A more practical measure of the achievable ADC SNR is to consider the ratio between the largest input signal and the internally generated noise floor of the ADC. This may be written:

$$SQNR(dB) = 1.76 + 20 \log_{10} \left(\frac{V_{fullscale_ADC}}{V_{noise}} \right) \quad (5-15)$$

The internal noise generated within the AD6644 is equivalent to 1.2 least significant bits (LSBs) peak-to-peak thus the maximum achievable SQNR is:

$$SQNR(dB) = 1.76 + 20 \log_{10} \left(\frac{2^{14}}{2^{1.2}} \right) = 78.8 \text{ dB} \quad (5-16)$$

5.8.3 Sampling Clock Jitter (Phase Noise)

When an analogue signal is sampled by an ADC any variation in the instantaneous sampling instant will translate directly into a change in the quantised amplitude (illustrated in Figure 5-16). The small random changes in the sampling instant from sample-to-sample are termed ‘aperture uncertainty’ or ‘aperture jitter’ and can have a marked impact on ADC performance.

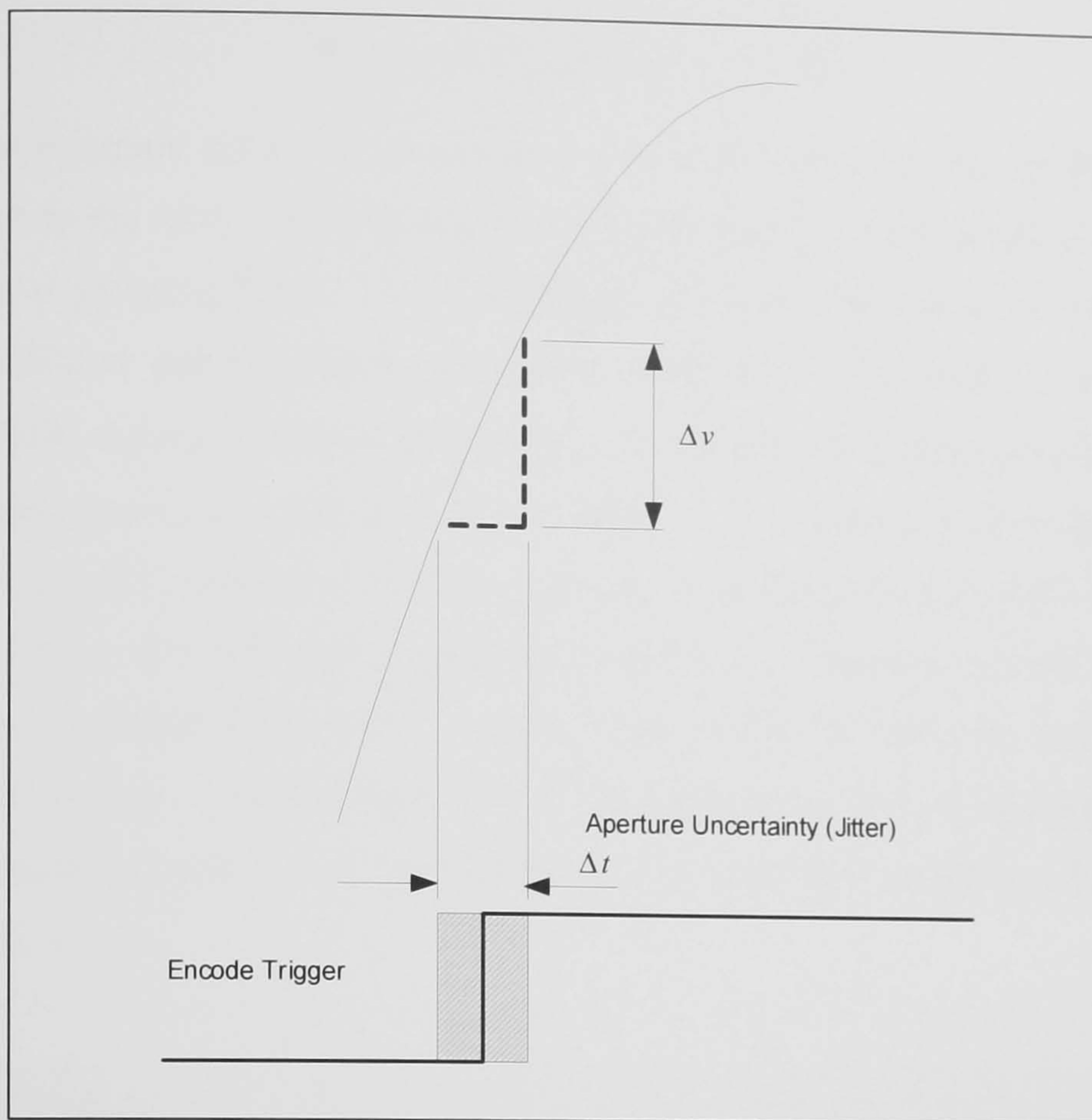


Figure 5-16 Error in Sampling Amplitude Due to ADC Aperture Uncertainty (Jitter)

Given a sine wave of frequency, F_A , its voltage is:

$$v = A \sin(2\pi F_A t) \quad (5-17)$$

The gradient (slew rate) is given by the first derivative:

$$\frac{dv}{dt} = A 2\pi F_A \cos(2\pi F_A t) \quad (5-18)$$

At the nominal sampling instant, $t=0$, the signal slew rate is given by:

$$\frac{\Delta v}{\Delta t} = \frac{dv}{dt} = A 2\pi F_A, \quad t = 0 \quad (5-19)$$

The error voltage at the sampling instant is the jitter, t_j , multiplied by the signal slew rate:

$$v_{ERROR} = \frac{\Delta v}{\Delta t} t_{JITTER} = A 2\pi F_A t_j \quad V \quad (5-20)$$

By considering a full scale input waveform it is then straight forward to write the theoretical SNR limitation imposed on the ADC due to RMS sampling jitter:

$$SNR = -20 \log_{10} \left(2\pi F_A t_{j_{RMS}} \right) \text{ dB} \tag{5-21}$$

This is an important result. In particular it should be noted that the available SNR is limited not by the ADC sampling rate but by the frequency of the signal being sampled and the total sampling jitter. The overall jitter is due to that present on the sampling clock (oscillator) and to aperture uncertainty within the ADC itself. For the 14-bit AD6644 ADC the nominal SNR is 75 dB ($F_s \leq 65$ MSPS) for 1st Nyquist zone sampling and internal aperture uncertainty is 200 ps RMS. The predicted ADC SNR (including the effects of ADC internal noise floor, dynamic non-linearities and jitter) is plotted in Figure 5-17 for different signal input frequencies as a function of RMS jitter. To achieve the specified 75 dB SNR for input signals up to 30 MHz the sampling clock RMS jitter must be no worse than ~400 fs. It can be seen that for applications where higher frequency signals are to be sampled (e.g. by band-pass sampling) clock purity is much more critical.

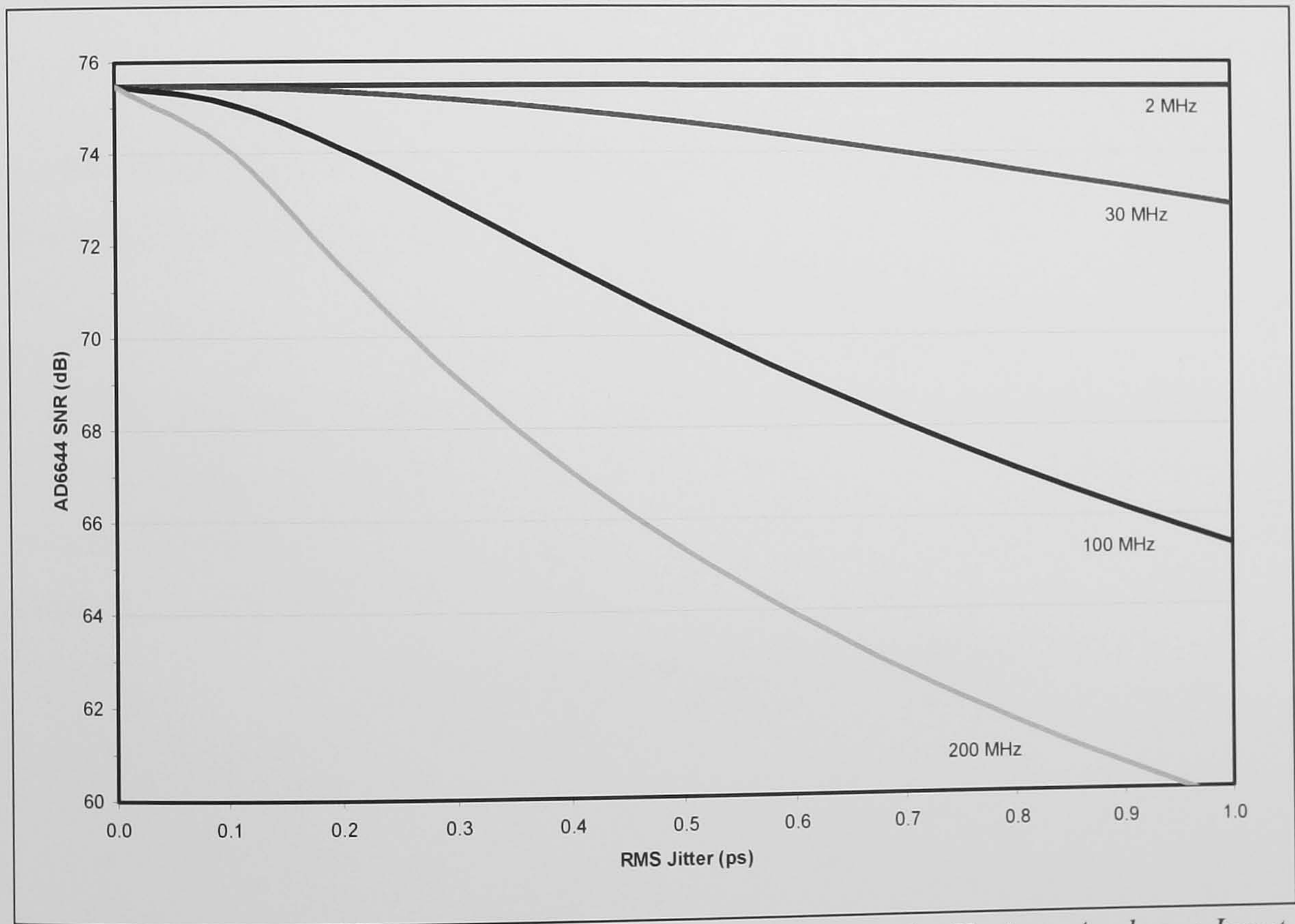


Figure 5-17 Predicted AD6644 SNR versus Clock Jitter for Various Analogue Input Frequencies

With certain assumptions the required jitter performance can be converted into a phase noise specification since phase jitter is essentially the integral of phase noise [Robins,

109]. If the noise is assumed to be white, ϕ_{RMS} is RMS phase jitter and F_A is the frequency under consideration, then:

$$\phi_{RMS} = 2\pi F_A t_{j_{RMS}} \quad \text{radians}$$

(5-22)

or

$$t_{j_{RMS}} = \frac{\phi_{RMS}}{2\pi F_A} \quad \text{seconds}$$

(5-23)

If the noise is assumed to be white then:

$$\phi_{RMS} = \sqrt{\frac{N_o B}{C}} \quad \text{radians}$$

(5-24)

where

- N_o is the noise power density in the specified bandwidth
- B is the noise bandwidth
- C is the oscillator output power.

Further, ϕ can be converted into an equivalent noise power spectral density, N_0 , relative to the oscillator signal power:

$$N_0 = 10 \log_{10} (\phi_{RMS}^2) - 10 \log_{10} B \quad \text{dBc / Hz}$$

(5-25)

The phase noise specification of a good quality synthesised local oscillator, as might be used in a high performance traditional HF receiver, is given in Table 5-1. An acceptable approximation is to interpolate these points with straight line segments as plotted in Figure 5-18.

Offset (Hz)	Phase Noise (dBc/Hz)
1 Hz	-75
10 Hz	-100
100 Hz	-125
1 kHz	-135
≥1 MHz	-160

Table 5-1 Phase Noise of a High Quality HF Synthesiser

Using the formulae derived in Appendix E it is possible to convert between a phase noise specification and an integrated phase noise and thence an RMS jitter by summing (integrating) the phase noise contribution for each line segment in turn. The phase noise

specification in Table 5-1 produces an integrated (double sided) phase noise of -77 dBc or an equivalent RMS jitter of 380 fs.

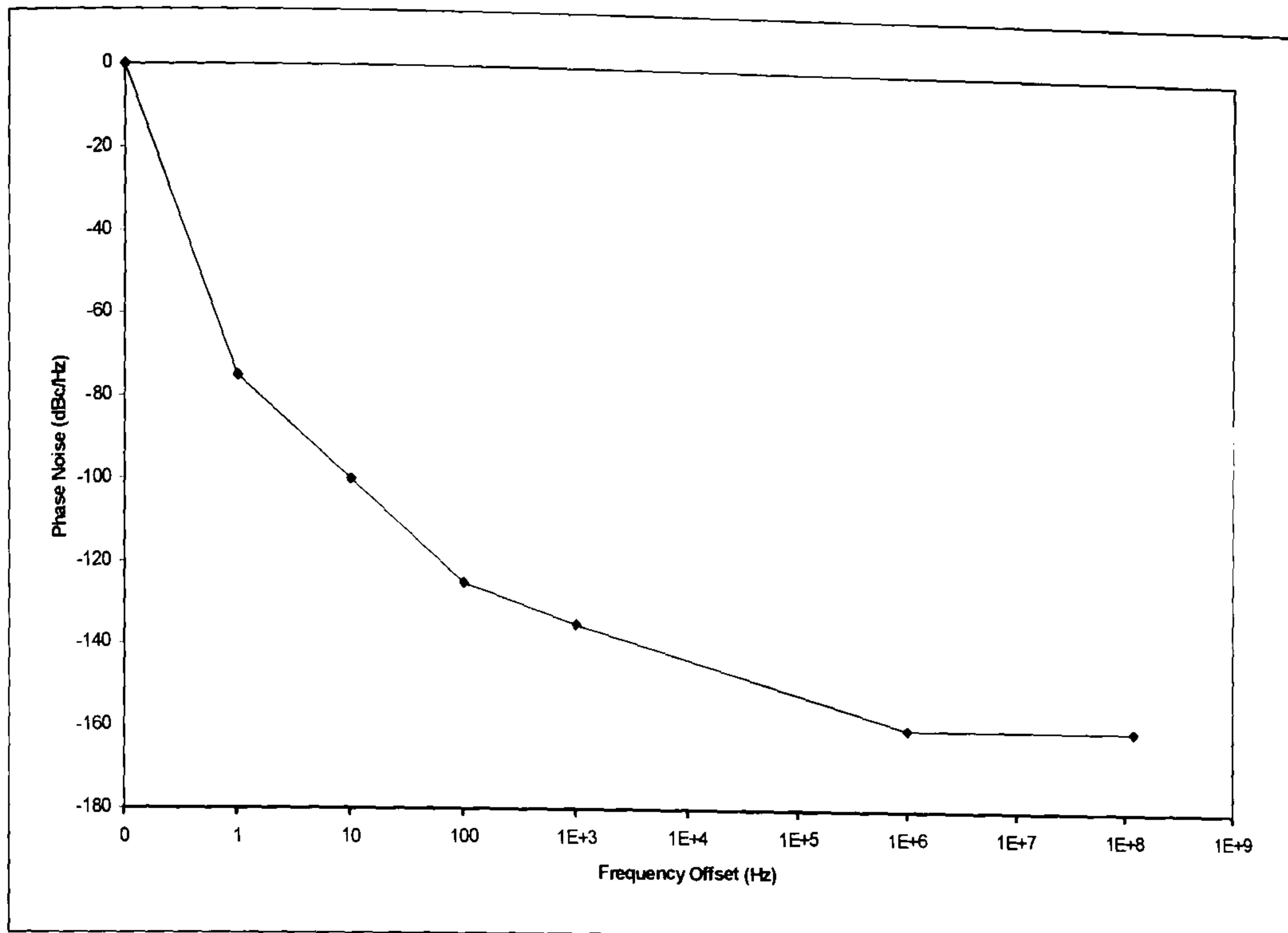


Figure 5-18 Typical High Quality Local Oscillator SSB Phase Noise Specification

Therefore with careful design a high quality crystal based oscillator can provide an adequate sampling clock with good wideband phase noise performance.

5.8.4 Spurious Free Dynamic Range and ADC Non-linearities

In an analogue receiver SFDR is generally determined by NF and $IP3_{IN}$ as previously discussed. Unfortunately, in a wideband digital receiver, the ADC sampling process can introduce much more restrictive SFDR limitations [Wepman, 89]. Differential non-linearities (DNLs) in a multi-stage ADC lead to the generation of harmonics and aliased harmonics of the input signal [Analog, 110], [Brannon, 111]. For the AD6644 ADC, spurious products limit SFDR to -90 dBFS (dB relative to full-scale) for a single tone full scale input. Worse still, unlike SFDR in a conventional receiver which is bounded by 3rd order IMDs, ADC spurious products do not generally reduce as the input signal level is reduced and so the impact is much greater. Where an ADC in a receiver is used to digitise a single signal the receiver analogue gain may be adjusted so that operation is always within the SFDR and thus principally limited by the converter SNR. However, in a wideband digital receiver (digitising multiple channels and applying selectivity using digital filtering), ADC SFDR is a significant performance limitation. Here there

is a need to be able to detect and process very weak signals in the presence of much larger ones.

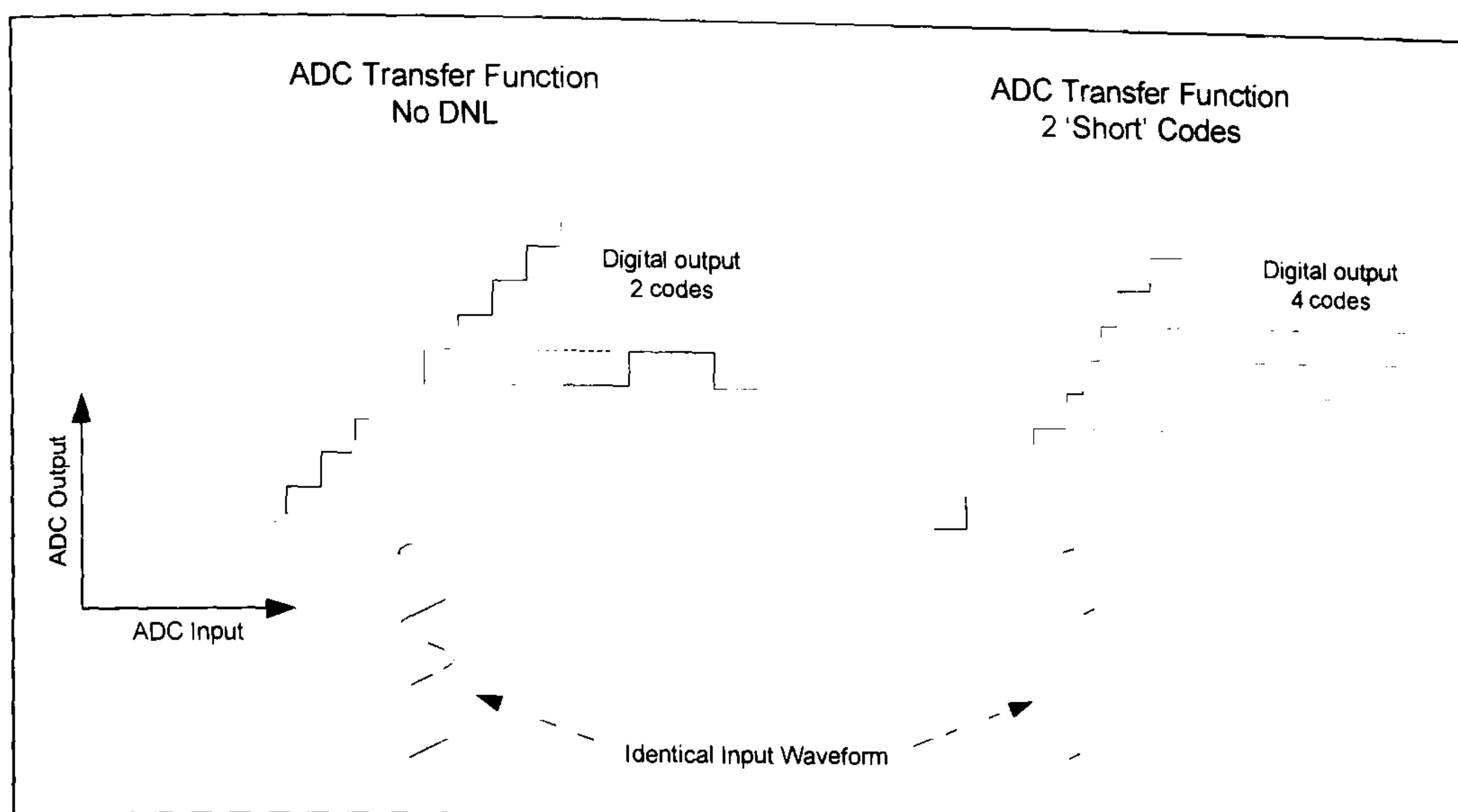


Figure 5-19 ADC Quantisation Errors Due to DNLs [after Brannon, 111]

The spurious due to DNLs is due to the repetitive use of a non-linear region of an ADC's non-linear transfer function (illustrated in Figure 5-19). In a high performance multi-stage sub-ranging ADC, such as the AD6644 (Figure 5-20), the principal cause of DNLs is due to small mismatches between the stages. Analysis by the manufacturers has shown that in AD6644 devices, the main cause is a mismatch between the first and subsequent stages.

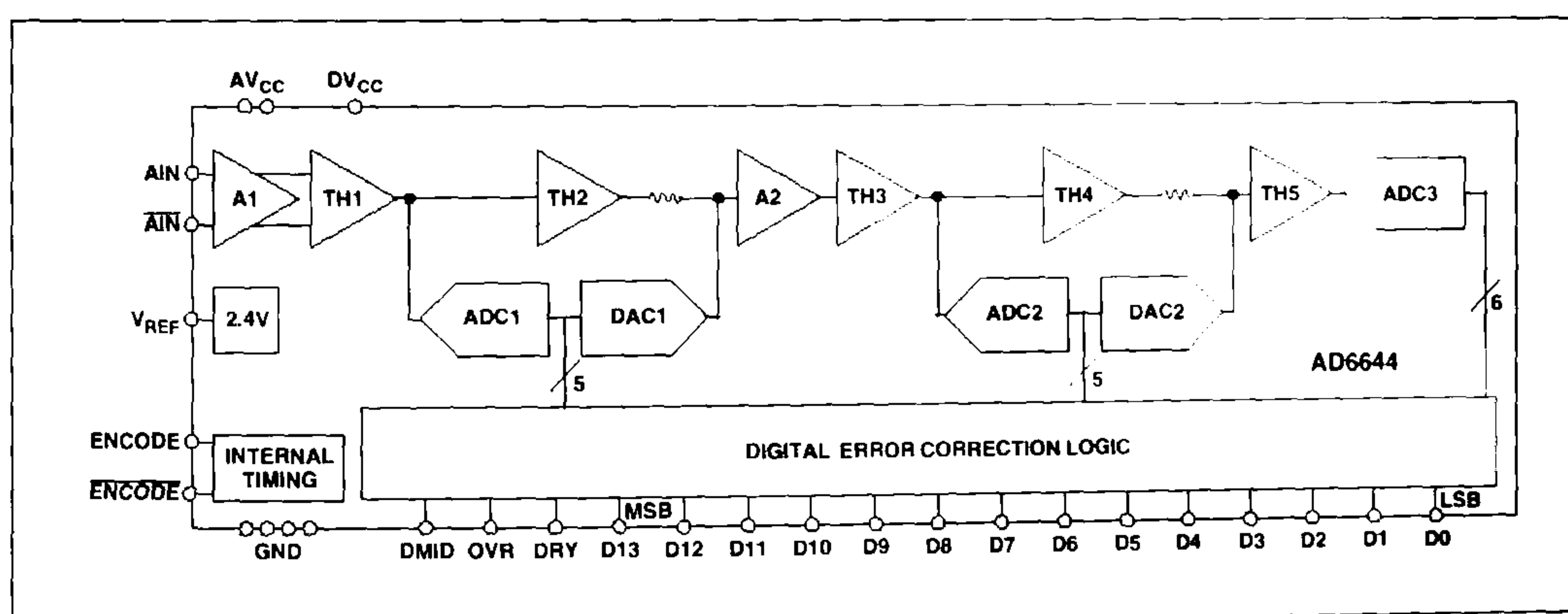


Figure 5-20 Architecture of High Performance AD6644 14-bit Multi-Stage ADC [Analog, 107]

It has been shown [Brannon, 111] that the application of an additional large noise-like signal (dithering) can improve ADC SFDR as much as 10 to 25 dB. The impact of DNLs can be reduced by applying an additive noise signal to the input of the ADC. Clearly, if this were simply added as wideband noise it would significantly reduce the ADC's sensitivity. This is therefore usually done either by injecting a wideband noise signal and using cancellation techniques (see Figure 5-21 [Agilent, 112]) or by injecting

a narrower noise signal in an unused part of the ADC's frequency range (normally near DC or close to $F_s/2$). The latter technique is easier to implement and has the further advantage that, in a digital receiver, the dither energy can be filtered out in the DDC. With the correct choice of noise power this signal has the effect of causing the non-linear transition region to be crossed frequently (but randomly) and hence spreading the spurious output. The net effect is to spread the spurious energy across the entire converter bandwidth and make it noise like. Hence for a small reduction in the effective SNR (of the order of $\ll 1$ dB) the spurious products can be greatly reduced.

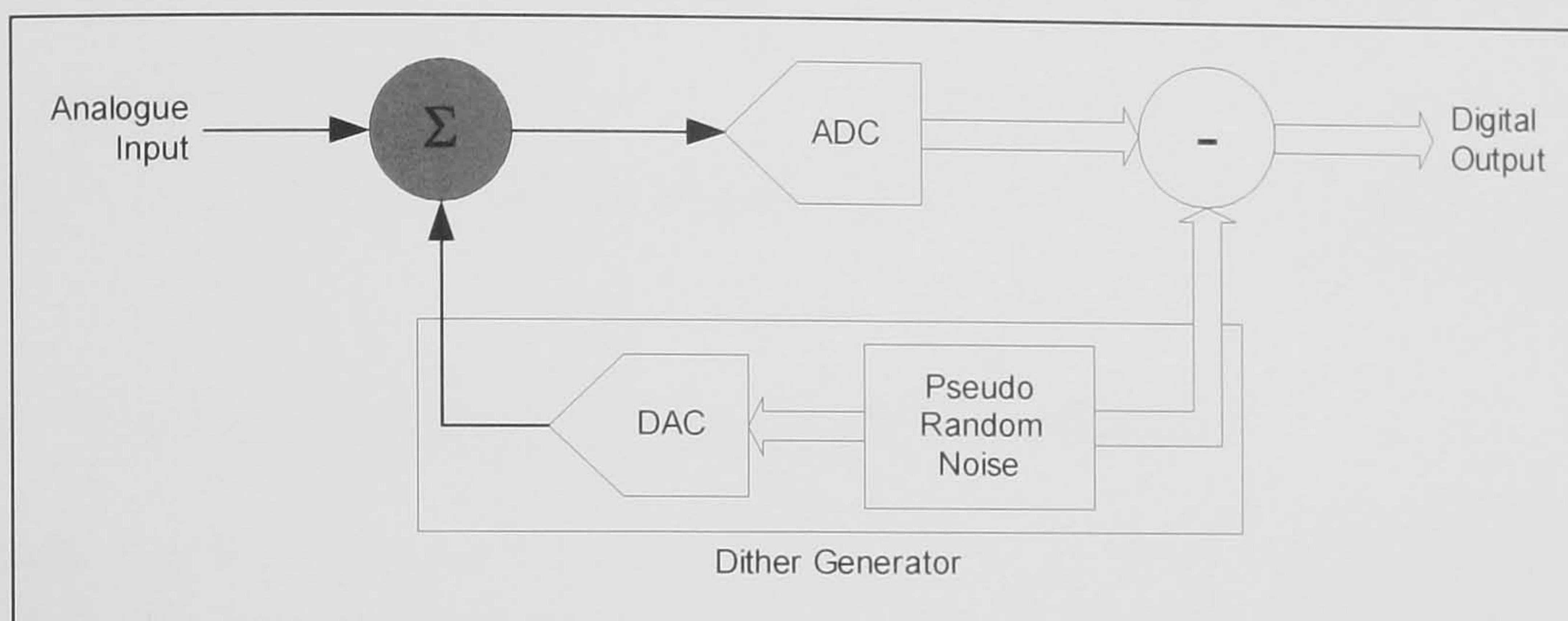


Figure 5-21 Application of Wideband Dither to Improve ADC SFDR

The required dither power can be accurately determined by means of a detailed characterisation of the ADC transfer function (input voltage versus output code) or approximately by inspection of the ADC architecture. For the AD6644 the main DNLs arise from a slight mismatch between the first and subsequent stages. The 9-bit final ADC stages (5-bit and 6-bit stages together, of which 2-bits are for error correction and hence not counted) will repeat every 2^9 (512) codes (quantisation intervals). In order to ensure the transition errors are completely randomised enough dither energy should be added to cross two repeat zones, or 1024 peak-peak codes. Hence the required dither energy relative to ADC full-scale input power is given by:

$$\text{Required Dither Power} = 20 \log_{10} \left[\frac{2^9 \times 2}{2^{14}} \right] \approx -24 \text{ dBFS} \quad (5-26)$$

As the AD6644 has a full scale input of ~ 5 dBm when correctly matched to 50Ω , the required dither power is -19 dBm. The significant improvement obtained by applying this dither power is illustrated in Figure 5-22.

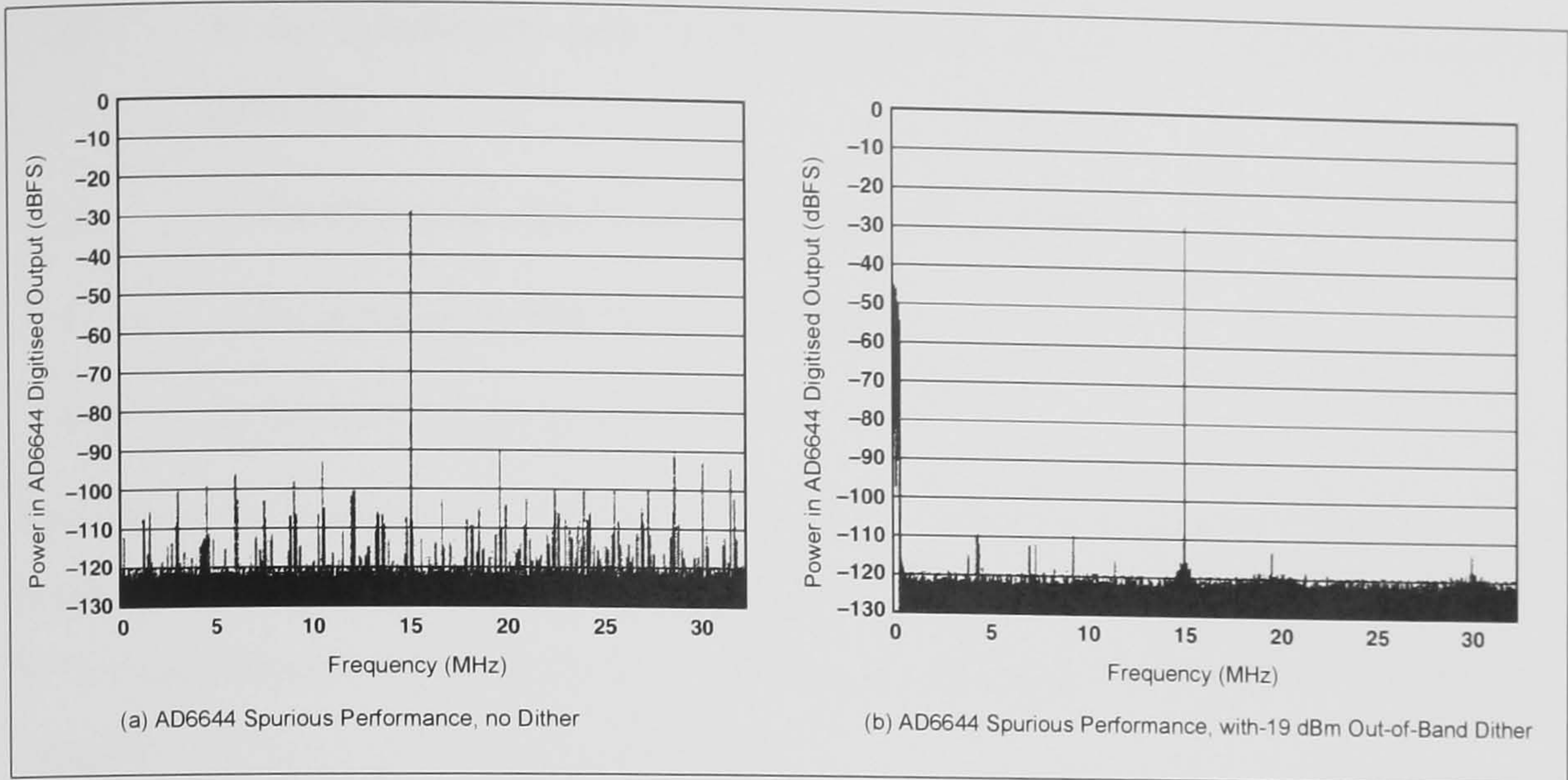


Figure 5-22 Improvement in AD6644 Spurious Performance with Addition of a Dither Signal [Analog, 107]

5.8.5 HF Congestion as a Source of Dither Power

The large number of uncorrelated signals present in the HF band (due to other user’s transmissions, noise, interference) is actually beneficial in that they effectively provide additional dither energy and thus, in this context, contribute to SFDR improvement.

Work has been done to quantify the extent to which signals of opportunity in the HF band can provide the necessary dither energy for a direct sampling HF receiver located in Europe. This was done using the Laycock-Gott occupancy model previously introduced with the model coefficients published by Economou [Economou, 35]. The model is capable of predicting congestion within any of the 95 ITU allocations against a signal strength threshold between 1 μV/m and 100 μV/m and measurement bandwidths between 200 Hz and 10 kHz. The model allows a lower bound to be placed on the mean available dither power due to congestion:

$$P_{DITHER} = 10 \log_{10} \left[\sum_{k=3}^{95} \left(\frac{P(k) BW(k)}{B} \right) \right] + 10 \log_{10} \left(\frac{E^2 G_{ANT} G_{RX}}{50 \times 0.001} \right) \quad dBm \quad (5-27)$$

where

- k is the ITU allocation number (k=3 to 95 covers the 2-30 MHz HF band);
- $P(k)$ is the probability of congestion in the k ’th allocation;
- $BW(k)$ is the bandwidth of the k ’th allocation;

B is the bandwidth used in the congestion model to establish occupancy (200 Hz);

E is the threshold signal strength in V/m (90 μ V/m);

G_{ANT} is the antenna power gain (3 dB); and

G_{RX} is the receiver power gain (17 dB).

The values in brackets are the values used in the analysis presented below. It is important to note the prediction is a lower bound because it assumes, due to limitations in this application of the occupancy model, that whenever a channel is occupied the congestion power is equal to the threshold.

The model was developed in MATLAB [Mathworks, 113] and used to predict the dither power available to a wideband digital receiver from the HF environment. Results have been obtained (Figure 5-23) for an antenna with an effective height of 2 m and located in Southern England with SSN=100. This gives confidence that congestion should provide the required dither power for the ADC. At higher SSN daytime absorption increases and the available dither energy decreases.

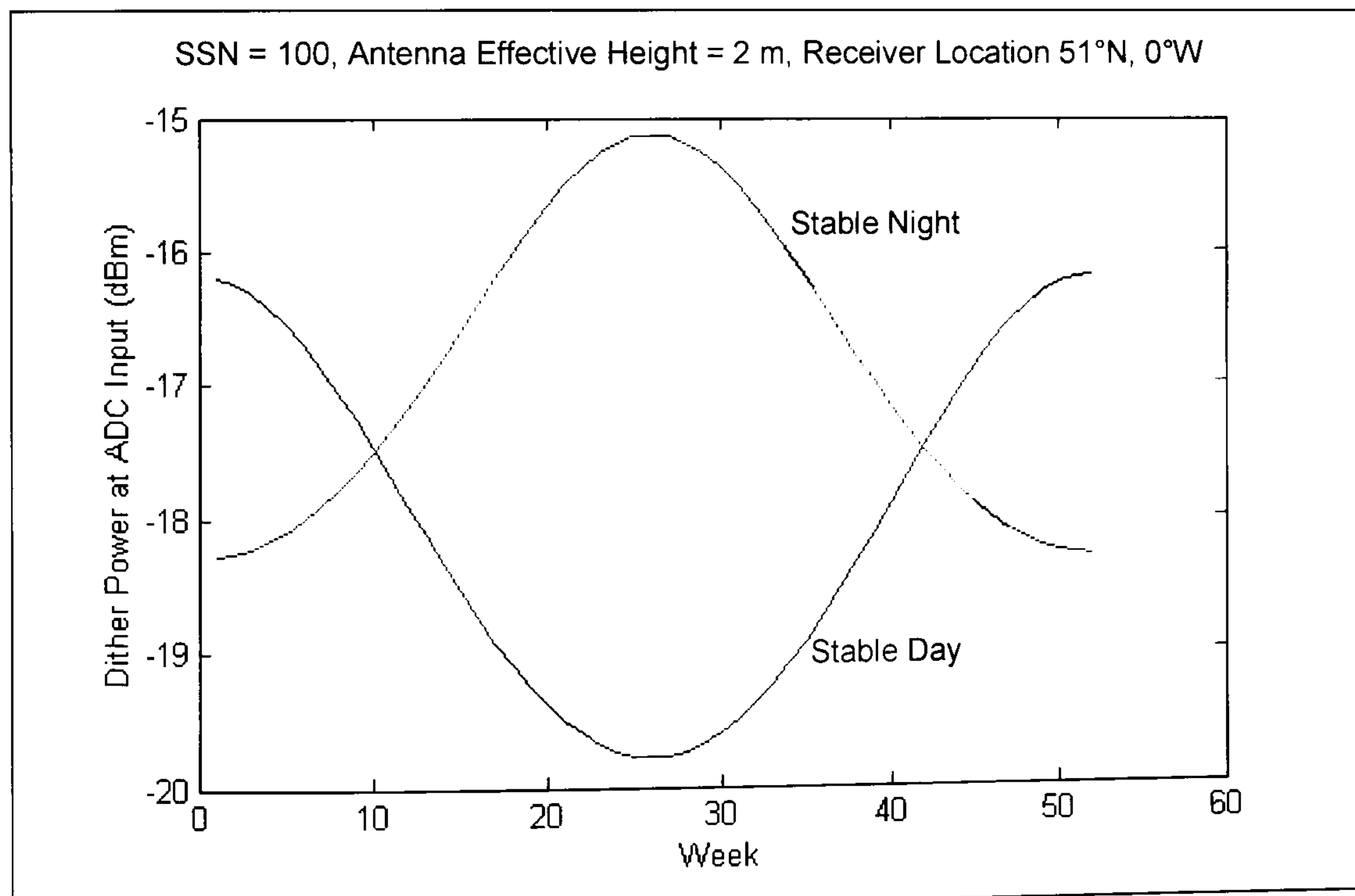


Figure 5-23 Predicted Mean Available Dither Power Due to HF Congestion (Lower Bound)

5.8.6 Summary of Practical Digitiser Performance

This section has considered some of the keys aspects of ADC performance that would impact their use in a direct-sampling HF digital receiver. New developments in ADC technology, embodied in the Analog Devices AD6644 ADC, suggest that this approach is now technically feasible. For an input frequency of 30 MHz the AD6644 has a calculated NF of 29.8 dB and a full-scale input power of 4.8 dBm (using a transformer coupled input [Analog, 107]). This equates to an ADC IDR/BDR of 149 dB in 1 Hz (114 dB in 3 kHz). With the use of dither a SFDR of 110 dB can be achieved.

5.9 Digital Down-Converter (DDC)

5.9.1 Introduction

Once the HF band has been digitised by the ADC a digital receiver function (or digital down-converter, DDC) is required to select each ‘channel’ of interest, to mix it down to complex baseband and to provide selectivity through filtering. To enable further signal processing to be implemented efficiently the signal sample rate is usually reduced to a value commensurate with the final signal bandwidth. Figure 5-24 is a block diagram of a basic DDC. A numerically controlled oscillator (NCO) is used to generate a quadrature sine/cosine waveform which is mixed with the input to translate it to baseband. The subsequent filtering and decimation produces a complex baseband output with a sample rate decimated by a factor M from that of the input.

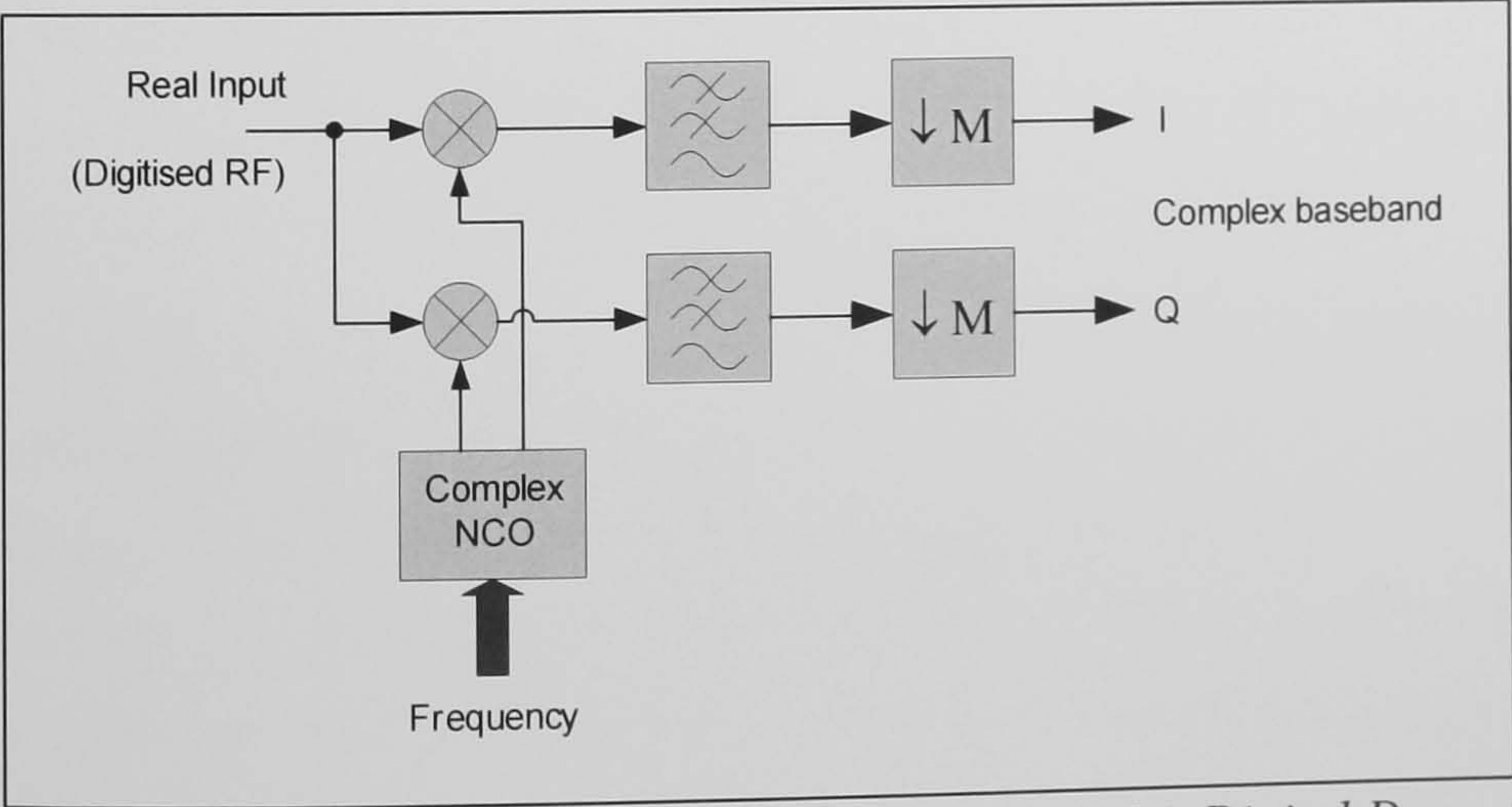


Figure 5-24 Digital Down-Converter

5.9.2 Processing Gain in Digital Receivers

Although a wideband receiver may digitise portions or even an entire frequency band, individual signals of interest have much narrower bandwidths. The process of digital filtering and decimation that selects the wanted signal reduces the available noise bandwidth whilst preserving the signal power and thus increases the effective SNR. This is termed processing gain. If F_s is the ADC Nyquist sampling rate and B is the bandwidth of the signal to be received then the SNR of the received signal is given by:

$$SNR = 10 \log_{10} \left(\frac{F_s}{2} \right) - 10 \log_{10} B + SNR_{ADC} \quad dB \quad (5-28)$$

where

SNR_{ADC} is the SNR measured at the ADC output.

5.9.3 Practical Digital Down-Converter Implementations and Performance

Conceptually, once a received signal has been digitised subsequent (digital) signal processing can be undertaken with an arbitrary degree of fidelity. However the implementation of DSP algorithms, particularly those operating at high sample rates, imposes practical constraints. DDCs generally use fixed precision arithmetic and the finite word length also imposes limits on dynamic range due to finite quantisation and rounding errors. Therefore in addition to the restrictions that the receiver RF front-end and ADC place on dynamic range, the DDC can also impose limitations. The following paragraphs consider practical DDC implementation and discuss the performance of the DDC used in the prototype digital receiver.

Frequency translation to complex baseband may readily be implemented by splitting the digitised (real) input signal into two branches and mixing them by in-phase (I) and quadrature (Q) outputs from a complex numerically controlled oscillator (NCO). Figure 5-25 illustrates the form of a basic sampled-time NCO using an incrementing phase register to address a sin/cos lookup table. Alternative implementations may calculate the samples more directly; for example using the COordinate Rotation DIgital Computer (CORDIC) algorithm [Volder, 114].

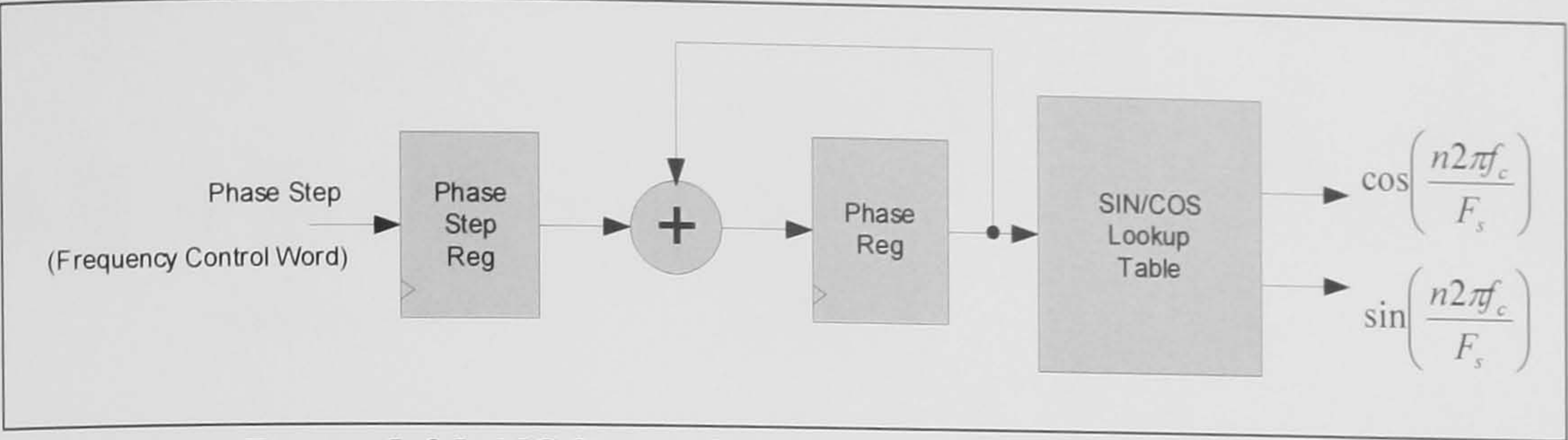


Figure 5-25 NCO as a Complex (Quadrature) Direct Digital Synthesiser

Once the signal of interest has been translated to baseband filtering must be applied to remove signals outside the bandwidth of interest and the images of the mixing process. A computationally economical class of decimating (or interpolating) sampled time filters has been proposed by Hogenaur [Hogenaur, 115]. These are generally known as cascaded integrator comb (CIC) filters. A decimating CIC has a transfer function of the form:

$$h(z) = \left(\frac{1 - z^{-MR}}{1 - z^{-1}} \right)^L \tag{5-29}$$

where

- M is the filter decimation factor;
- L is the filter order (number of integrator and comb stages); and
- R is the differential delay in the comb section.

This class of filters may be implemented as recursive running sums (RRS) with feedback, thus requiring no multipliers and making them particularly suited to implementation in digital hardware. Further, the integrator and comb filter sections may be separated by the sample decimator, only requiring the integrator section to be run at the full input sample rate, F_s , whilst the comb section can run at F_s/M (Figure 5-26).

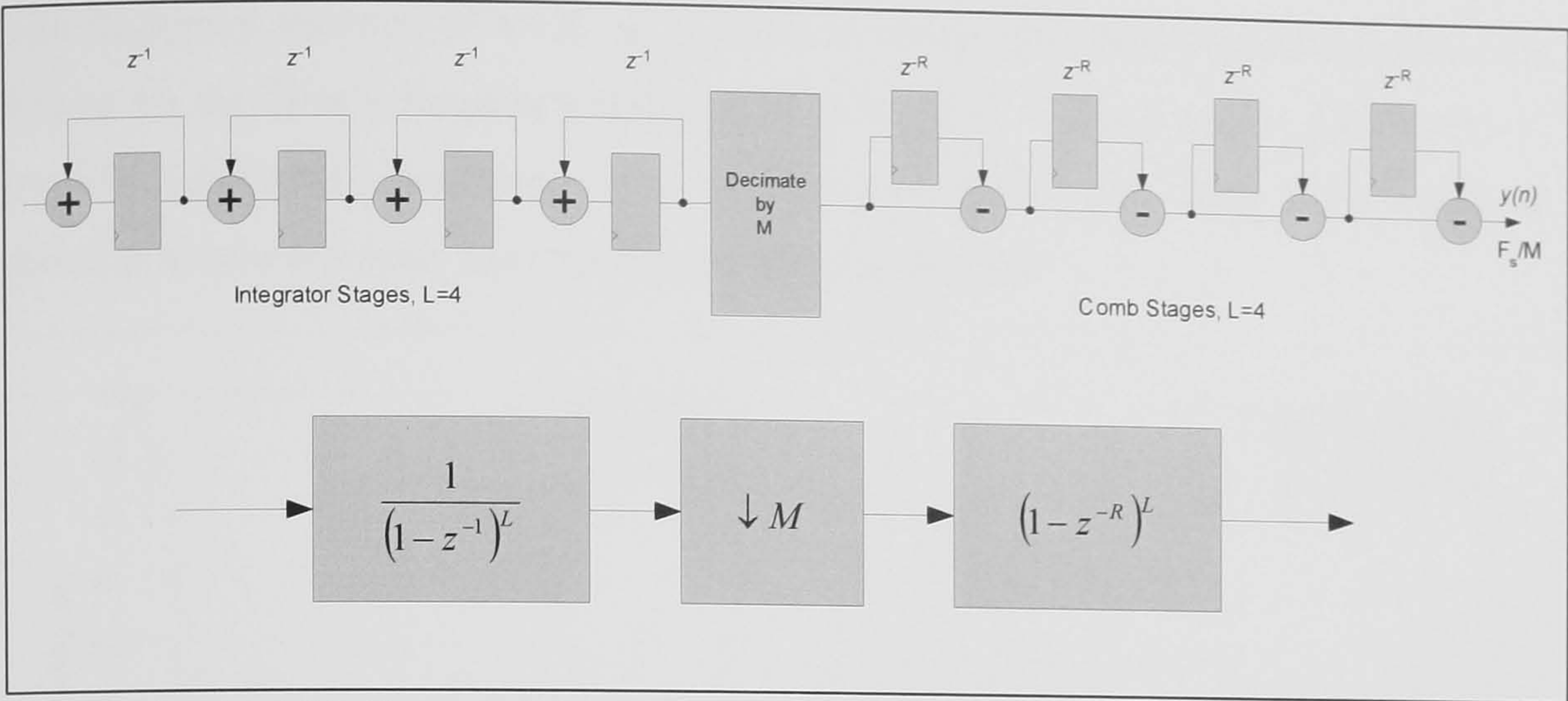


Figure 5-26 Practical Decimating CIC Filter - Integrator, Decimator and Comb

The frequency response of a decimating CIC filter is given by [Hyuk, 116]:

$$H(e^{j\omega}) = \left(\frac{1}{MR} \frac{1 - e^{j\omega MR}}{1 - e^{j\omega}} \right)^L$$

(5-30)

Figure 5-27 shows the frequency response of an un-decimated CIC filter with a normalised output frequency. Aliasing that occurs when the signal is decimated determines the filter’s useful selectivity. Further, it should be noted that the response in the pass-band is not flat. In a practical implementation the CIC must be followed by another filter (typically an FIR) which corrects the pass-band ‘droop’ and provides additional selectivity (image rejection).

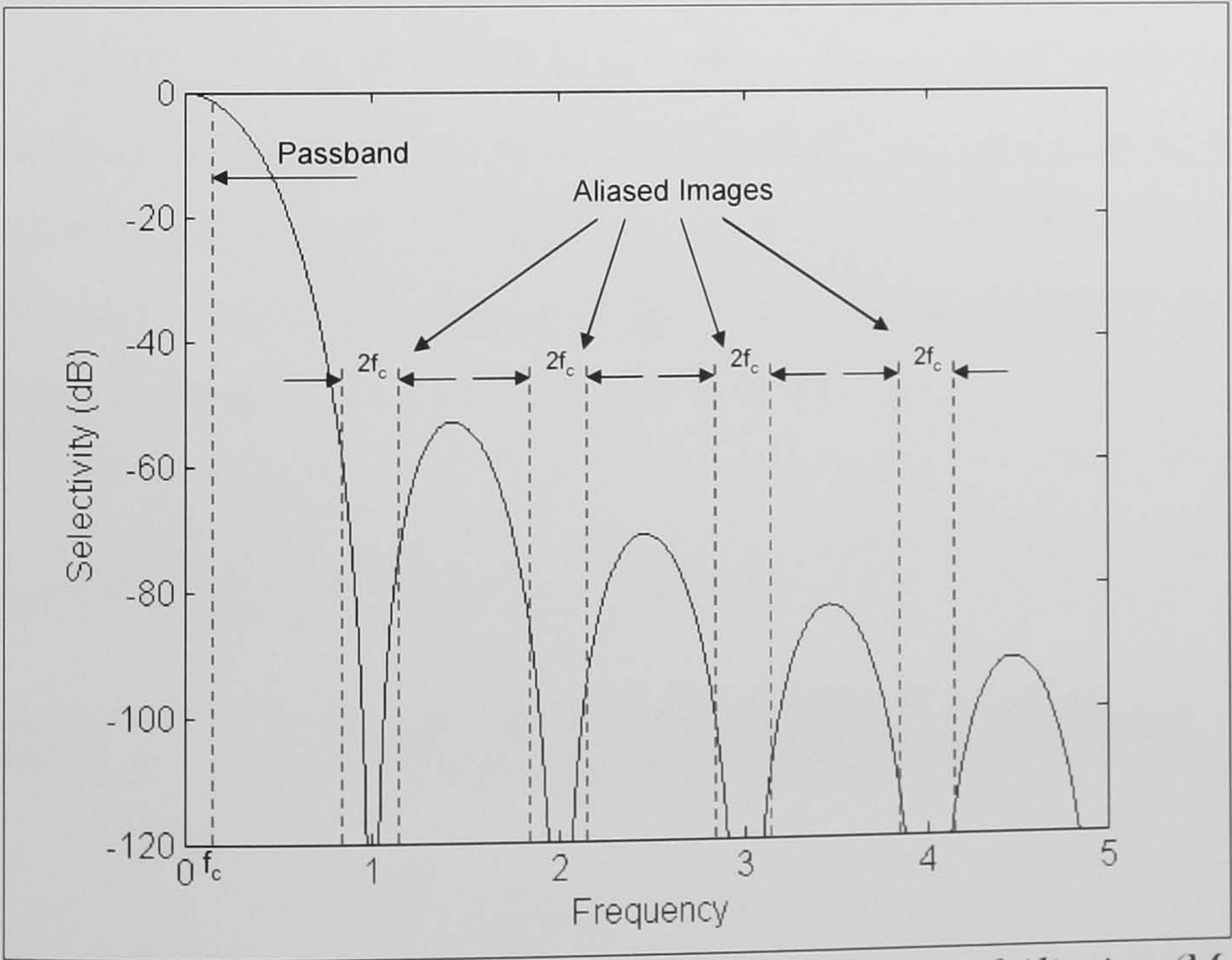


Figure 5-27 Frequency Response of CIC showing Impact of Aliasing ($M=100, L=4, R=1$)

The frequency response of a CIC as L and R are varied has been modelled to show the impact on the filter’s frequency response (Figure 5-28). Increasing the filter order, L , provides additional selectivity, whilst increasing the differential delay in the comb, R , provides a narrower pass band for a given decimation rate.

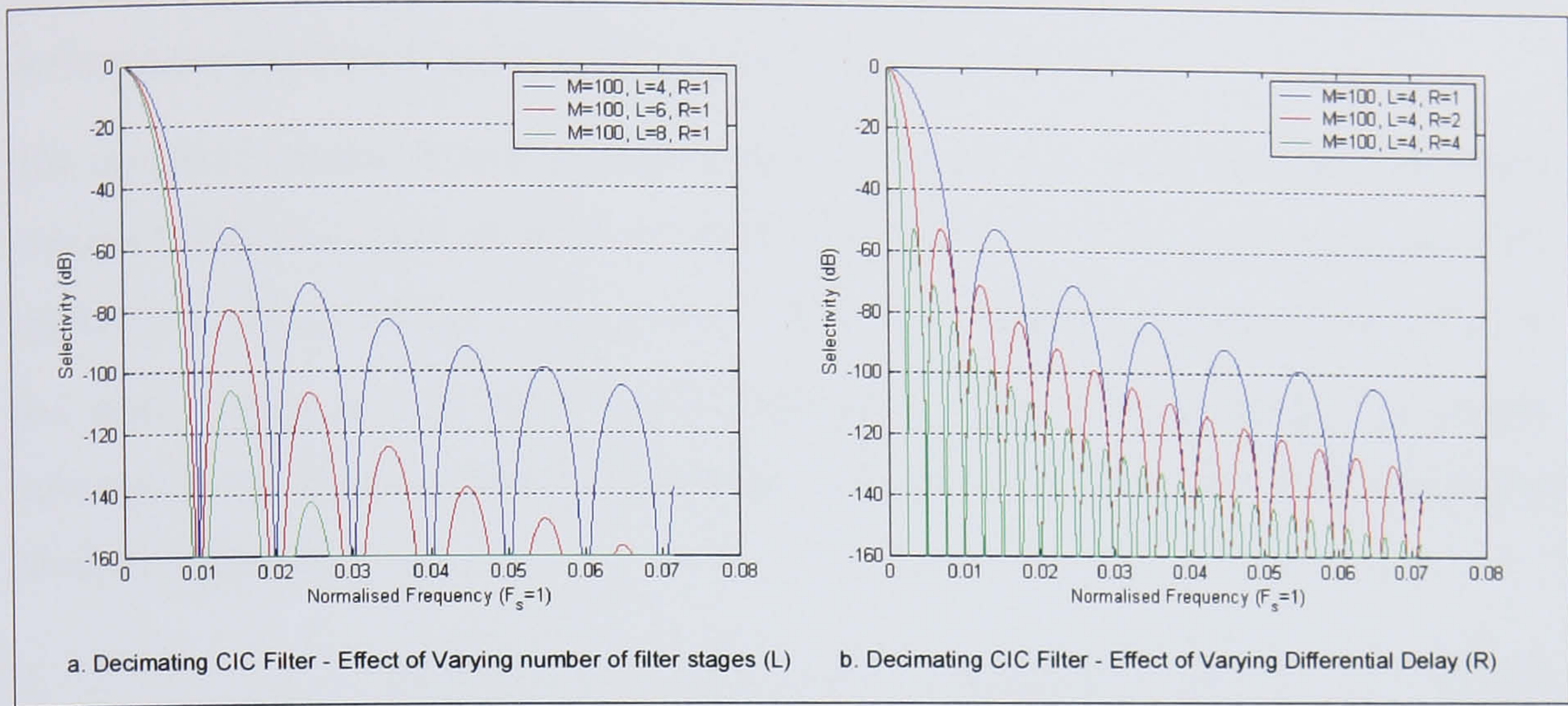


Figure 5-28 Modelled Frequency Response of CIC Filters as a function of L and R .

5.9.4 Receiver Blocking Dynamic Range

For the high performance ADC considered (75 dB SNR_{ADC}) at a sampling rate of ~ 65 MSPS, the 3 kHz SNR is ~ 115 dB. This is both the receiver’s instantaneous dynamic range (IDR) and its blocking dynamic range (BDR). The use of a digitally controlled attenuator in the front end of the receiver allows the available IDR to be shifted by typically up to 30 dB (Figure 5-29). Thus, large total input powers ($\leq +15$ dBm) can be accepted albeit at a penalty in sensitivity (as would be the case in a ‘blocked’ narrowband conventional receiver). In cases where the receive performance is externally noise limited (as is often the case at HF), attenuation can be added to cope with strong signals without compromising useful sensitivity.

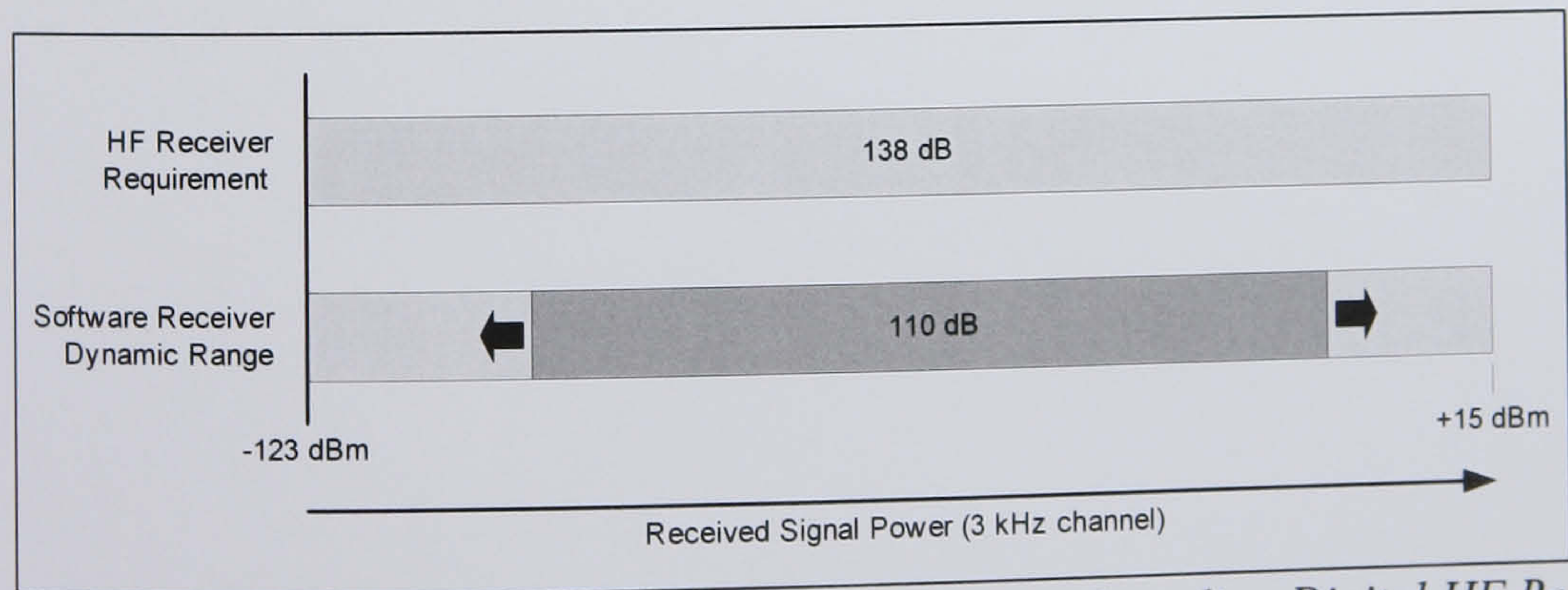


Figure 5-29 Dynamic Range in the Direct Sampling Digital HF Receiver

5.10 A High Performance Direct Sampling Digital HF Receiver

A spreadsheet based analysis has been undertaken to predict the performance of a wideband direct sampling HF receiver using the AD6644 ADC and a commercially available high performance RF amplifier [REMEC, 117]. The other component performance parameters are based on a survey of typical values.

The cascaded parameter analysis is presented in Table 5-2. Note that the spreadsheet cascaded analysis results are given in terms of parameters referenced to the output of the system (i.e. $IP2_{OUT}$, $IP3_{OUT}$, $P_{SAT_{OUT}}$ etc). These are converted to figures referenced to the input, which are the more useful measure of receiver performance, by simply subtracting the receiver gain (in decibels). The BDR of such a wideband digitising receiver is given by:

$$BDR = (P_{SAT_{IN}}) - 174 - NF - 10 \log_{10}(BW) \quad dB \quad (5-31)$$

The results show that a very high performance receiver is possible: $NF=13.8$ dB, $IP3_{IN}=+27.2$ dBm, $IP2_{IN}=+80.7$ dBm and $BDR(3 \text{ kHz})=112.8$ dB. It is expected that performance would meet or exceed that of the majority of the highest performance conventional narrow band HF receivers currently available and yet, being a wideband design allow reception of an arbitrary number of channels using a single analogue front-end.

Digital HF Receiver - Cascaded Nominal Input/Output Parameters

Analysis of Direct Sampling Architecture - using OB101 High Intercept Point RF Amplifier

Cumulative Output Summary									
P[signal] (dBm)		Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P[saq] (dBm)	P[sig] (dBm)	P[n] (dBm/BW)	SFDR (dB)
-113.00		17.20	13.76	97.92	44.38	4.80	-95.80	-142.90	124.86
Cumulative Parameters									
Device Parameters { @ Output }		Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P[saq] (dBm)	P[sig] (dBm)	P[n] (dBm/BW)	SFDR (dB)
Component Designation									
1 Front-end filter/protection		-2.00	0.00	1000.00	100.00	20.00	-115.00	-175.85	183.90
2 Digitally controlled Attenuator		-2.00	0.00	85.00	45.00	18.00	-117.00	-177.85	148.57
3 QB-101 (note 1)		21.80	4.50	105.00	54.00	31.00	-95.20	-148.60	134.92
4 Harmonic filter		-0.30	0.00	1000.00	100.00	30.70	-95.50	-148.90	134.92
5 Dither Combiner, Transformer (1:4)		-0.30	0.00	1000.00	100.00	30.40	-95.80	-149.20	134.92
6 AD6644 ADC (note 2)		0.00	29.80	115.00	45.00	4.80	-95.80	-142.90	124.86

Notes:

1	Q-bit High Performance Amplifier
2	AD6644 used with dither to provide 110 dB SFDR.

Table 5-2 Predicted Performance of a Direct Sampling HF Receiver

5.11 An Alternative Single Conversion Wideband Receiver Architecture

Given the demanding 2nd order IMD and harmonic performance requirement in the amplifier of a direct sampling receiver an alternative architecture worthy of consideration is one employing a single, whole band up-conversion. Such a receiver would have the majority of its signal gain at a wideband IF reducing the 2nd order IMD and harmonic performance requirements on that amplifier. However, such an architecture would require additional circuit elements (mixer, IF filter) which must have excellent linearity in order not to themselves degrade the receiver performance. If, in a particular implementation, an RF amplifier is required ahead of the mixer then its performance requirements are commensurate with that of the RF amplifier in the direct sampling approach. In such a case the single conversion approach is unlikely to provide any benefit.

The IF frequency selected must be within the ADC's analogue bandwidth and low enough that the SNR reduction due to sampling jitter (from all sources) is acceptable. The IF following the frequency translation must be sufficiently high in frequency to provide both good image and good out-of-band rejection. The experience of designing the front-end (anti-aliasing) filter for the direct sampling receiver indicates that an IF frequency centred on ~70 MHz would be practical and not be overly demanding on the sampling clock phase noise (jitter) performance.

A review of the applicable literature has been undertaken to establish the performance of mixers suitable for use in such a receiver. The analysis presented is based on the use of a high performance mixer (e.g. [GEC, 118], [Cox, 119], [Dexter, 120]).

The predicted performance of a single conversion receiver is shown in Table 5-3, namely: NF=13.4 dB, $IP3_{IN}=+22.7$ dBm, $IP2_{IN}=+77.1$ dBm and BDR(3 kHz)=111.3 dB. In this case the performance is limited by the IF amplifier and could be improved by using a higher performance alternative. However, this would require an amplifier with similar performance to that identified for the direct sampling receiver and would give similar performance but have greater complexity. It is therefore concluded that for a wideband whole-band digitising HF receiver this architecture offers no significant additional benefit.

Digital HF Receiver - Cascaded Nominal Input/Output Parameters

Analysis for Wideband Single Conversion															
Component Designation	Device Parameters (@ Output)					Cumulative Output Summary									
	Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P1dBr (dBm)	Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P1dBr (dBm)	P1sig (dBm)	P1n (dBm/Hz)	SNR (dB)	DR (dB)	SFDR (dB)
	-113.00					19.15	13.39	96.23	41.81	4.80	-93.85	-141.31	47.46	146.11	122.08
Cumulative Parameters															
	Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P1dBr (dBm)	Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P1dBr (dBm)	P1sig (dBm)	P1n (dBm/Hz)	SNR (dB)	DR (dB)	SFDR (dB)
1 Front-end filter/protection (note 1)	-2.00	0.00	1000.00	100.00	20.00	-2.00	0.00	1000.00	100.00	20.00	-115.00	-175.85	60.85	195.85	183.90
2 SW-395 Rx Switch	-0.55	0.00	85.00	48.50	21.00	-2.55	0.00	85.00	48.50	19.45	-115.55	-176.40	60.85	195.85	149.94
3 Mixer (note 2)	-1.00	4.00	83.00	43.00	100.00	-3.55	5.71	77.47	41.68	18.45	-116.55	-171.70	55.15	190.15	142.25
4 IF Filter (note 3)	-2.00	0.00	1000.00	100.00	100.00	-5.55	5.71	75.47	39.68	16.45	-118.55	-173.70	55.15	190.15	142.25
5 IF Amplifier, variable gain (note 4)	25.00	4.50	1000.00	45.00	100.00	19.45	10.11	100.47	44.96	41.45	-93.55	-144.30	50.75	185.75	126.17
6 Dither Combiner, transformer (1:4)	-0.30	0.00	1000.00	100.00	100.00	19.15	10.11	100.17	44.66	41.15	-93.85	-144.60	50.75	185.75	126.17
7 AD6644 ADC (note 5)	0.00	29.80	105.00	45.00	4.80	19.15	13.39	96.23	41.81	4.80	-93.85	-141.31	47.46	146.11	122.08

Notes:

- Use of mixing reduces roll-off requirement on band-select/image reject front-end filter
- Requires very high IP2 and IP3 performance mixer (e.g. Switched MOSFET design).
- High IF selected (e.g. 70-98 MHz). Large bandwidth implies use of a lumped element filter.
- IF amplifier IP3 performance is key but use of high IF makes IP2 and harmonic of minimal importance.
- AD6644 used with dither to provide 110 dB SFDR.

Table 5-3 Predicted Performance of a Wideband Single Conversion Digital HF Receiver

5.12 Chapter Summary

This chapter has considered the implementation of wideband digital HF radios. The requirements that the HF environment places on receiver design have been investigated. The performance of a high performance conventional narrowband HF receiver has been characterised to establish a basis for comparison.

The work presented indicates that it is now possible, for the first time, to construct a very high performance, direct sampling wideband digital HF receiver. Such a receiver would conceptually allow an arbitrary number of channels to be simultaneously received using a single RF front-end and digitiser. With careful design of the front-end filter and selection of a suitable RF amplifier, performance closely matching or even exceeding that of the highest performance single channel receivers commercially available can be obtained. Whilst receivers employing front-end pre-selection (i.e. sub-octave filters), have the potential to offer higher performance, the application of such filtering makes them inherently narrowband.

It has been shown that in a direct sampling receiver, front-end linearity, particularly for the RF amplifier, is critical. As there is no frequency translation in such a receiver and since the HF band covers approaching four octaves the amplifier second order intermodulation and harmonic performance will have a major impact on the overall receiver strong signal handling performance. The RF amplifier performance requirements have been calculated and a number of suitable commercial RF amplifiers have been identified showing that the proposition is practical.

An alternative wideband receiver architecture employing a single, whole band, up-conversion has been investigated and compared with the direct sampling approach. Such a receiver would have the majority of its signal gain at a wideband IF reducing the 2nd order IMD and harmonic performance requirements on that amplifier. However, such an architecture would require additional circuit elements (mixer, IF filter) which must have excellent linearity in order not to themselves degrade the receiver performance. It is believed that, in practical implementations this architecture is unlikely to offer any benefit over the direct sampling approach.

The following chapter presents a prototype direct sampling HF receiver design that has been constructed and evaluated.

Chapter 6.

Performance of a Prototype Direct Sampling Digital HF Receiver

The previous chapter considered the requirements for high performance HF receivers and examined the characteristics of practical direct sampling receiver implementations. This chapter presents the design of a prototype receiver and measured performance results obtained from a laboratory prototype. Suggestions for improvements to the prototype design are advanced.

The prototype digital receiver was implemented as part of a digital transceiver whose construction is described in detail in the next chapter. This chapter concentrates on the basic implementation and its measured characteristics.

6.1 Description of Prototype Receiver

Figure 6-1 is a block diagram of the prototype direct sampling digital receiver that has been designed and constructed. A separate front-end protection and filtering module provides overload protection and the necessary anti-alias filtering ahead of the receiver itself. In the prototype a digitally controlled RF switch allows the receiver input to be switched between different sources. This is followed by a variable gain RF amplifier, implemented as a digitally controlled attenuator followed by a fixed gain RF amplifier. A 30 MHz harmonic and noise reduction filter minimises the level of internally generated out-of-band signals reaching the digitiser. A digitally controlled narrowband dither source (applied below 1 MHz) is included to maximise the ADC SFDR. The digitised signal is passed to a programmable DDC ASIC which selects and down-converts the channel to be received.

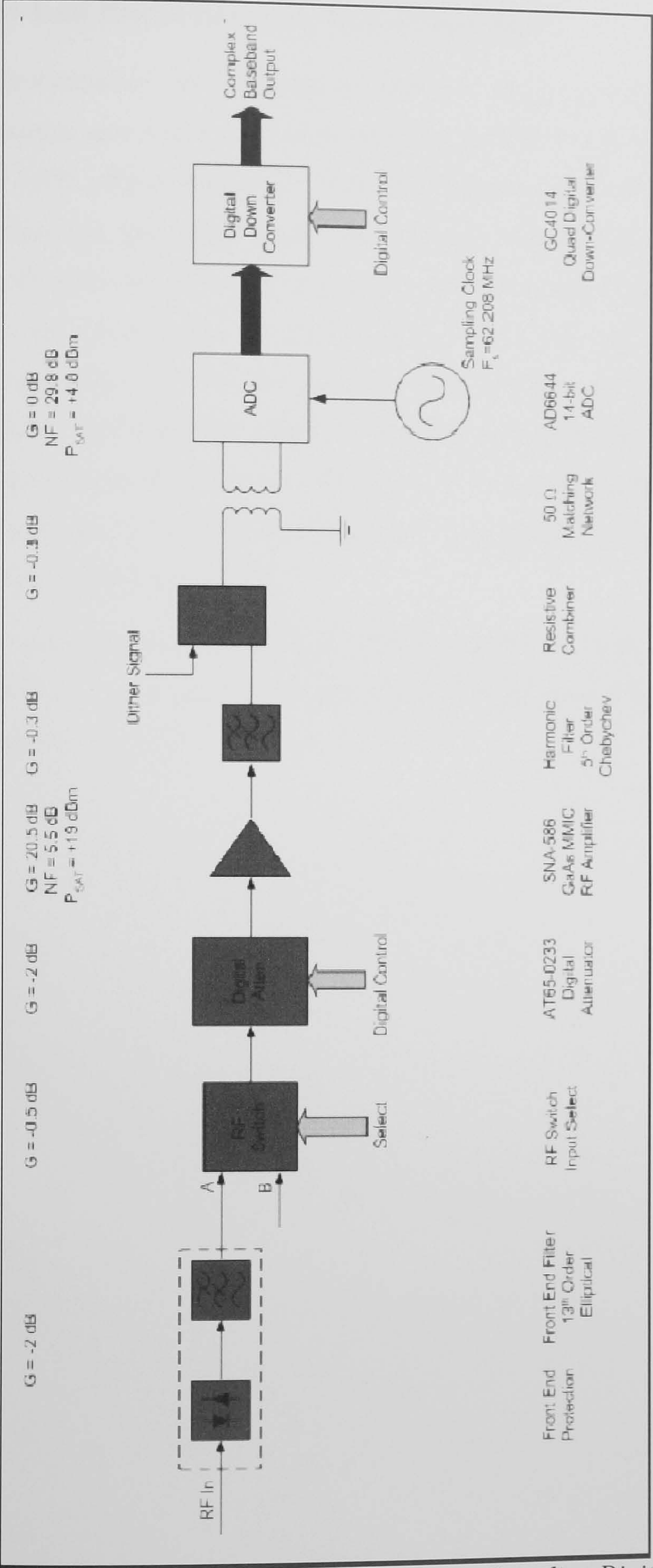


Figure 6-1 Block Diagram of Prototype Direct Sampling Digital HF Receiver

6.1.1 Front-End Protection and Anti-Alias Filter

Following experimentation with a number of prototype designs the final anti-aliasing filter implementation uses a dual stage high-order design. The first is a 7th order elliptic LPF with a 28 MHz corner frequency. Tuneable ferrite-cored inductors are used to allow the insertion loss, pass-band corner, and transition region to be optimised. The second filter, a 9th order elliptical LPF, makes use of fixed air-cored inductors for their high Q. These were found to give the greatest overall attenuation and to minimise roll-up at higher frequencies. In fact the large inherent analogue bandwidth of the RF amplifier and ADC (250 MHz for AD6644) results in a requirement for a filter that maintains its performance well beyond 500 MHz. The measured performance of the filter is shown in Figure 6-2 (selectivity), Figure 6-3 (group delay variation) and Figure 6-4 (input/output impedance matching).

Whilst the filter selectivity was generally found to be satisfactory (approaching 120 dB) it would benefit from additional work to reduce the insertion loss at the top of the HF band and to improve its VSWR.

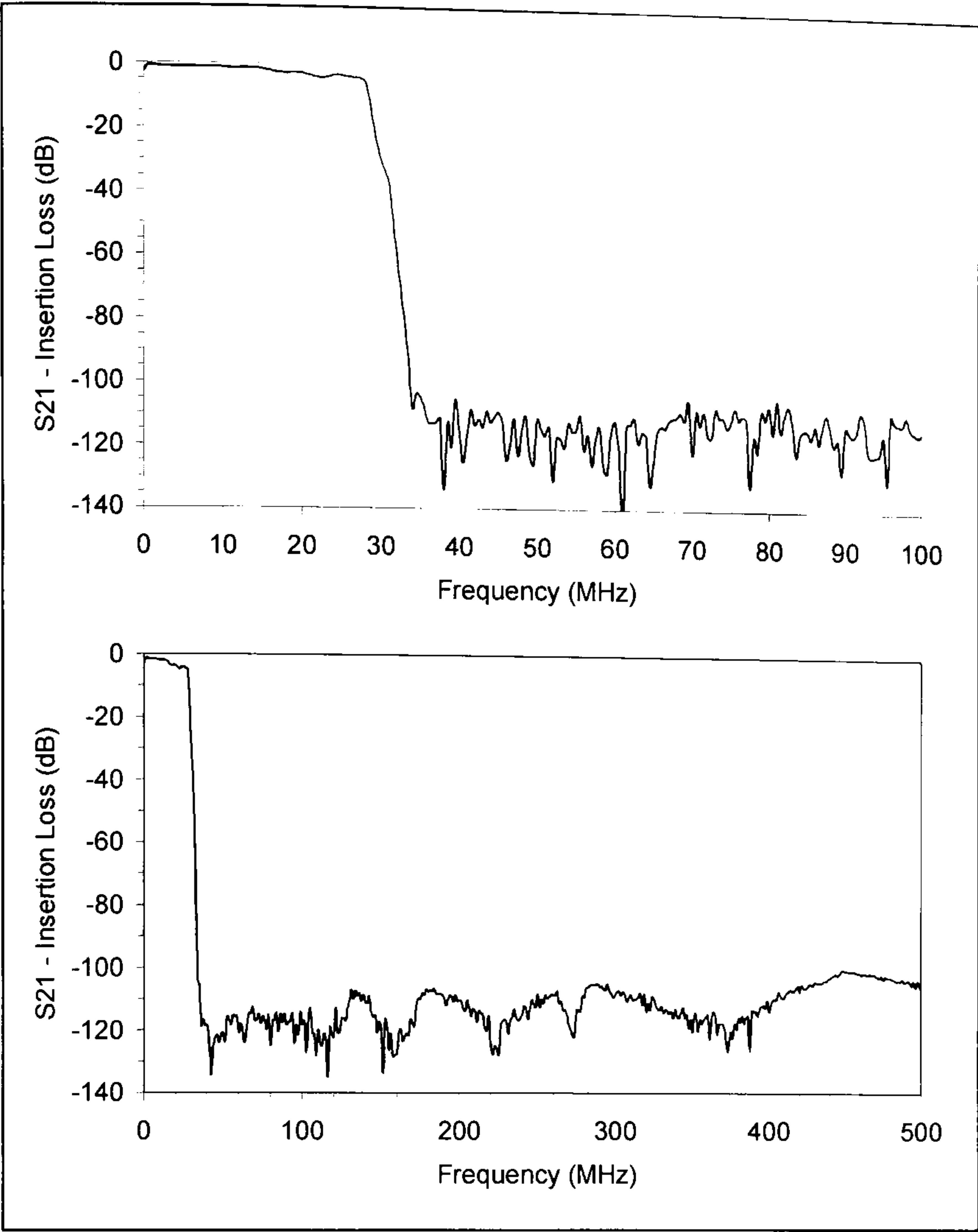


Figure 6-2 Measured Selectivity of Combined 28 MHz Elliptic Low Pass Filter

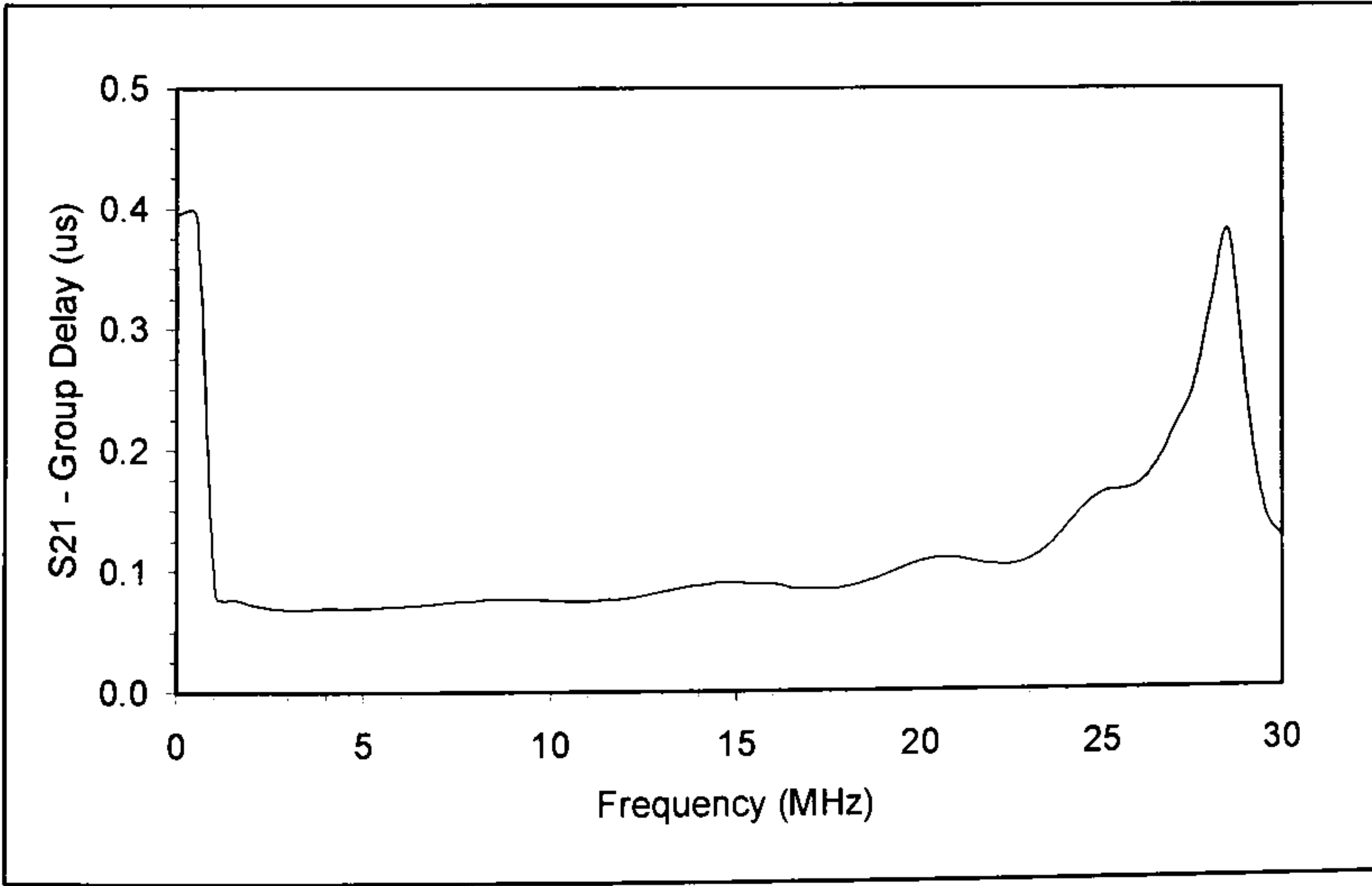


Figure 6-3 Front-End Filter Group Delay Variation

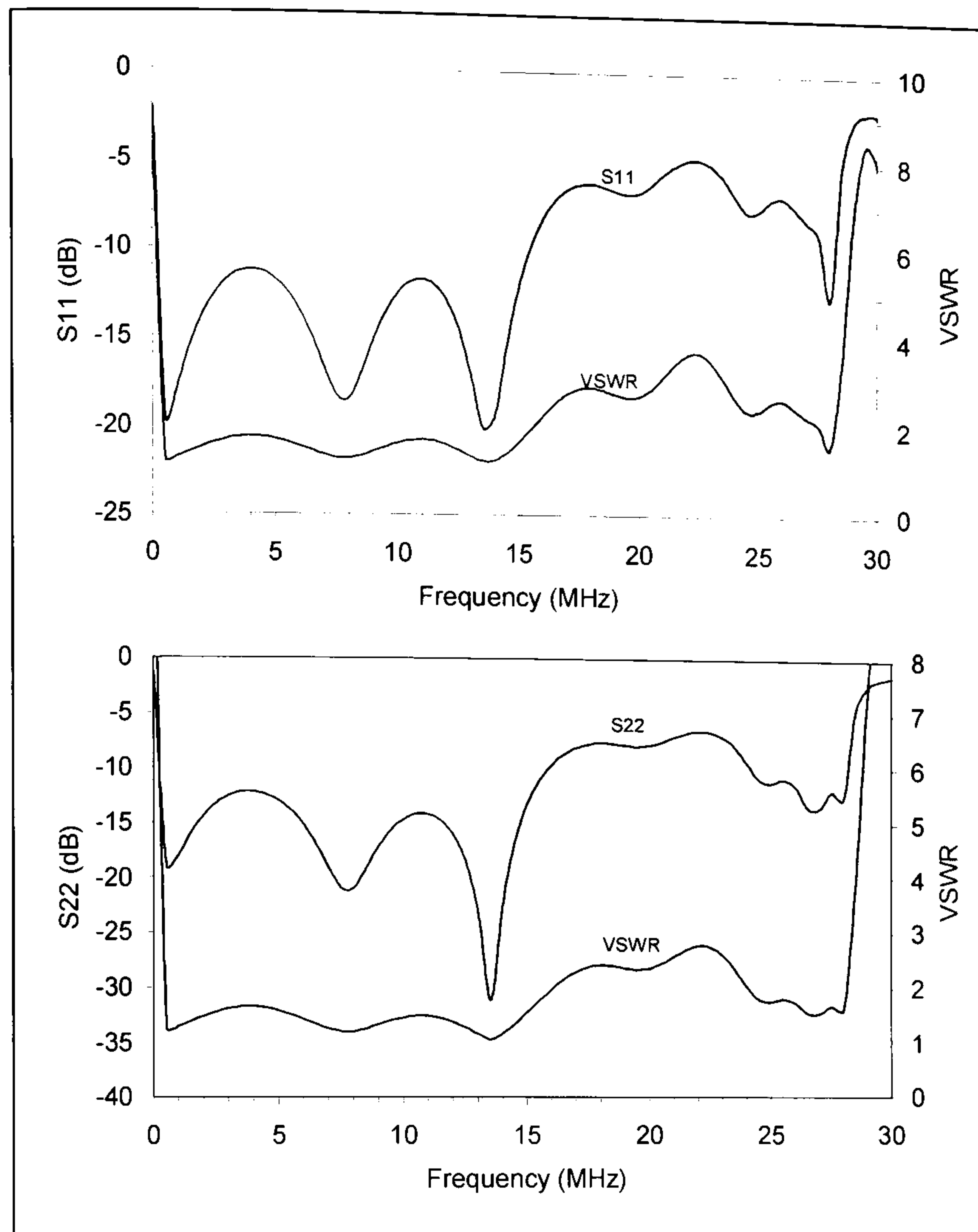


Figure 6-4 Prototype Front-End Filter Impedance Matching

6.1.2 Gallium Arsenide (GaAs) MMIC RF Amplifier with Digital Gain Control

This section discusses the performance of the GaAs miniature microwave integrated circuit (MMIC) RF amplifier used in the prototype direct sampling receiver. The amplifier used was a type SNA-586 50Ω gain block [Stanford, 121] which was readily available, small, easy to use and had good published NF and third order linearity. It was subsequently found that its second order (harmonic and IMD) performance is not ideal for this application.¹

¹ The choice of the RF amplifier device and the decision to not replace it are closely related to the progress of the project as a whole. The digital receiver was first investigated as a means to developing a wideband down-converter and digitiser following a conventional super-heterodyne front-end. An early prototype had been built using the chosen amplifier for that purpose. Due to limited resources it was decided to utilise the same device but to include a harmonic filter to provide some mitigation of harmonics above 15 MHz. Further work on characterising the digital receiver performance has quantified the limitations due to the amplifier.

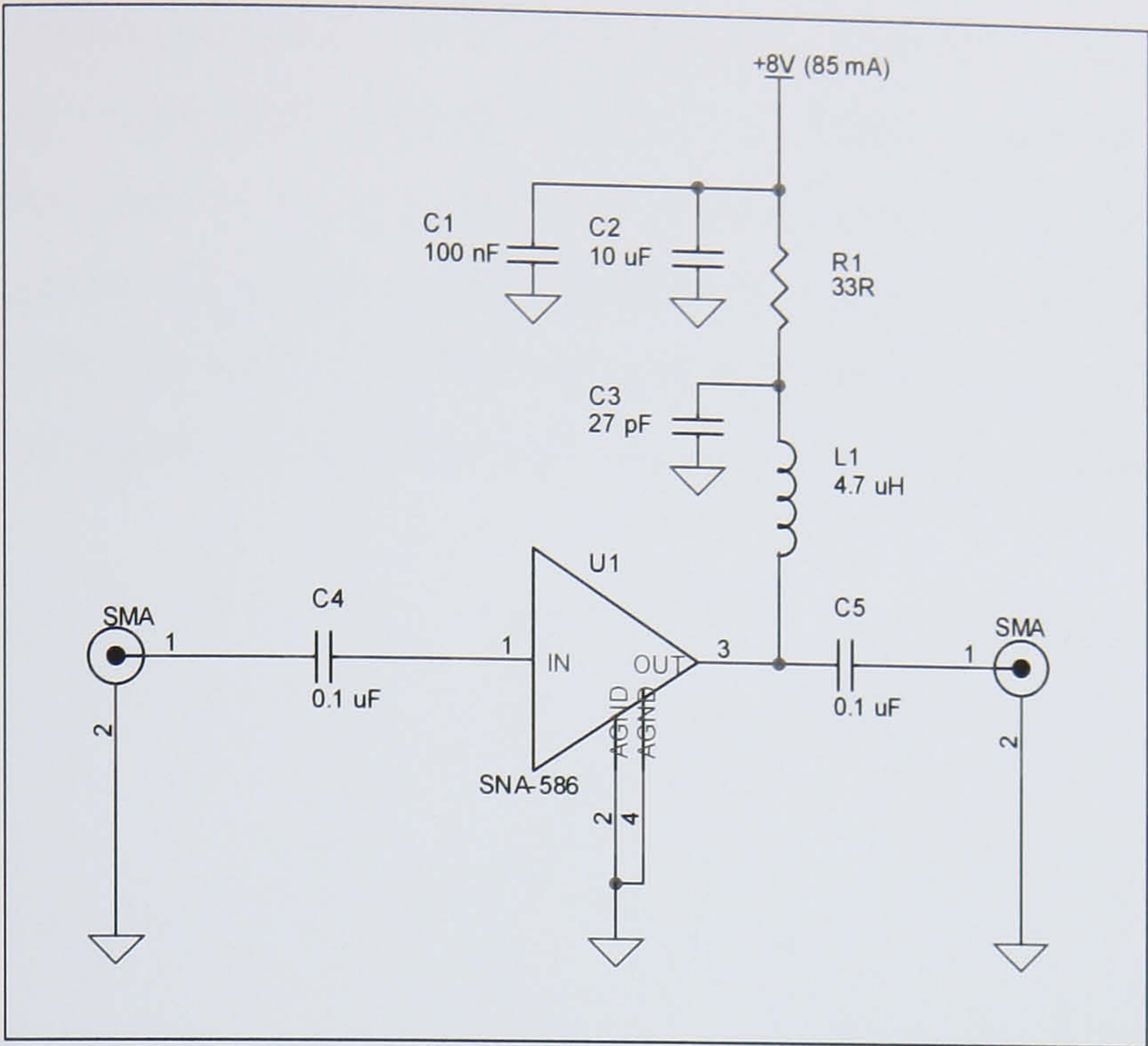


Figure 6-5 SNA586 GaAs RF Amplifier Test Circuit

The amplifier has been characterised using the circuit of Figure 6-5 constructed as a test piece (Figure 6-6). The amplifier was measured in this configuration using an s-parameter network analyser. The results indicate that it offers acceptable gain and matching performance for the intended HF application (Figure 6-7).

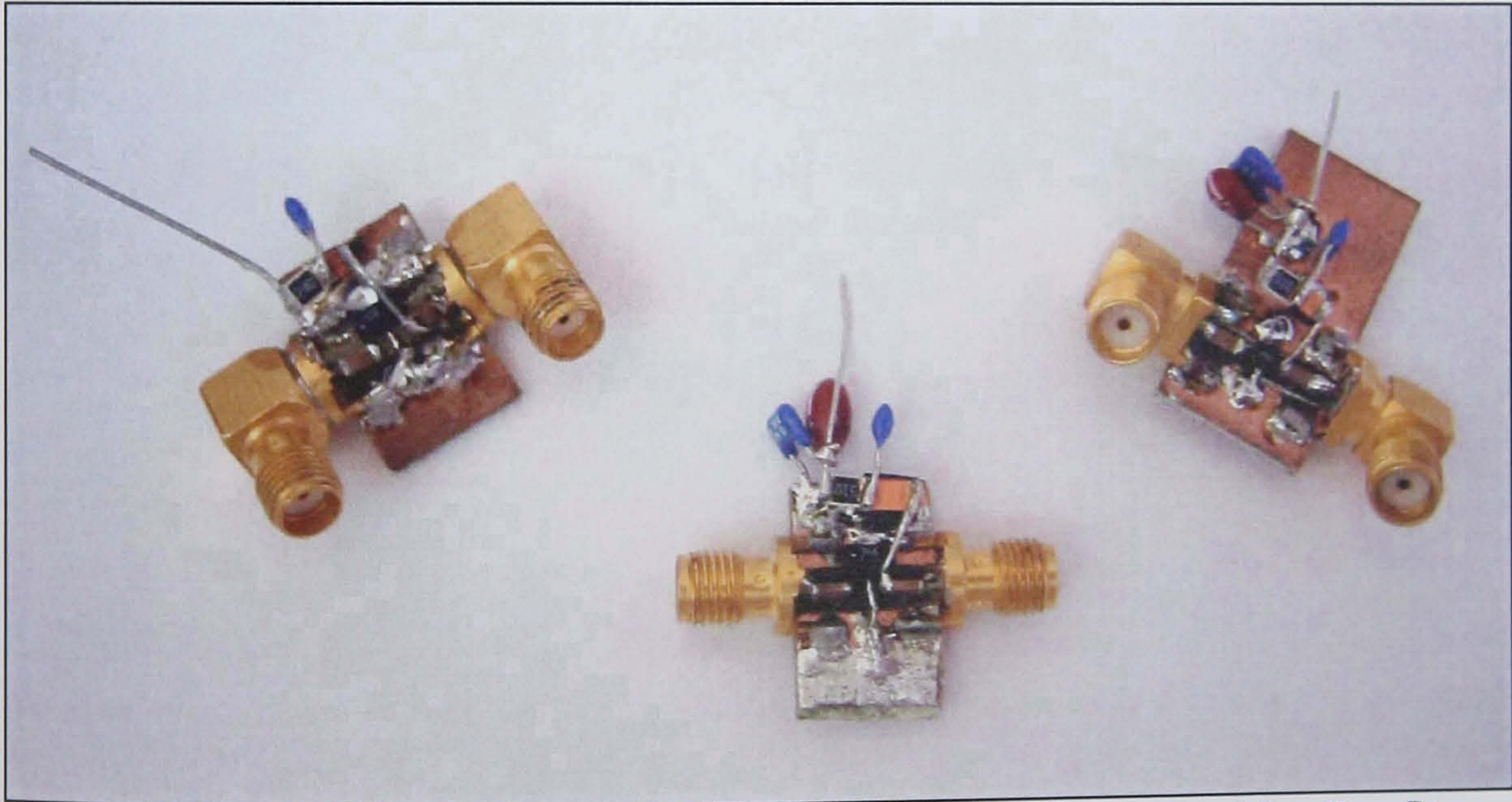


Figure 6-6 MMIC RF Amplifier Test Pieces

It has been found that whilst its IP_{3IN} was acceptable its IP_{2IN} and harmonic performance were inadequate to realise the full digital receiver capability for strong signal handling. The amplifier's measured IP_{3IN} was measured as +17.5 dBm. Using Figure 5-13 it can be seen that to realise the full SFDR this requires an IP_{2IN} in excess

of +70 dBm. Measured results for the amplifier’s second and third order intercept point as a function of frequency are shown in Figure 6-8. Table 6-1 presents the measured harmonic performance of the amplifier. Using these results and assuming a standard second order characteristic Figure 6-9 has been drawn to show at what input signal level 2nd and 3rd order harmonics would start to impact harmonically related channels. Products of order greater than three were not found to be a significant performance limitation.

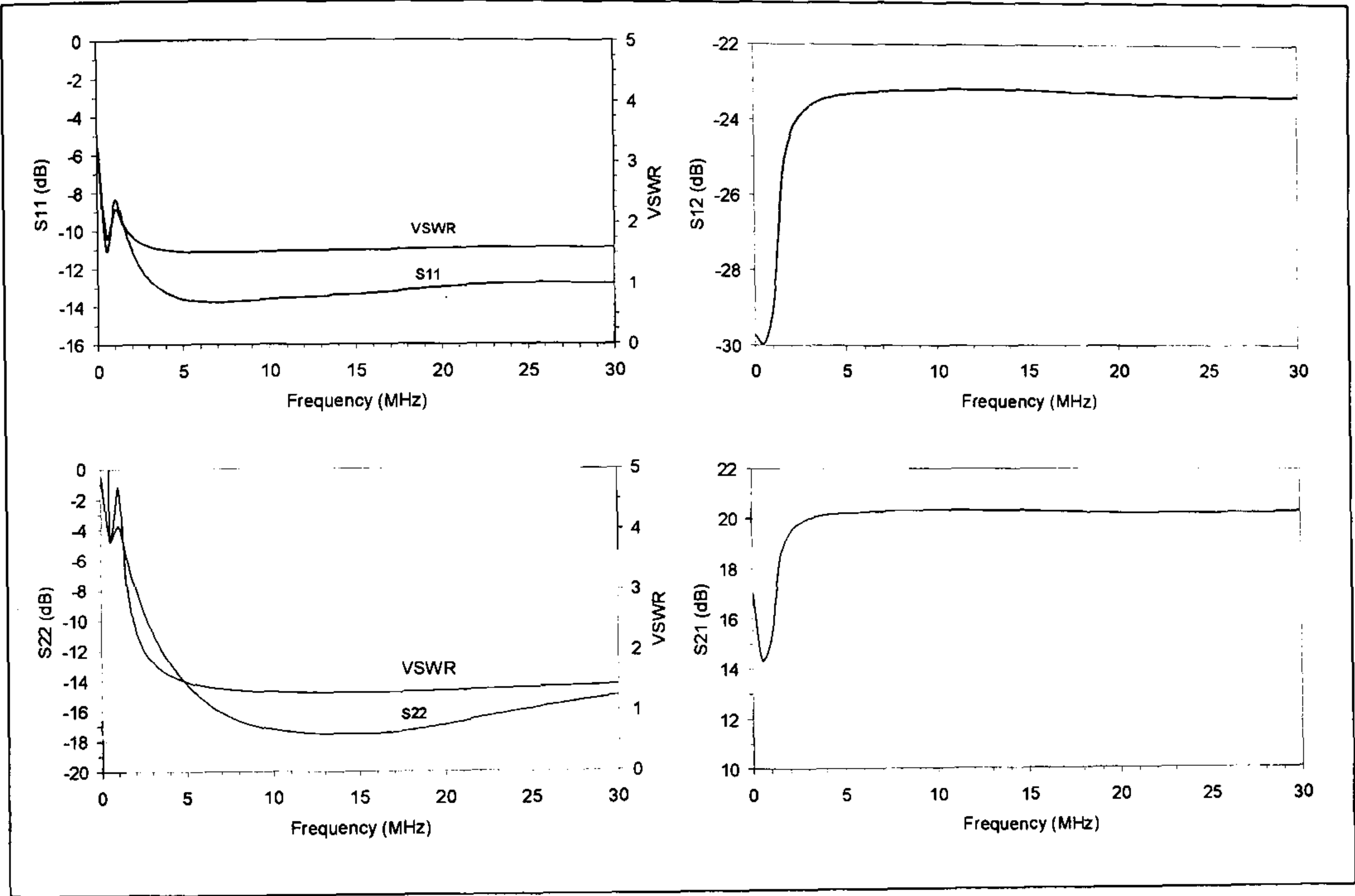


Figure 6-7 SNA-586 GaAs RF Amplifier Characteristics Measured on Network Analyser

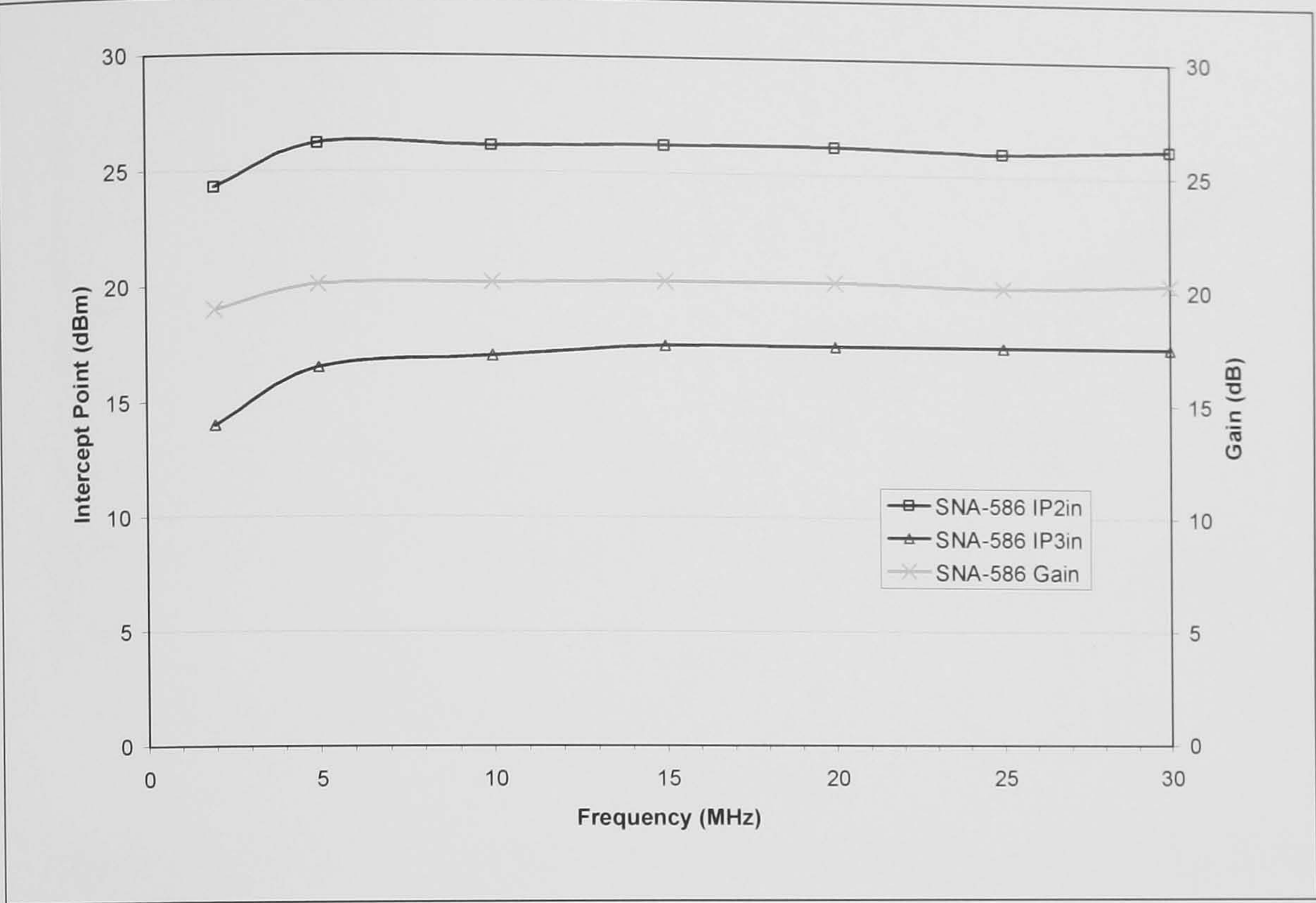


Figure 6-8 SNA-586 GaAs RF Amplifier Gain and Linearity Measurements

Frequency (MHz)	2 nd Harmonic (dBc)	3 rd Harmonic (dBc)
2	-42.0	-55.0
5	-44.0	-51.1
10	-41.0	-56.0
15	-42.0	-57.0
20	-42.3	-57.1
25	-39.5	-57.3
30	-40.0	-59.0
2-30 (Mean of above)	-41.5	-56.1

Table 6-1 SNA-586 Measured Harmonic Performance (-15 dBm input)

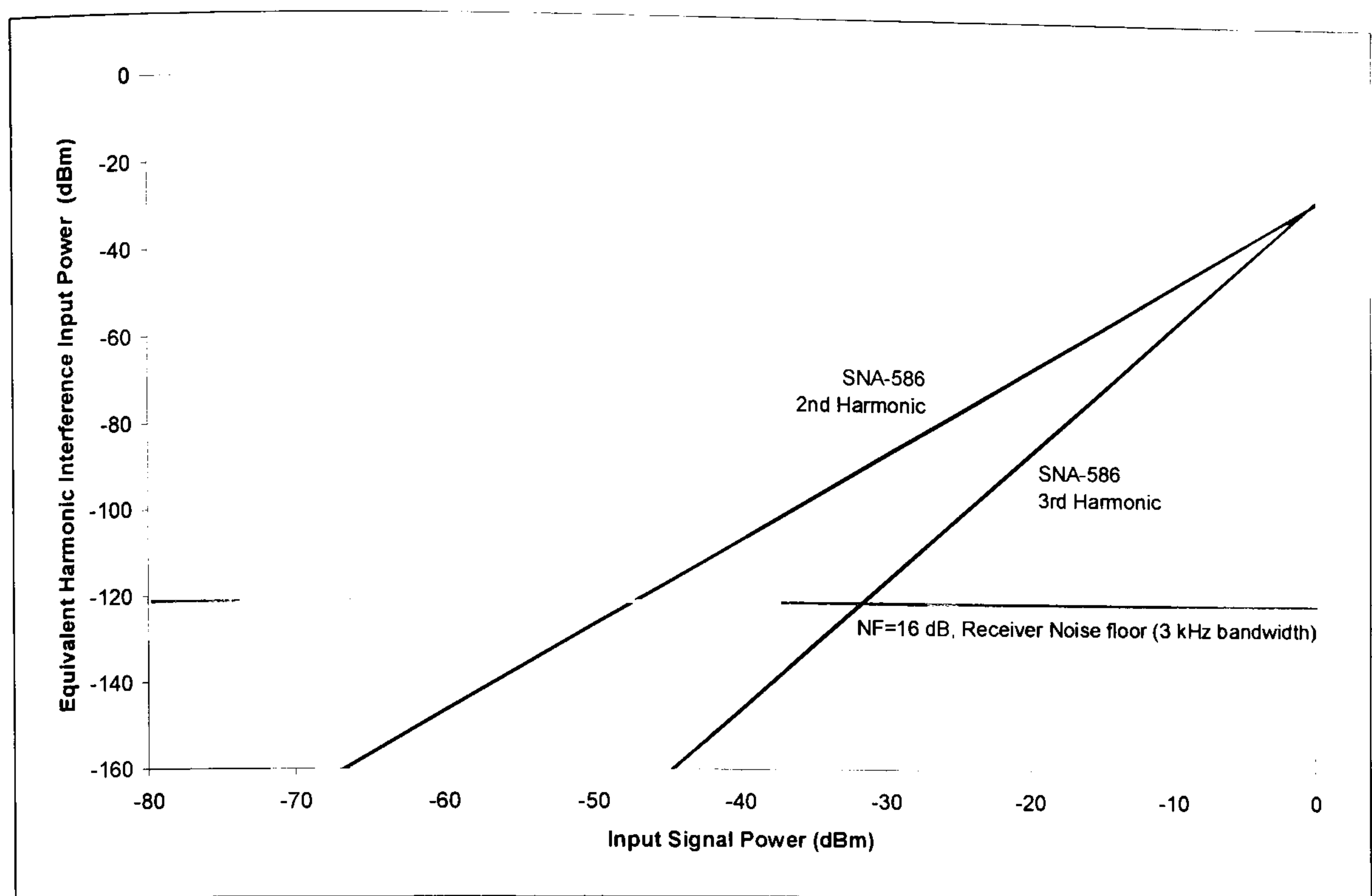


Figure 6-9 SNA-586 RF Amplifier 2nd and 3rd Harmonic Performance (Extrapolated)

6.1.3 Harmonic Filter

A fifth order 0.25 dB Chebychev filter with a corner frequency, f_c , of 30 MHz has been implemented to minimise the impact of harmonics that fall out-of-band (particularly those due to the RF amplifier used). The filter was modelled using the SPICE analogue circuit simulation tool (Figure 6-10).

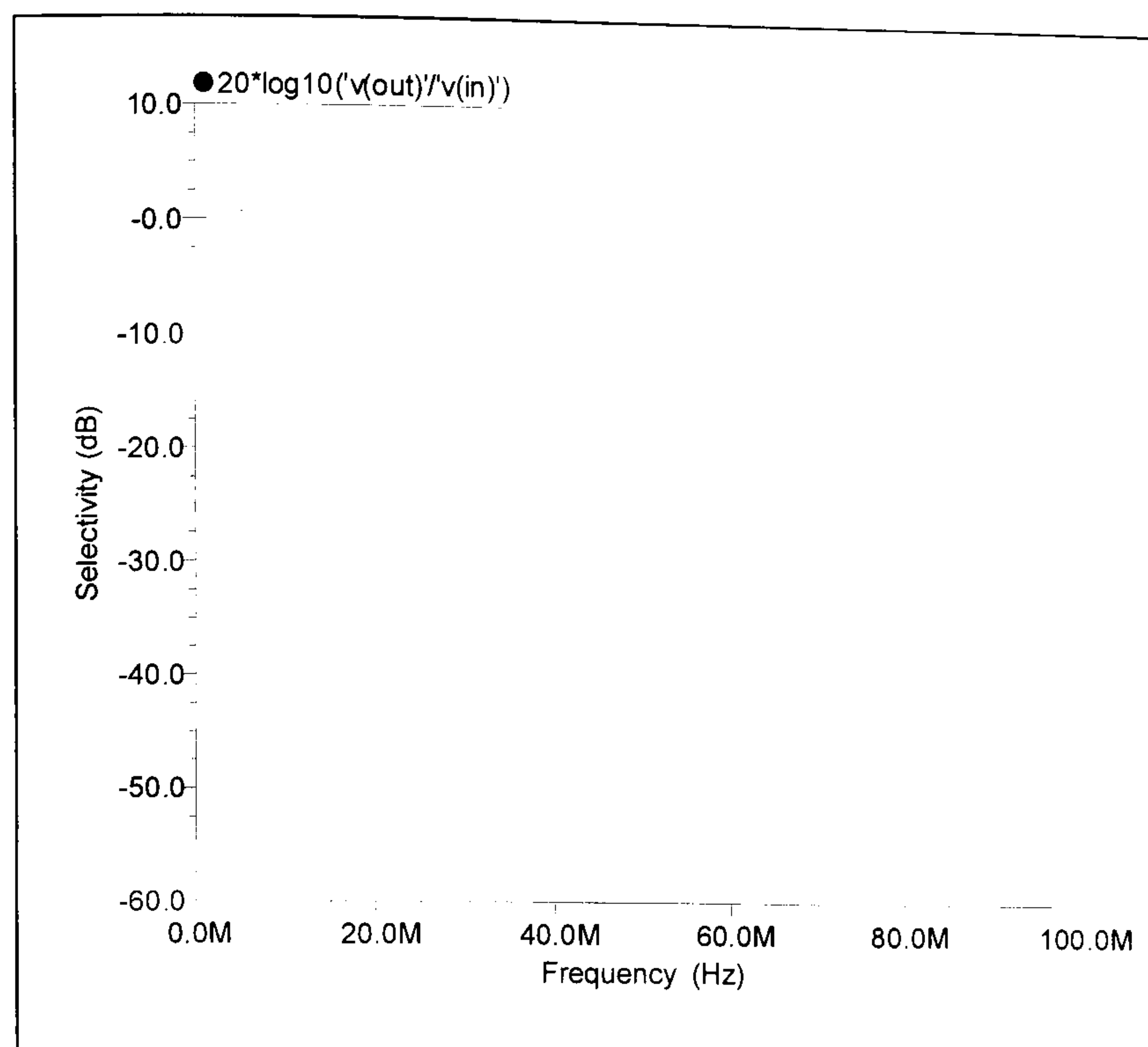


Figure 6-10 Selectivity of 5th Order Harmonic Filter (Modelled with SPICE)

6.1.4 Digitiser (Analogue-to-Digital Converter)

A high performance ADC, the Analog Devices AD6644 [Analog, 107], that became available (as a pre-production 'X-Grade' part) at the time that this study was undertaken was selected for use in the prototype direct sampling receiver. This is a high performance 14-bit ADC which supports sampling rates up to 65 MSPS. The AD6644 has a calculated NF of 29.8 dB and a full-scale input power of 4.8 dBm (using a transformer coupled input). This equates to an ADC IDR/BDR of 149 dB (114 dB in 3 kHz). The basic ADC SFDR is 90 dB. With the use of dither a SFDR of ≥ 110 dB can be achieved. Therefore a narrowband dither generator is included in the prototype implementation and allows a dither noise signal to be added to the input of the ADC. To maximise performance the dither is added out-of-band at frequencies below 1 MHz.

6.1.5 Sampling Clock Generation

In the prototype direct sampling digital receiver a sampling clock has been implemented by utilising a high quality voltage controlled crystal oscillator (VCXO) with a narrow (~ 15 kHz) tuning range, and phase locking this to either a temperature compensated crystal oscillator (TCXO) or a high stability external frequency standard (e.g. a Rubidium standard). The VCXO utilised (Connor Winfield HV54 VR1 [Connor, 122])

has an RMS phase jitter of ≤ 0.6 ps (at offsets from 12 kHz to 20 MHz). The TCXO (Connor Winfield HTV546 [Connor, 123]) has improved close-in phase noise. Phase locked together they have a predicted phase noise (from datasheet specifications and allowing for the PLL implementation) as shown in Table 6-2 which equates to an integrated RMS phase jitter of ~ 0.7 ps. Using the VCXO phase locked to an external frequency standard with good long term stability maximises the performance of the prototype receiver.

Offset (Hz)	Phase Noise (dBc/Hz)
1 Hz	-75
10 Hz	-80
100 Hz	-100
1 kHz	-125
10 kHz	-140
≥ 1 MHz	-155*

*Estimated Value

Table 6-2 Prototype Wideband Digital Receiver TCXO/VCXO Combined Phase Noise

6.1.6 DDC Performance in Prototype Wideband Digital Receiver

The prototype direct sampling digital receiver makes use of a Graychip GC4014 DDC ASIC [Graychip, 124]. This device contains four independent DDC cores enabling reception of up to four signals simultaneously. The input is mixed down to complex baseband using a complex NCO. It is then filtered and decimated using a 4-stage (L=4, R=1) cascaded integrator-comb (CIC) digital filter including a programmable decimator (M=16...32k). This is followed by a 21-tap, decimate-by-2, compensating FIR (CFIR) low pass filter and then a 63-tap, decimate-by-two or by-four programmable FIR (PFIR) low pass filter (Figure 6-11). The device produces a 16-bit complex baseband (IQ) output. The gain through each stage of the digital receiver may be programmed to maximise the instantaneous dynamic range for a given input signal level.

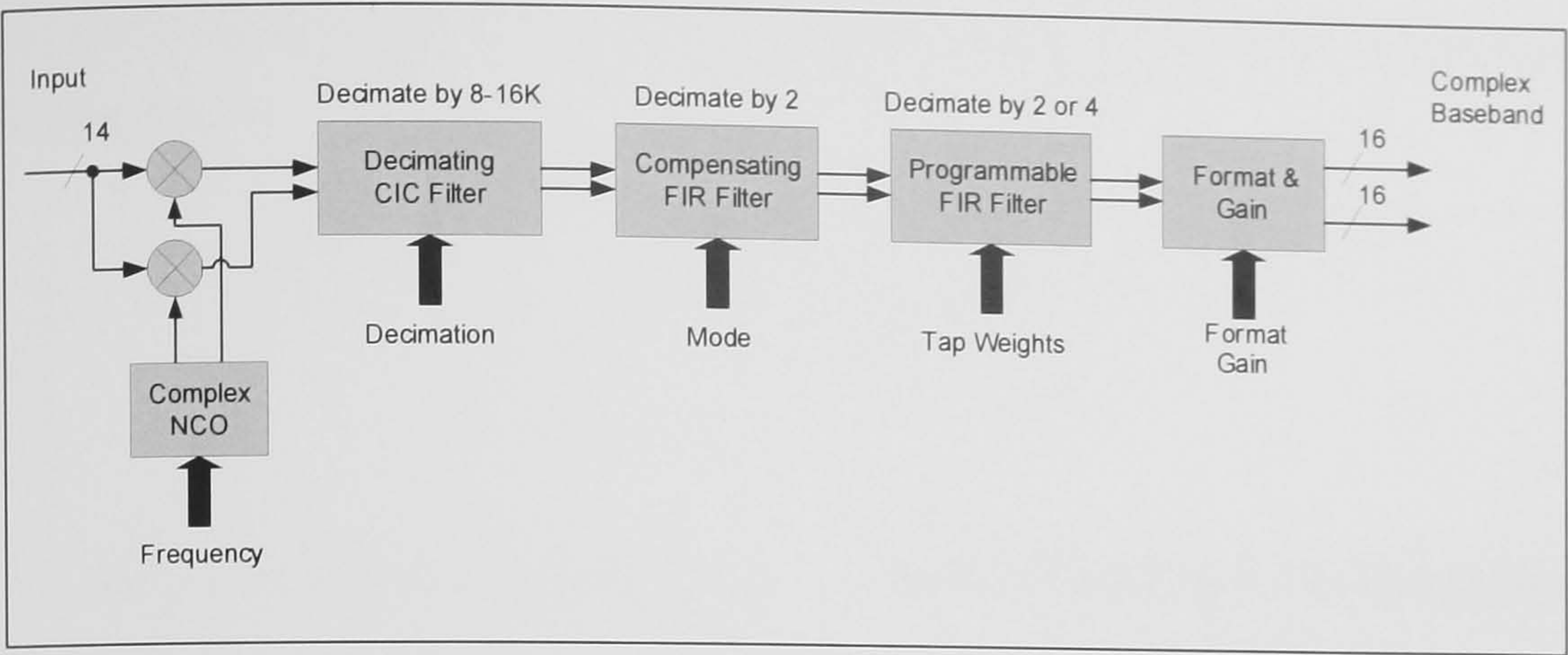


Figure 6-11 Programmable Digital Down-Converter [after Graychip, 124]

The GC4014 NCO (Figure 6-12) maintains a 32-bit phase address register which it uses to access a 16384 value (2^{14}) sine/cosine look-up table to generate 16-bit output samples. The finite look-up table word-length leads to periodic errors which manifest themselves as spurious NCO outputs. In an analogous manner to the techniques used to improve ADC spurious performance, a digital noise signal (dither) can be applied to improve the SFDR.

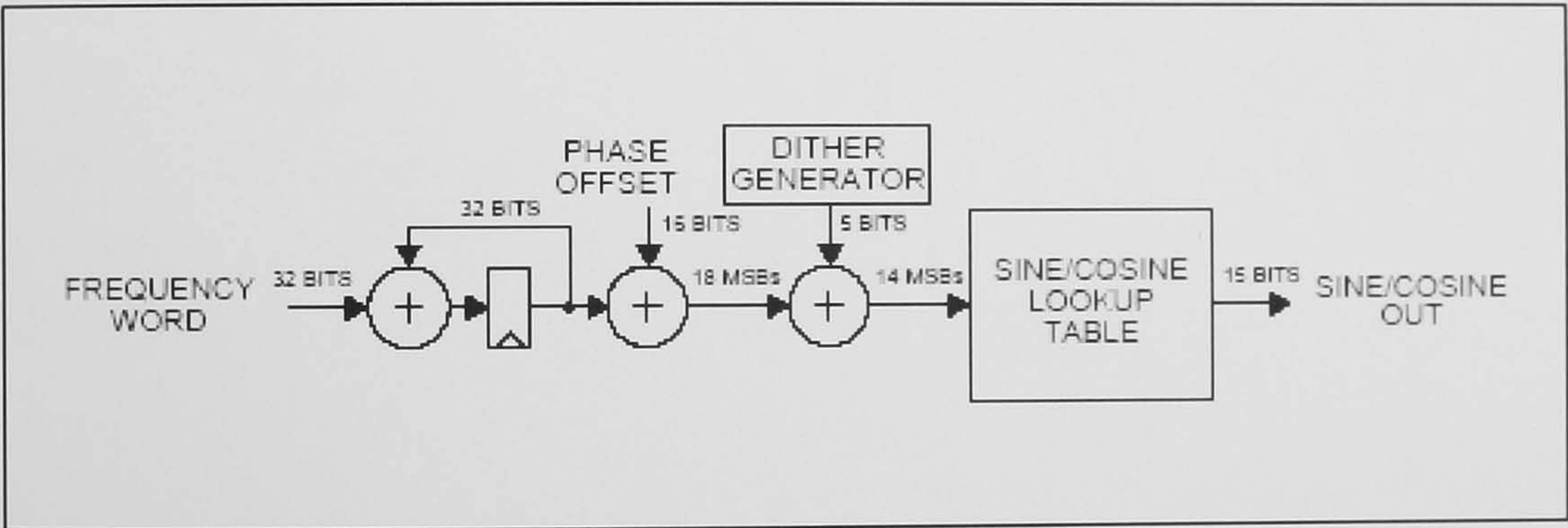


Figure 6-12 GC4014 DDC NCO Implementation [Graychip, 124]

The GC4014 NCO performance, taken from the data sheet, is reproduced in Figure 6-13. Without dithering the worst case spurs occur at -82 dBc (Figure 6-13a) whilst, with dithering applied, the majority of spurs fall below -105 dBc (Figure 6-13b). Without dither the worst case NCO spurs occur at -82 dBc, such as the one shown in Figure 6-13c, and are due to a few frequencies that are related to the sampling frequency by small rational numbers (e.g. $\frac{3}{16} * F_s$). In these cases the rounding errors in the sine/cosine lookup table repeat in a regular fashion, thereby concentrating the error power at a single frequency, rather than spreading it across the spectrum. These worst case spurs can be avoided by selecting an initial phase that minimises the errors or by changing the tuning frequency by a small amount (50 Hz). The data sheet states that all

spurs can be made to fall below -96 dBc with the selection of a proper initial phase or tuning frequency.

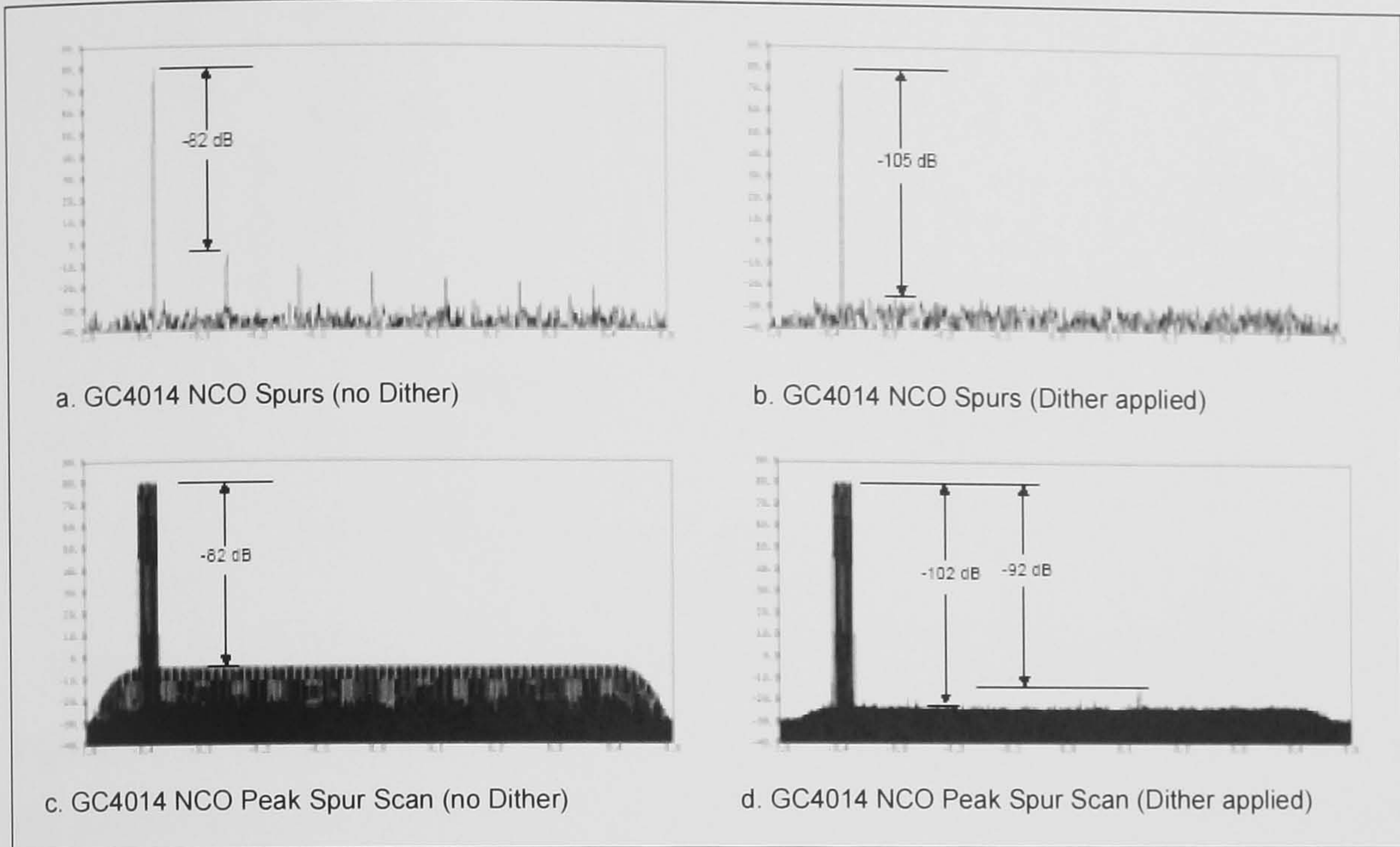


Figure 6-13 GC4014 Numerically Controlled Oscillator (NCO) Spurs [Graychip, 124]

The CIC output is filtered by two stages of filtering. The first stage is the CFIR, which compensates for the slope of the CIC pass band and provides close-in selectivity. One of two sets of (ROM based) coefficients may be selected. The set of coefficients used in the ‘normal’ mode give a pass-band which is flat (0.01 dB ripple) over 100% of the final output bandwidth and which has 85 dB of out of band rejection. The ‘narrow’ mode coefficients provide >110 dB out of band rejection at the expense of halving the useful output bandwidth. The second stage decimate-by-two or four PFIR filter uses either internal ROM based coefficients, or externally downloaded filter coefficients. The internal 80% bandwidth PFIR filter provides 80 dB of out of band image rejection and 0.03 dB peak-to-peak pass-band ripple.

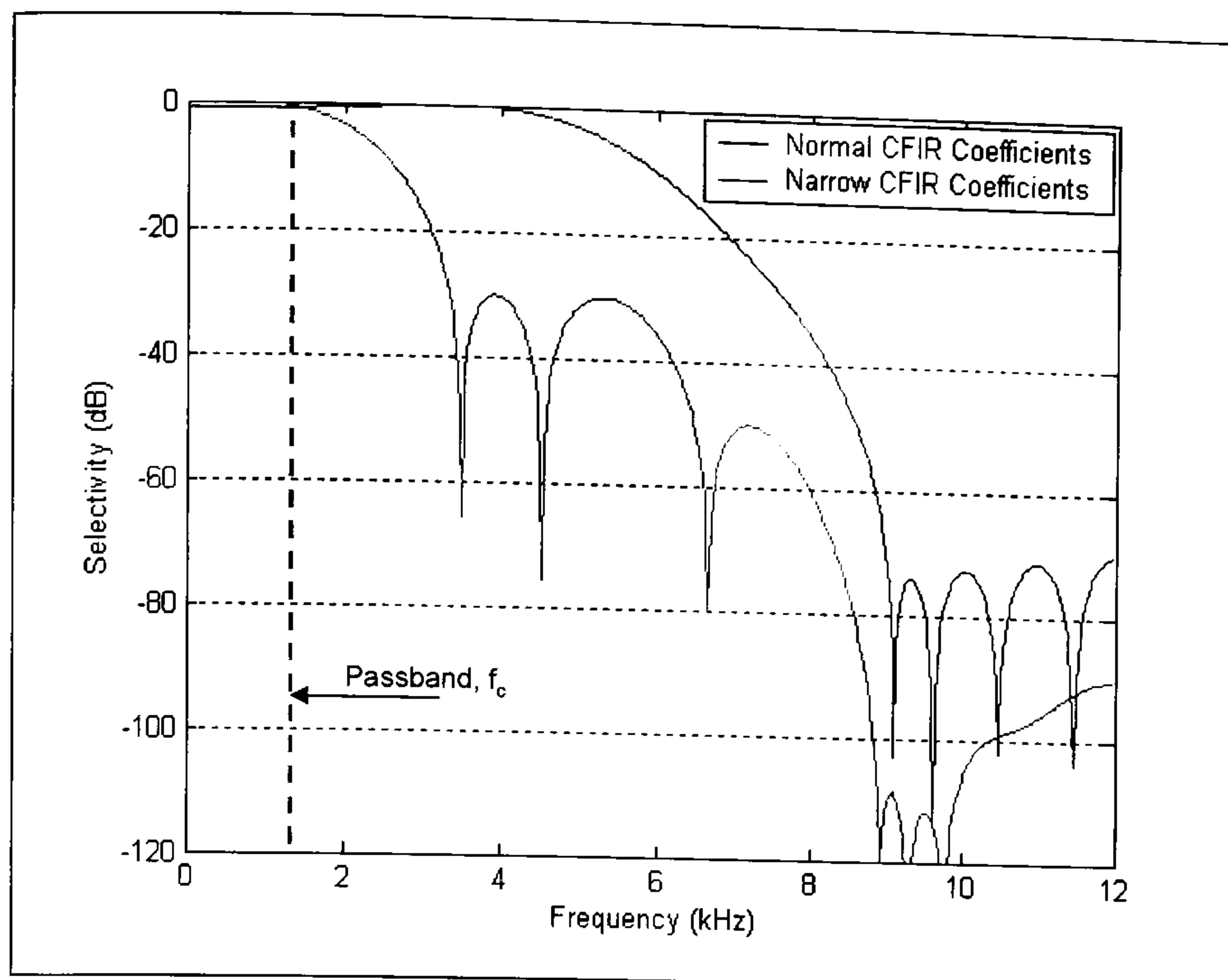


Figure 6-14 Frequency Response of GC4014 CFIR Filter (3 kHz Nyquist bandwidth)

Figure 6-15a shows the overall DDC selectivity in the normal mode and Figure 6-15b in the narrow mode (as modelled in MATLAB using the GC4014 CIC, CFIR and PFIR filter specifications). The DDC implementation is designed such that the peaks in the stop band at 3.5 times the output sample rate will, after decimation, fold into the transition band from 0.4 to 0.5 of the output sample rate. This out of band power can be filtered out by either using a custom PFIR filter with a narrower pass band, or by post-filtering the DDC output.

In summary the GC4014 DDC used in the prototype receiver is able to provide >110 dB selectivity within the centre of the pass band and a SFDR of ≥ 102 dB (typically 105-110 dB).

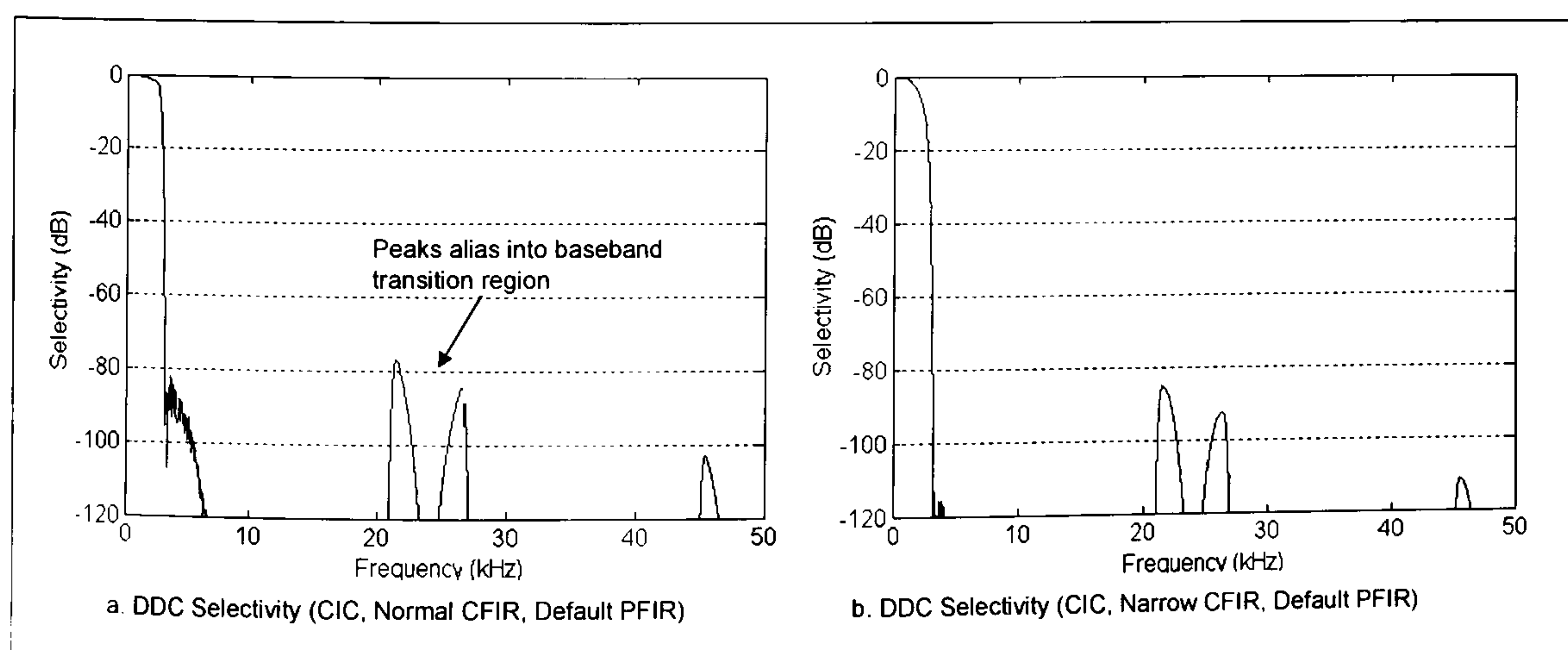


Figure 6-15 Modelled Performance of GC4014 DDC (3 kHz Nyquist bandwidth)

6.2 Predicted Performance of Prototype Digital HF Receiver

Following an examination of the major components in the digital receiver that effect performance, a cascaded parameter analysis has been undertaken to predict the performance of the prototype receiver that has been constructed. The results of this are given in Table 6-3 which has been repeated for inputs of -113 dBm and -10 dBm, which is the predicted ADC clipping level (0 dBFS). The key predicted performance parameters that come from this analysis are as follows: NF=16 dB, $IP3_{IN}=+19$ dBm, $IP2_{IN}=+27$ dBm, BDR=110 dB. The 3 kHz channel BDR is predicted to be ~110 dB (determined by the ADC noise floor). The previous analysis indicated that the DDC will provide an IDR of ~115 dB in 1 Hz bandwidth (80 dB in 3 kHz) but this may be placed wherever it is required (by programming the DDC gain) without impacting the front-end performance.

Digital HF Receiver - Cascaded Nominal Input/Output Parameters												
Analysis for Direct Sampling Architecture - using SNA-586 RF Amplifier												
Cumulative Output Summary												
Device Parameters (@ Output)												
Component Designation	Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P[saq] (dBm)	P[sig] (dBm)	P[n] (dBm/Hz)	SNR (dB)	DR (dB)	SFDR (dB)		
	15.35	15.57	43.38	35.82	4.80	-97.65	-142.93	45.28	147.73	119.16		
Cumulative Parameters												
Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P[saq] (dBm)	P[sig] (dBm)	P[n] (dBm/Hz)	SNR (dB)	DR (dB)	SFDR (dB)			
-2.00	0.00	1000.00	100.00	21.00	-115.00	-175.85	60.85	196.85	183.90			
-2.55	0.00	85.00	48.00	20.45	-115.55	-176.40	60.85	196.85	149.60			
-4.55	0.00	44.89	39.03	18.45	-117.55	-178.40	60.85	196.85	144.95			
15.95	9.17	44.21	36.98	19.00	-97.05	-148.73	51.68	167.73	123.81			
15.65	9.17	43.91	36.68	18.70	-97.35	-149.03	51.68	167.73	123.81			
15.35	9.17	43.61	36.38	18.40	-97.65	-149.33	51.68	167.73	123.81			
15.35	15.57	43.60	35.82	4.80	-97.65	-142.93	45.28	147.73	119.16			
Notes:												
1 Driving SNA-586 at 85 mA.												
2 Assuming use of dither to provide 110 dB SFDR												

Digital HF Receiver - Cascaded Nominal Input/Output Parameters												
Analysis for Direct Sampling Architecture - using SNA-586 RF Amplifier												
Cumulative Output Summary												
Device Parameters (@ Output)												
Component Designation	Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P[saq] (dBm)	P[sig] (dBm)	P[n] (dBm/Hz)	SNR (dB)	DR (dB)	SFDR (dB)		
	15.35	15.57	43.38	35.82	4.80	5.35	-142.93	148.28	147.73	119.16		
Cumulative Parameters												
Gain (dB)	NF (dB)	IP2 (dBm)	IP3 (dBm)	P[saq] (dBm)	P[sig] (dBm)	P[n] (dBm/Hz)	SNR (dB)	DR (dB)	SFDR (dB)			
-2.00	0.00	1000.00	100.00	21.00	-12.00	-175.85	163.85	196.85	183.90			
-2.55	0.00	85.00	48.00	20.45	-12.55	-176.40	163.85	196.85	149.60			
-4.55	0.00	44.89	39.03	18.45	-14.55	-178.40	163.85	196.85	144.95			
15.95	9.17	44.21	36.98	19.00	5.95	-148.73	154.68	167.73	123.81			
15.65	9.17	43.91	36.68	18.70	5.65	-149.03	154.68	167.73	123.81			
15.35	9.17	43.61	36.38	18.40	5.35	-149.33	154.68	167.73	123.81			
15.35	15.57	43.60	35.82	4.80	5.35	-142.93	148.28	147.73	119.16			
Notes:												
1 Driving SNA-586 at 85 mA.												
2 Assuming use of dither to provide 110 dB SFDR												

Table 6-3 Predicted Performance of Prototype Wideband Direct Sampling HF Receiver

6.3 Prototype Receiver Performance Measurements

Following construction the performance of the prototype receiver has also been characterised by undertaking a series of measurements. The complex baseband signal was streamed to disk from the output of the receiver's DDC. This was then analysed using MATLAB. The results presented here are from measurements made without the front-end filtering and protection module. The following measurements were made to establish the basic receiver performance:

- Impact of dither on ADC SFDR;
- Receiver sensitivity (noise figure);
- Third order intermodulation products;
- Second order intermodulation products;
- Harmonic performance;
- Receiver SFDR;
- Blocking Dynamic Range (BDR) and Instantaneous Dynamic Range (IDR);
- 62.208 MHz sampling clock phase noise; and
- Under-sampling (sub-octave sampling) performance.

6.3.1 Impact of Dither on ADC SFDR

In order to assess the benefit of adding dither to the input of the ADC input to improve its linearity, two -30 dBm (equivalent to -20 dBFS for the ADC) signals (11.0 MHz and 11.01 MHz) were applied to the receiver. Figure 6-16 shows that, with the receiver's dither generator switched on, the power of spurious signals decreased from -80 dBc (-100 dBFS) to approximately -90 dBc (-110 dBFS). The dither level used (set by commanding a DAC which in turn set the gain of a voltage controlled amplifier) was determined empirically – the level being increased until no further SFDR improvement was seen. The results measured agree with the improvement predicted from the analysis presented earlier.

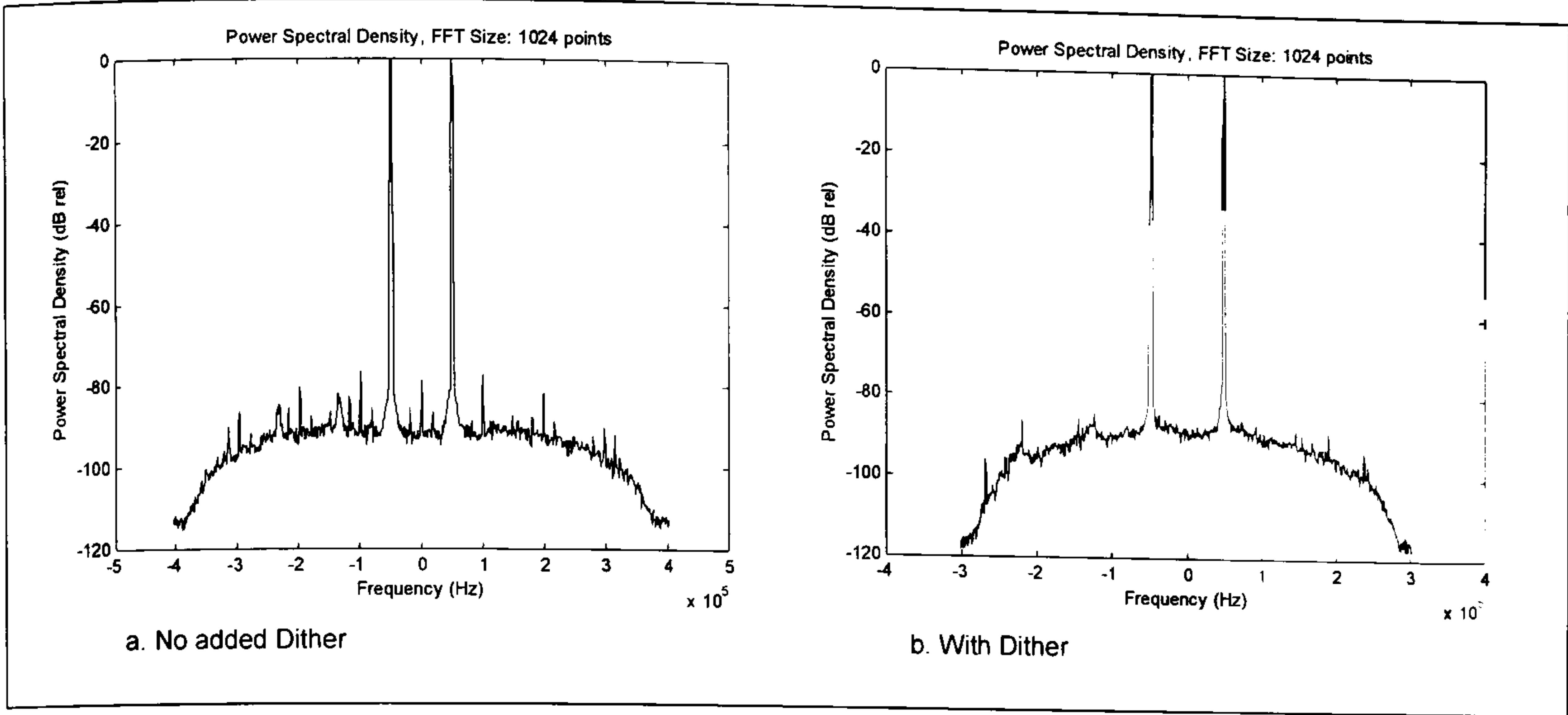


Figure 6-16 Effect of Adding Dither to ADC Input Signal (Input tones are -20 dBFS)

6.3.2 Receiver Sensitivity

With the receiver bandwidth set to 1 kHz a single RF tone was applied and its level reduced until its output was 45 dB above the noise floor (equivalent to an SNR of 10 dB in 3 kHz). The required input signal level to achieve this was -113 dBm (see Figure 6-17), giving a noise floor of -158 dBm/Hz. This accorded closely with the predicted receiver sensitivity.

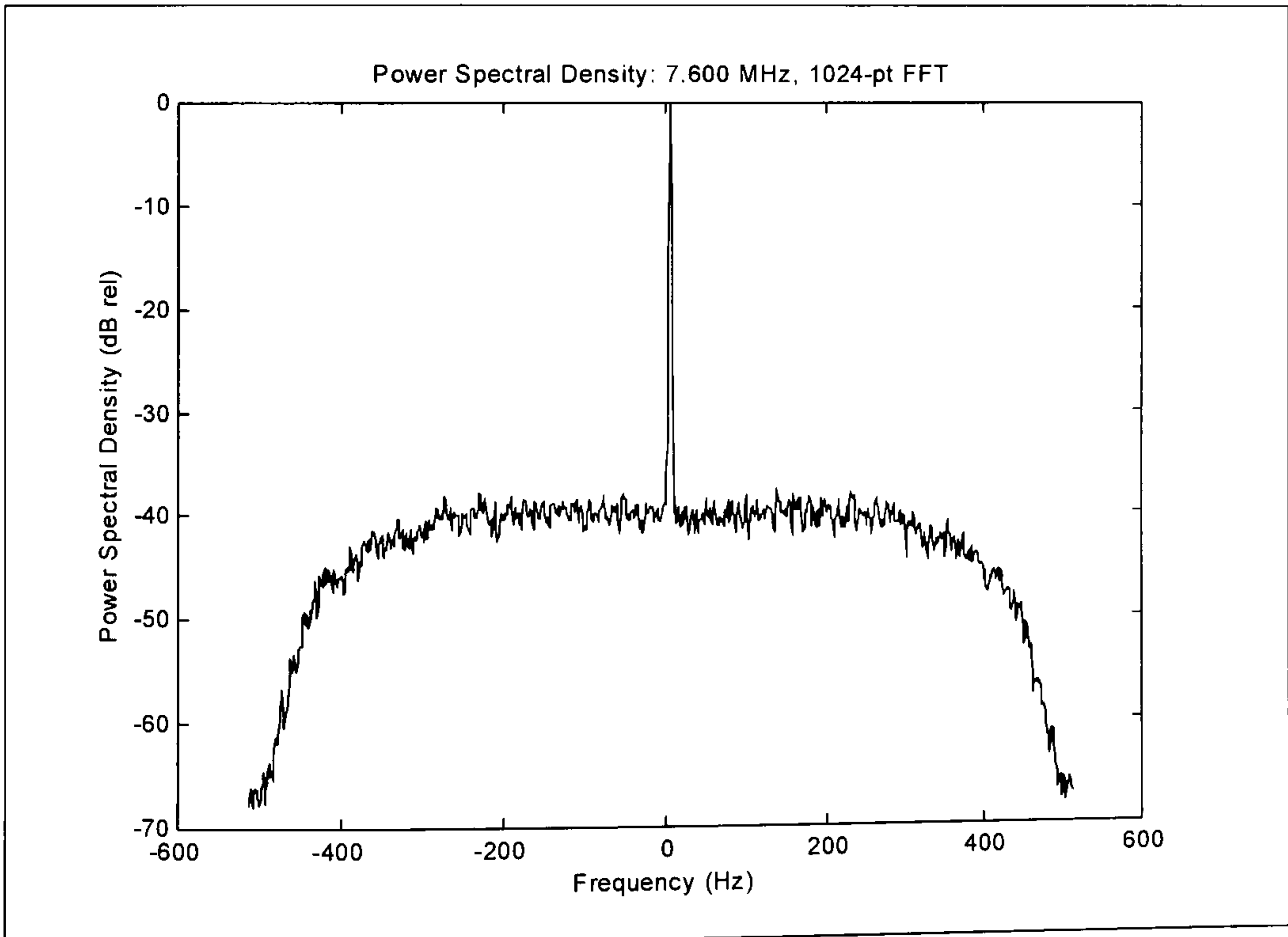


Figure 6-17 Measured Digital Receiver Sensitivity: -158 dBm Hz

6.3.3 Third Order Intermodulation Products

Using two signal generators, two -20 dBm tones were applied to the receiver at a separation of 20 kHz. The third order intermodulation product could then be clearly seen when the Fourier transform of the receiver output was taken (Figure 6-18). A spurious output of -78 dBc is equivalent to a third order intercept point of $+19$ dBm.

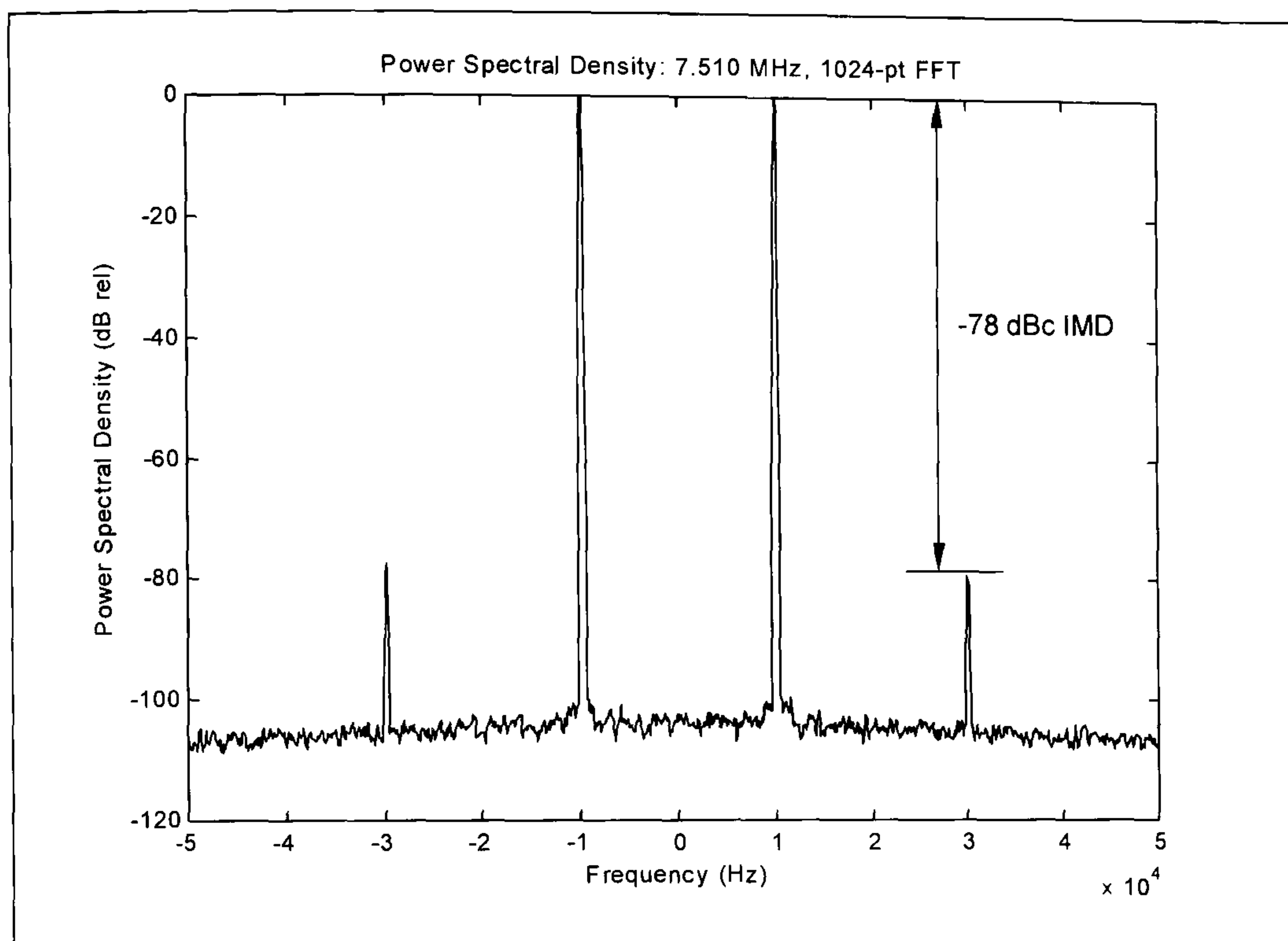


Figure 6-18 Measured Digital Receiver IMD using 2 tones at -20 dBm

6.3.4 Second Order Intermodulation Products

The second order intermodulation performance of the receiver was measured using two -15 dBm input tones at 6.3 MHz and 7.2 MHz. This resulted in a 2nd order IMD product of -57 dBm at 14.5 MHz. Hence $IP2_{IN}$ was calculated to be $+27$ dBm. The 2nd order nature of these products was confirmed because a 1 dB change in the input signal level resulted in a 2 dB change in the IMD level.

6.3.4.1 Harmonic Products

The harmonic performance of the receiver was found to accord closely with the results presented earlier for the harmonic performance of the RF amplifier (see 6.1.2).

6.3.5 Blocking Dynamic Range (BDR) and Instantaneous Dynamic Range (IDR)

The receiver's maximum input signal level was confirmed by applying an RF tone and increasing its power until the ADC overload indicator was activated. The power required to do this was -13 dBm. Given the measured noise floor of -158 dBm/Hz this gives the receiver a BDR of 145 dB.

The IDR was measured by applying a -15 dBm signal to the receiver, and adjusting the gain in the down-converter to maximise its dynamic range. The result of this test is shown in Figure 6-19. As can be seen the IDR is 115 dB which is less than the BDR and is limited by the DDC performance (word length, NCO performance etc) as previously discussed. Since the output the DDC is programmable it is always possible to adjust its gain to maximise the IDR for the signal power in the selected channel (frequency/bandwidth).

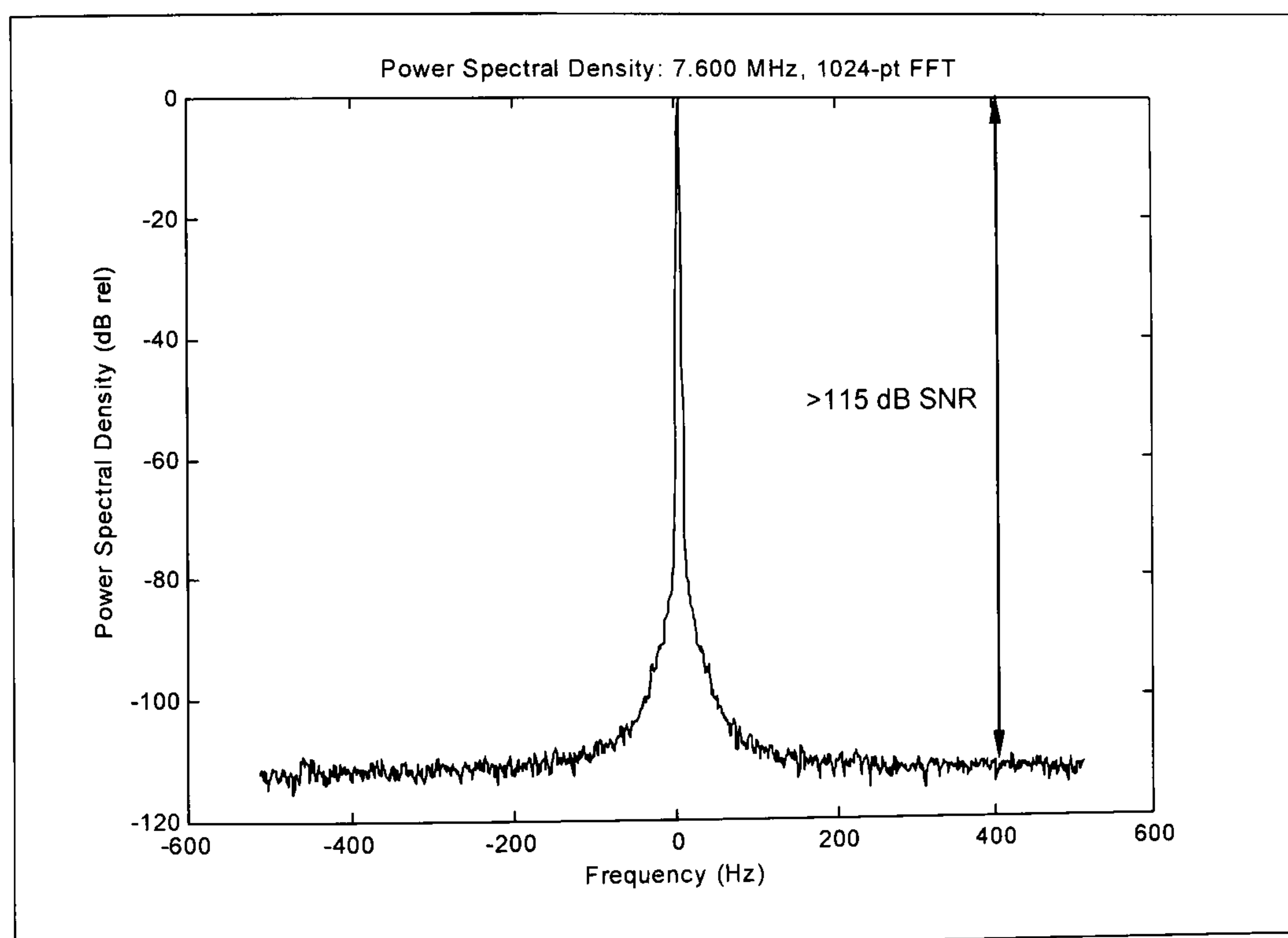


Figure 6-19 Measured Receiver Instantaneous Dynamic Range with -15 dBm input

6.3.6 Performance of 62.208 MHz Sampling Clock Generator

A prototype of the 62.208 MHz phase locked master oscillator was constructed and tested by using it as the sampling clock source on the prototype receiver. A high quality signal generator was used to provide a test tone and the received signal spectrally analysed in Matlab. The measured oscillator performance is as shown in Figure 6-20 to Figure 6-22. Figure 6-20 shows the phase noise of the VCXO free-running. In Figure 6-21 it is shown phase-locked to the TCXO improving its performance. In Figure 6-22 the performance when the VCXO is phase locked to the TCXO which is, in turn, phase locked to an external high quality frequency standard (some very low level spurs, probably due to the PLL, are evident in this case). This demonstrates that near ideal performance was achieved with the close-in phase noise being determined by the 10 MHz TCXO reference oscillator and, outside of the loop bandwidth, by the 62.208 MHz VCXO.

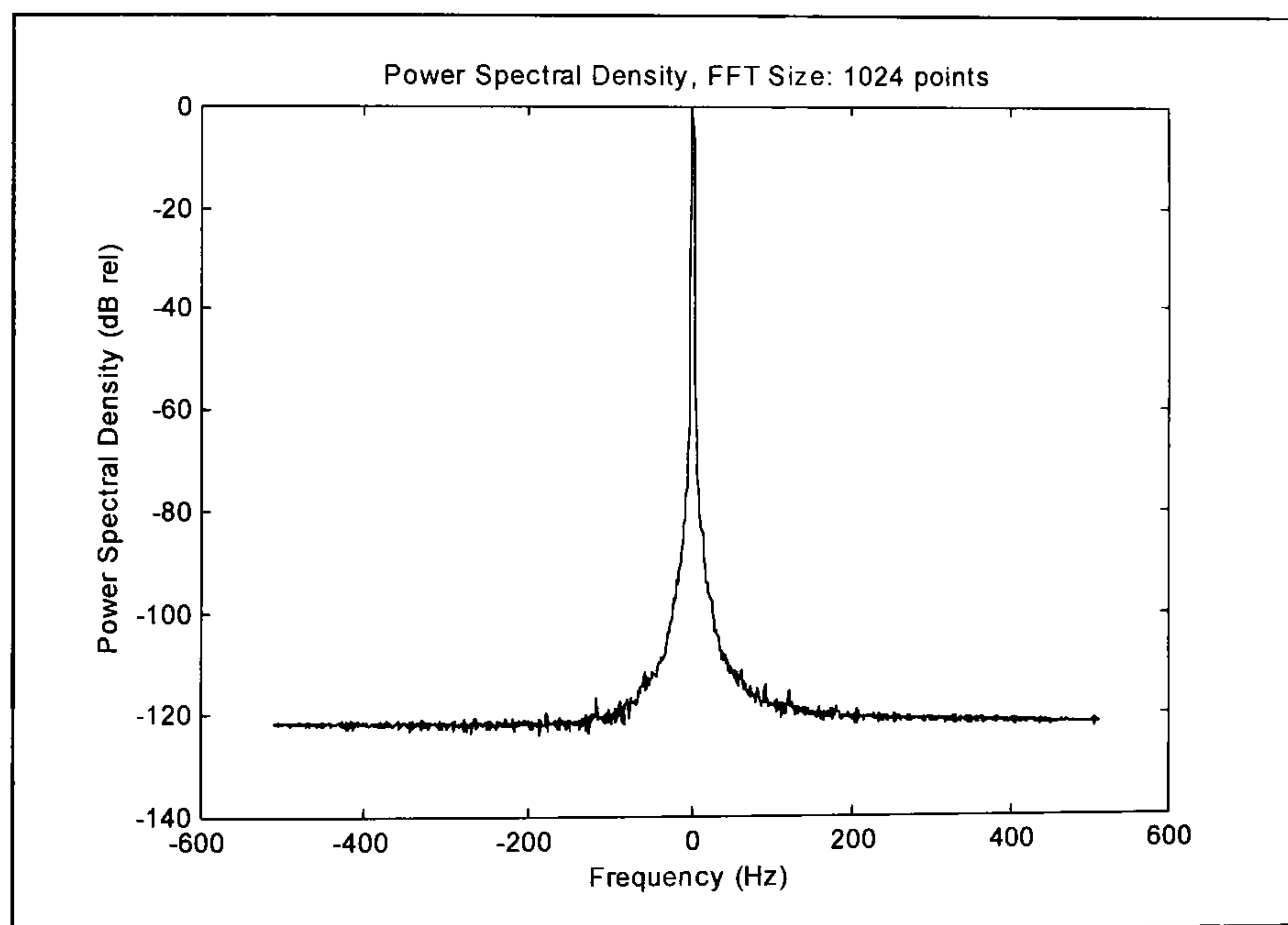


Figure 6-20 62.208 MHz Sampling Clock Phase Noise (Free Running)

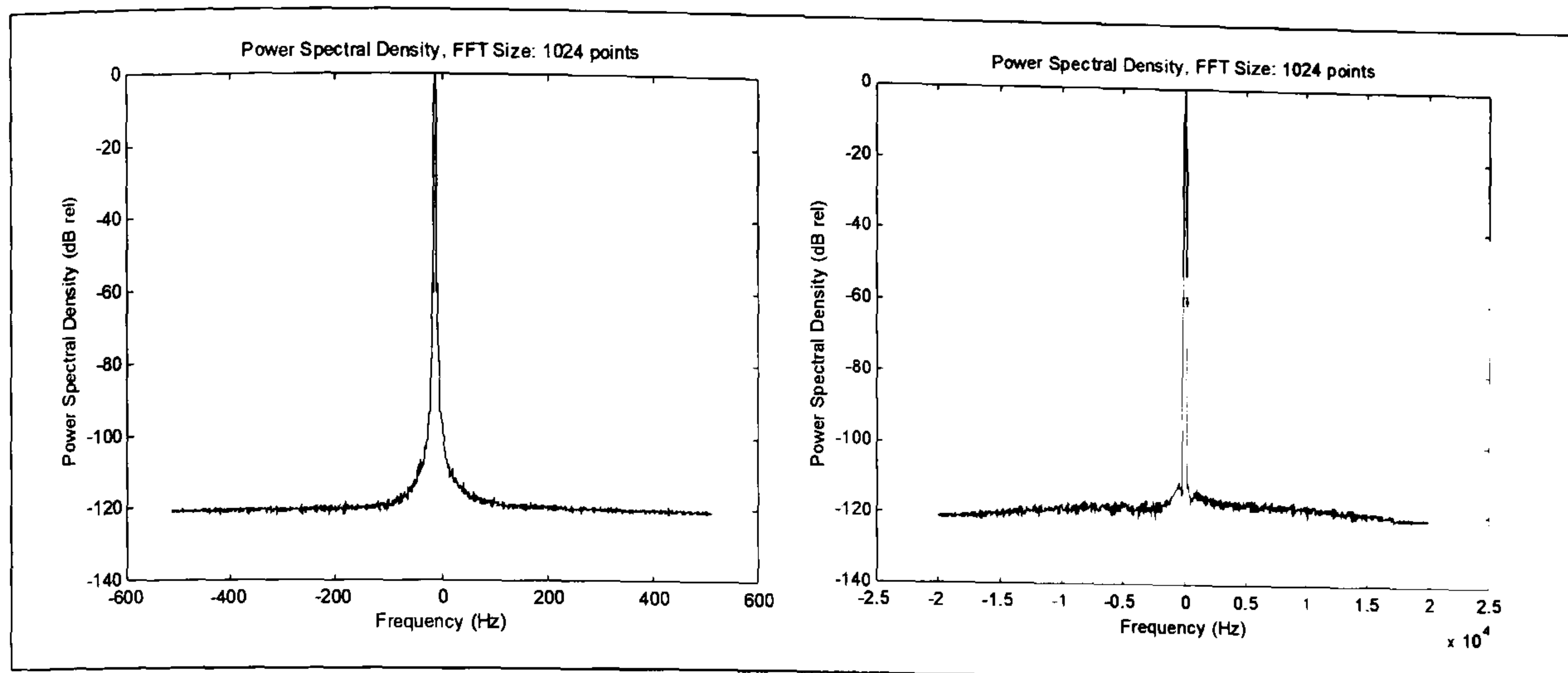


Figure 6-21 62.208 MHz Sampling Clock Performance (VCXO locked to TCXO)

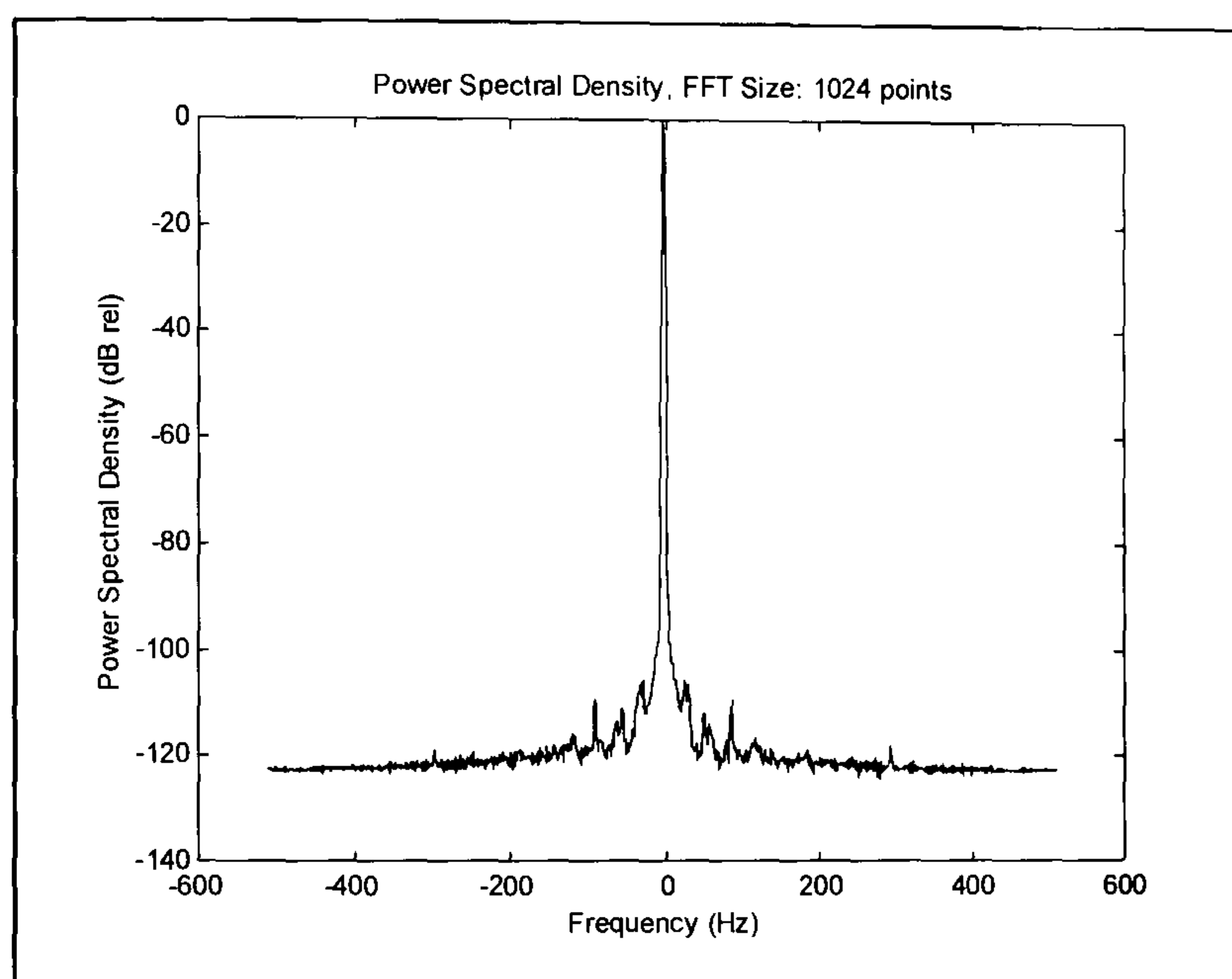


Figure 6-22 62.208 MHz Sampling Clock Phase Noise (VCXO/TCXO/Ext. Standard)

6.3.7 Under-Sampling Performance – VHF/UHF Applications

The wideband digital receiver design is flexible and capable of wider application. The basic receiver was designed to allow signals within the full analogue bandwidth of the ADC, ~250 MHz, to be utilised. The large analogue bandwidth makes it suitable for under-sampling applications. Hence the wideband digital receiver architecture could be used as the final IF/digital stages in VHF and higher frequency radios. In order to meet the Nyquist criteria the signal applied to the receiver must be externally band-pass filtered to ensure that it is not wider than $F_s/2$ (i.e. ~31 MHz). The under-sampling performance of the prototype receiver was evaluated (with the pre-ADC harmonic filter removed) using a -15 dBm 200 MHz input tone and found to be close to the expected

theoretical performance (see Figure 6-23). Note that when under-sampling an input signal the impact of phase noise (jitter) increases with frequency (as discussed in 5.8.3). This manifests itself as a reduction in SNR.

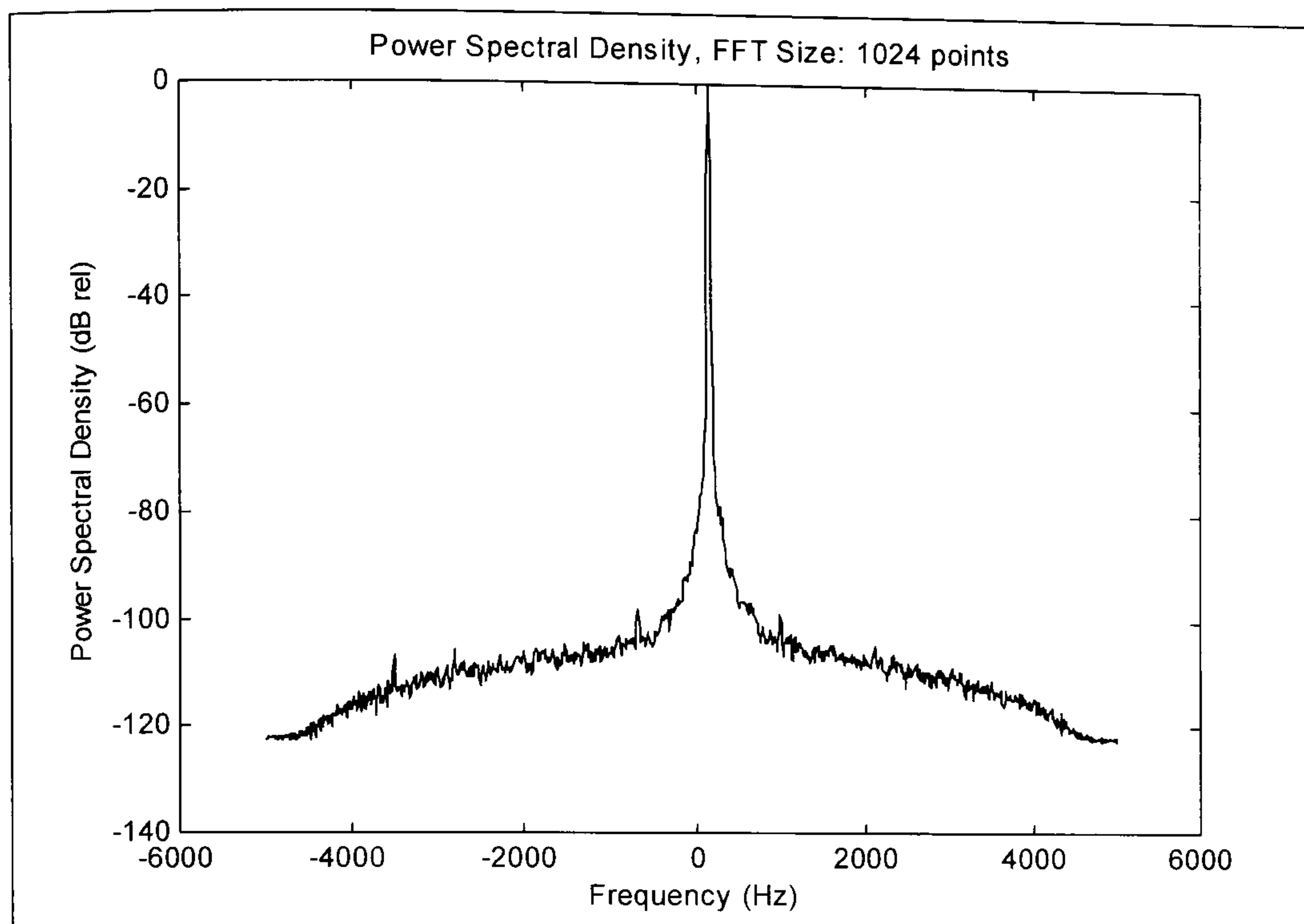


Figure 6-23 Receiver Under-sampling Performance: -15 dBm input at 200 MHz

6.3.8 Discussion of Prototype Direct Sampling HF Receiver Performance

The prototype receiver performance was found to accord closely to that predicted in all respects (measured as $NF=17$ dB, $IP3_{IN}=+20$ dBm, $IP2_{IN}=+27$ dBm, $BDR(3\text{ kHz})=110$ dB, $IDR=115$ dB). The receiver sensitivity, BDR and 3rd order IMD are all good and directly comparable with good conventional narrowband receivers. The IDR is excellent and typically 35 dB better than a conventional narrowband receiver. IDR, which implies linear gain through the receiver, is of particular importance where absolute signal strength is important (e.g. in a channel sounder) or where AGC is undesirable. However, as the performance predictions showed, the 2nd order IMD and harmonic performance of the RF amplifier used in the prototype receiver fell significantly short of optimal for good strong signal handling. The performance achieved is not a fundamental limitation of the architecture but is directly related to the RF amplifier used.

6.4 Improving the Performance of the Prototype Receiver

The following paragraphs consider how the performance of the digital receiver may be improved.

6.4.1 Rejection of Sub-HF Frequencies

Numerous broadcasters transmit high power signals at long-wave and medium-wave frequencies (LF and MF). Further, the noise floor at LF/MF is significantly higher than at higher frequencies. For a receiver intended for solely HF operation it would be useful to include pre-selection filtering to reject these lower frequencies as it would reduce harmonic and IMD. It is worthy of note that the prototype inherently provides additional rejection due to poorer filter and RF amplifier matching at these out-of-band frequencies.

6.4.2 Use of a Higher Performance RF Amplifier

It is clear from both the analysis and measurement results presented that the performance of the direct sampling receiver prototype is limited by the linearity of the RF amplifier that was used. A search of the literature and specifications for commercially available high intercept point amplifiers has provided information on a number of suitable devices (or with sufficient expertise a suitable amplifier could be designed and build). Alternative RF amplifier configurations such as those utilising a higher operating voltage and so providing a greater linear voltage swing range, balanced push-pull designs (with inherent second order harmonic cancellation) and the use of linearisation techniques (e.g. feed-forward error cancellation) techniques are all potentially applicable.

Calculations were presented in the previous chapter, assuming the use of a type QB101 RF amplifier [Remec, 117]. The performance of this amplifier is compared with that of the SNA-586 used in the prototype receiver in Table 6-4. This indicates that it would be possible to construct a much higher performance whole-band direct sampling digital HF receiver and address the second order IMD performance, the major deficiency of the prototype receiver.

Parameter	RF Amplifier SNA-586	RF Amplifier QB101
Noise Figure	5.5 dB	4.5 dB
Gain	20.5 dB	21.9 dB
Output P1dB	+21 dBm	+31 dBm
IP3 _{IN}	+17 dBm	+32 dBm
IP2 _{IN}	+26 dBm	+83 dBm
Supply voltage	5 V	24 V
Supply Current	85 mA	420 mA

Table 6-4 RF Amplifier Performance Characteristics Compared

6.4.3 Benefit of ADCs with Higher Sample Rates

The performance of the ADC has a major impact on the performance of a digital receiver. In the time since the prototype receiver was built incremental technology developments have led to the availability of ADCs with similar dynamic performance to the converter used but in higher speed grades. The AD6645 from Analog Devices [Analog, 125], a derivative of the AD6644, allows operation at up to 105 MSPS. The principal benefit of employing higher sample rates in a direct sampling HF receiver is that it lessens the transition requirement in the front-end anti-aliasing filter. Whereas the prototype receiver allowed operation up to 28 MHz at full performance using a ~62 MSPS ADC a higher sampling rate would allow whole band coverage and significantly ease the filter design requirement. This would likely allow a reduced order filter to be used and thus make it easier to achieve good pass-band ripple and matching (VSWR).

6.4.4 Improving Digital Down-Converter Dynamic Range

It was previously noted that, once digitised, signal processing can be undertaken with an arbitrary level of fidelity. The performance of the GC4014 used in the prototype receiver provides >102 dB (typ. 105-110 dB) SFDR. More recent ASIC DDC implementations are able to provide slightly improved performance: >115 dB SFDR (e.g. [Graychip, 126]). They also have greater output word lengths (24-bit) reducing the need for gain adjustment in operation. More latterly it has been shown that the implementation of DDCs with similar performance is becoming practical within FPGAs

[Walke, 127]. Given the performance of available ADCs, with this level of performance the DDC will not limit the performance of a digital receiver.

6.5 Chapter Summary

A prototype wideband direct sampling digital HF receiver has been constructed and its performance measured. The results achieved (measured as $NF=17$ dB, $IP3_{IN}=+20$ dBm, $IP2_{IN}=+27$ dBm, $BDR(3\text{ kHz})=110$ dB and $IDR=115$ dB) were found to agree closely with those predicted/specified for the design. In general they are in accordance with the requirements for high performance HF receivers (discussed in Chapter 5). Whilst the prototype receiver implementation could have been improved in a number of respects as proposed (particularly 2nd order IMD performance) it demonstrated that, for the first time, a high performance wideband, direct-sampling digital HF receiver is a practical proposition.

The following chapter presents the design of a wideband digital HF transceiver (HF software radio) which incorporates the direct sampling HF receiver discussed in this chapter and a complementary digital HF transmitter exciter. Chapter 9 and Chapter 10 discuss an application of the wideband digital transceiver as an HF channel sounder and present results from on-air measurements.

Chapter 7.

A Wideband, Multi-Channel, HF Software Radio

This chapter describes a wideband, multi-channel, direct sampling digital HF transceiver that has been designed and constructed¹. It has been specifically designed as a highly re-configurable, software defined radio system. The previous chapter discussed the technical performance of its direct sampling digital HF receiver and presented measurement results. This chapter describes the overall transceiver design and implementation. Applications for which the digital transceiver system was designed include use as a multi-channel HF radio modem and as a platform on which to implement a flexible HF channel sounder to allow the characterisation of the HF environment. This latter use is described in Chapter 9.

¹ The implementation of such a complex system is a very significant piece of work. The hardware design of the digital transceiver is the author's own work. However, a number of others made significant contributions to realising a working system. In particular, Mike Bova of CRC designed and implemented the bus arbitration and local bus control logic in a CPLD. As part of this work he also implemented a number of software routines to permit communications with the board. Once the author had identified the placement of key components, Minh Huynh of CRC undertook the routing and placement of the transceiver PCB under the author's supervision. Also, a number of undergraduate students under the author's direction made useful contributions as detailed in the acknowledgements at the start of this thesis.

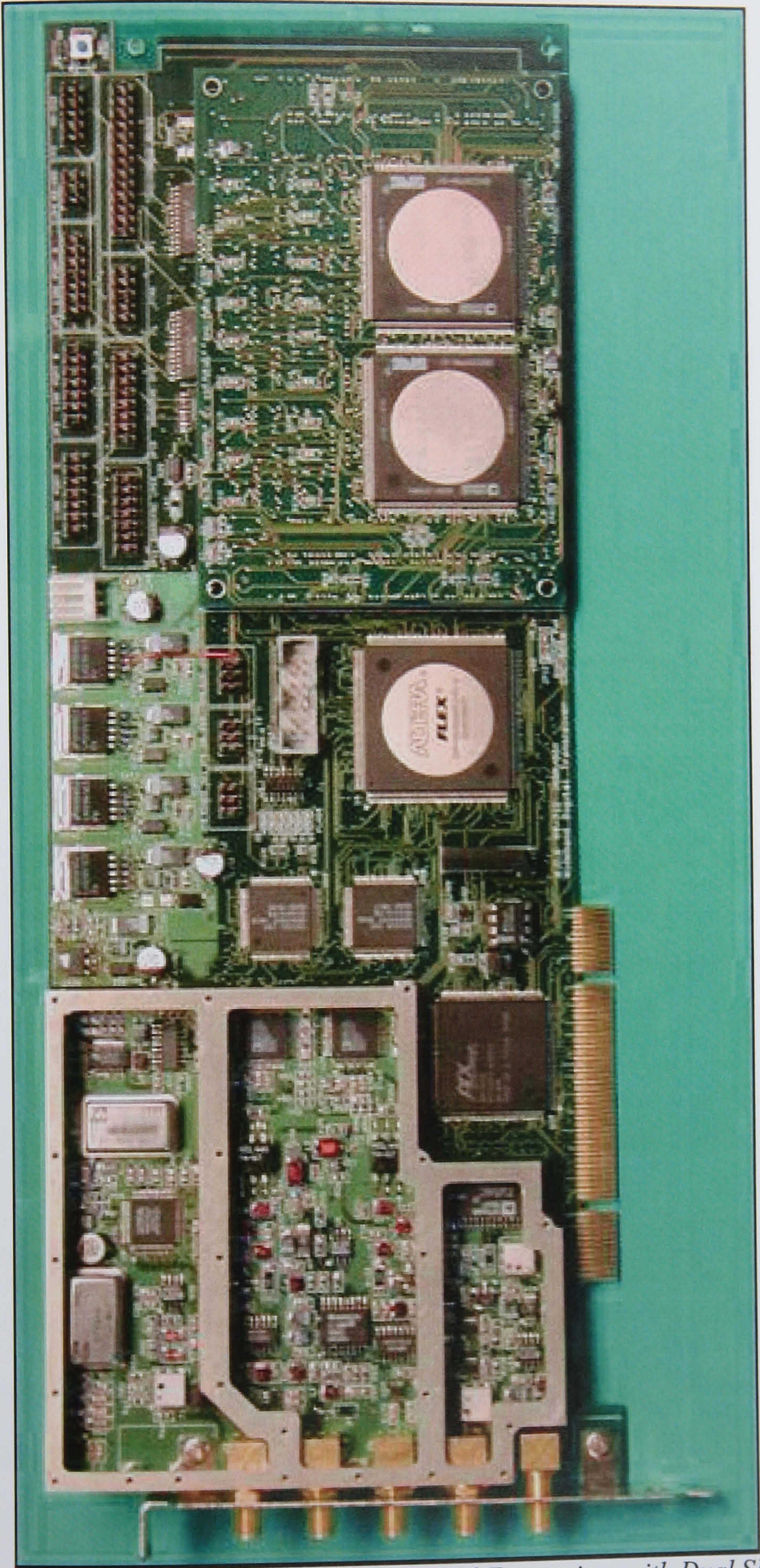


Figure 7-1 Prototype (Serial No. 001) Digital Transceiver with Dual SHARC DSP

7.1 Wideband Digital Transceiver Architecture

The digital transceiver hardware architecture (illustrated in Figure 7-2) has been designed to allow its functionality to be very largely defined through the download of application software and PLD configurations. The transceiver has been designed as a full length peripheral component interconnect (PCI) card which can be hosted in a conventional personal computer (PC). Application software may be downloaded from the host to the processors within the DSP sub-system. All interaction with the principal peripherals (e.g. digital transmitters and receivers) occurs via a large (100,000 gate) RAM based field programmable gate array (FPGA, [Brown, 128]). This device, termed the processing FPGA, can be used to perform additional high speed or time critical processing in hardware. It also allows data paths to be configured as required for any particular application. The host can download new configurations to this FPGA to implement application specific functionality.

The principal features of the digital transceiver are summarised below and described in more detail in the following sections:

- A PCI interface to allow the transceiver to be installed in a host PC;
- An architecture employing a local address/data bus with bus arbitration and multiple bus mastering;
- A high performance DSP sub-system module installed on a mezzanine site;
- A flexible architecture allowing software configuration and download of application software;
- A frequency standard sub-system responsible for generating stable, low phase-noise sampling clocks and other reference frequencies;
- 4-Channel digital HF receiver with diversity RF input;
- 4-Channel digital HF transmitter exciter;
- Digital interfaces including synchronous and asynchronous serial data interfaces;
- Built-in self test diagnostic capabilities; and
- A separate front-end protection and filter module.

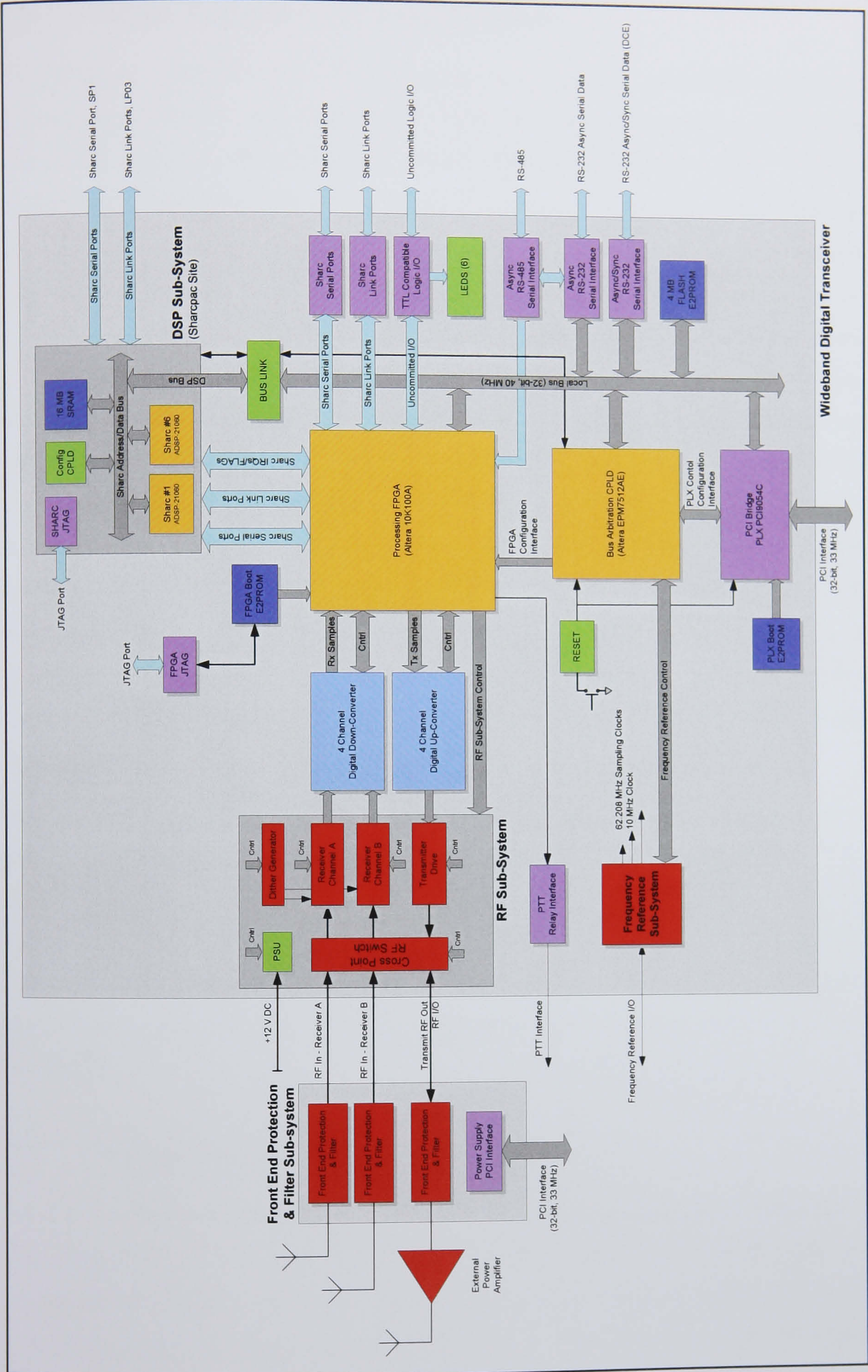


Figure 7-2 Architecture of Wideband Digital Transceiver

7.2 Digital Transceiver PCI Bus Interface

The wideband transceiver has been designed as a standard peripheral component interconnect (PCI, [PCI-SIG, 129], [Solari, 130]) card. This allows multiple transceiver cards to be hosted in, and controlled by, a standard personal computer (PC). PCI is a sophisticated, high bandwidth (132 Mbytes/s peak) bus which supports such features as multiple bus mastering, bridging, processor independence and some well defined software interfaces. Multiple bus mastering and background direct memory access (DMA) transfers allows data to be streamed to and from the PC host with minimal intervention and little impact on program execution speed. To minimise the development effort required the digital transceiver uses a commercial PCI bus interface ASIC (PLX9054 [PLX, 131]). This device utilises a small accompanying serial PROM which configures it at system start. The PLX9054 is a PCI interface adaptor capable of acting as both initiator and target for data transfers. It has dual DMA engines which can perform both block (contiguous memory) DMA transfers and scatter-gather DMAs (in which a descriptor list describes a series of chained block DMAs to be performed). It also supports simple messaging protocols between host and local bus using mailbox registers (effectively dual port registers accessible from either PCI or local bus) and doorbell registers (mailbox registers that can trigger an interrupt on being written).

The PLX9054 PCI interface device provides low-level hardware support for a commercially developed standard called Intelligent Input/Output (I₂O [I2O-SIG, 132]). This is a high performance data transfer technology and standardised protocol which is intended for use with PCI peripherals that must sustain large communications bandwidths (e.g. hard disk controllers). In the next chapter a new, high performance, event based processing architecture that makes use of this I₂O messaging capability is introduced.

7.3 Digital Transceiver Bus Arbitration CPLD

An Altera EPM7512 CPLD [Altera, 133] is used to manage the digital transceiver's local control/address/data bus (see Figure 7-2). The CPLD provides the logic and management required to interface to the local bus side of the PCI interface device. It also manages the bus interface to the DSP sub-system. The system is designed to allow

the host PC, the PLX9054 PCI interface device or one of the DSP sub-system processors to make a bus request, to become bus master and to orchestrate transactions.

A key requirement of the bus arbitration CPLD is to allow the software configuration of the processing FPGA. A memory-mapped configuration engine is implemented to allow host PC software to download configuration files to the FPGA. This is the preferred method of programming the FPGA.

The scope of the bus arbitration CPLD functionality has been carefully bounded such that once its design had been completed it did not need to be modified. It is the intention of the digital transceiver architecture that any application specific logic is implemented in the processing FPGA. For this reason a PROM based CPLD is used for the bus arbiter. It is programmed using a Joint Test Action Group (JTAG) boundary-scan compatible programmer [IEEE, 134].

In summary, the bus arbitration CPLD provides the following functionality:

- Local bus arbitration;
- Primary address decoding for digital transceiver peripherals;
- Interface to PCI bridge;
- Interface to DSP sub-system; and
- FPGA programming/configuration interface.

7.4 Digital Signal Processing (DSP) Sub-System

7.4.1 Choice of SHARC ADSP-2106x DSP Device

Analog Device's ADSP21060 Super Harvard Architecture (SHARC) processor device [Analog, 135] was selected for use in the digital transceiver DSP sub-system based on its overall processing performance, its high bandwidth interfaces and an architecture optimised for use in multi-processing solutions. The following specific capabilities have been exploited for the digital transceiver implementation:

- **Internal Architecture** – The processor internal architecture (Figure 7-3a) is optimised for high speed processing using an enhanced Harvard architecture¹ allowing the simultaneous access of separate program and data memories and utilising caching techniques. Further, a separate I/O processor and dual ported internal memory allows a high sustained input/output bandwidth. Multiple DMA engines allow data transfers (between internal memory, external memory and the high speed SHARC external interfaces) to be undertaken in the background with no software intervention (once initiated). A 40 MHz ADSP-2106x processor has a sustained processing performance of 80 million floating point operations per second (MFLOPS) and 120 MFLOPS peak using a floating point arithmetic logic unit (ALU).
- **High Speed Link Port Interfaces** – Each SHARC processor has six high speed 4-bit wide link port interfaces that can each transfer data at rates of 20 or 40 Mbytes/s under the control of a DMA engine with no loss of bandwidth to the processor's external bus.
- **High Speed Serial Ports** – Each SHARC processor has two high speed serial ports capable of 40 Mbits/s transfers under DMA control.
- **Cluster Processing** – The SHARC has specific design features to optimise its use in multi-processor cluster computing. The internal memory of each processor in a cluster (of up to six processors) is directly accessible by other SHARCs in the cluster and by host processors (Figure 7-3b). The use of dual ported internal memory means that these accesses do not cause bus conflicts with internal processing activities. Broadcast writes to the internal memory of all devices in a cluster are also possible (useful for multi-processor synchronisation, semaphores and spin-locks etc).

¹ First developed by Howard Aiken of IBM. In the Harvard architecture (as opposed to the *von Neuman*) instructions and data are stored in separate areas of memory. The first implementation of this architecture was in the 'Harvard MK 1' relay based computer built by IBM and shipped to Harvard University (hence the name) in 1944.

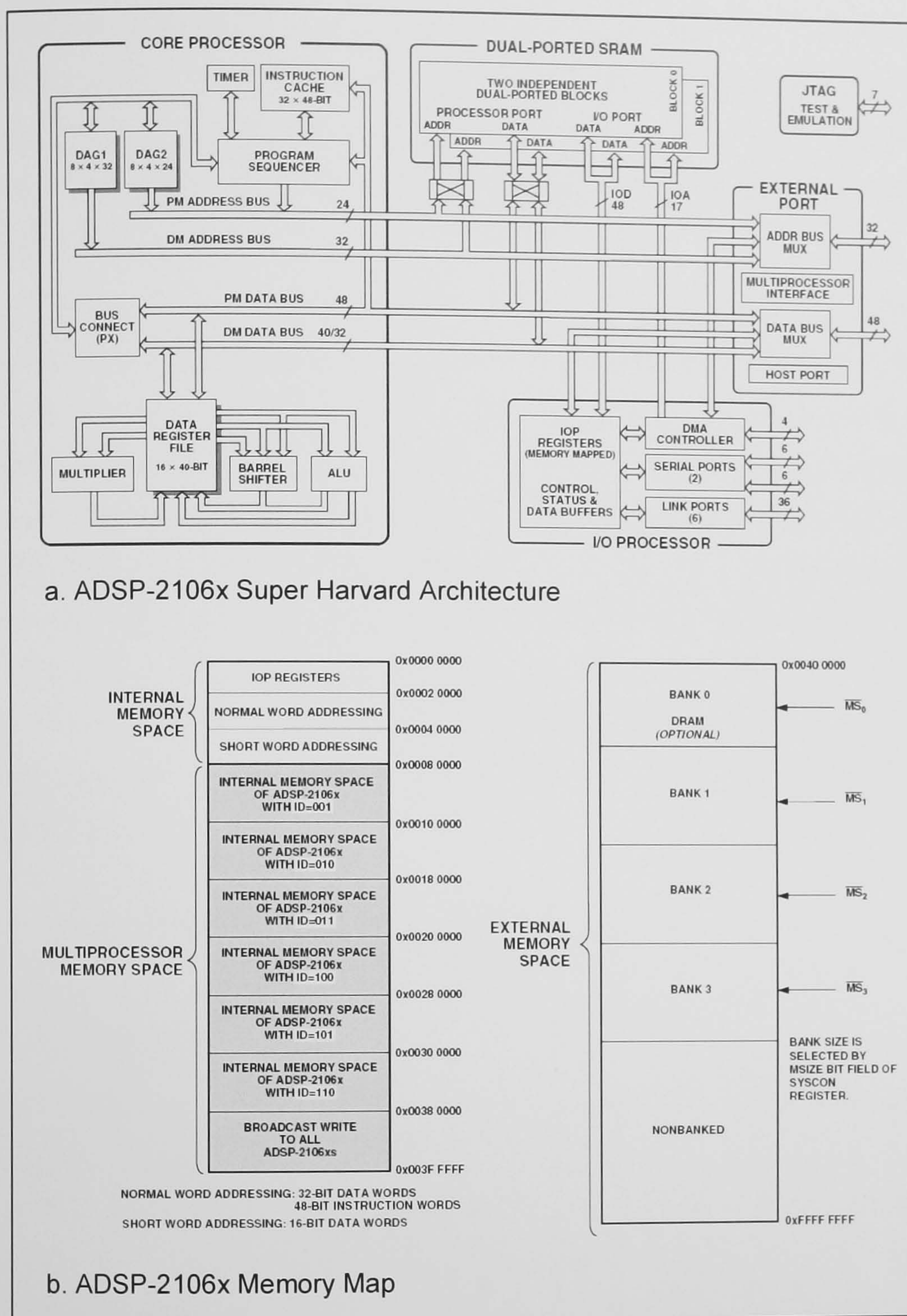


Figure 7-3 SHARC ADSP-2106x Architecture (from [Analog, 135])

7.4.2 DSP Sub-system Mezzanine Site (SHARCPAC Site)

A SHARCPAC [Bittware, 136] compatible mezzanine site is included on the transceiver board to allow the incorporation of a local, tightly coupled DSP sub-system. SHARCPAC modules, which are available commercially, have up to four processors. They are available with on-board, high speed local memory. The inclusion of a SHARCPAC compatible site allows modules with different processing/memory

capabilities to be installed to meet the needs of a given application without requiring hardware modifications to the main transceiver board. Although the SHARCPAC interface has been designed for use with SHARC processors it would be possible to develop a DSP sub-system module with alternative (i.e. more powerful) processors should the need arise.

The wideband transceiver board has been designed with a split local (control/address/data) bus architecture so that if a SHARCPAC module is installed, it may operate at full speed even whilst other transactions are taking place on the transceiver's local bus (see Figure 7-2). The two buses are only joined when transactions between the transceiver local bus and DSP sub-system are required. The bus link function employs high speed 2-port bus switches [Pericomm, 137] in preference to logic transceivers as this allows fully bi-directional operation and very low signal latencies. A dedicated power plane for the SHARCPAC site and a judicious choice of the bus switch power supply voltage allows the use of 5 V or 3.3 V DSP processor modules with the change of a single link (the main transceiver board logic is wholly 3.3 V).

7.5 Dual SHARC DSP Processor Module

7.5.1 Description

A DSP sub-system module (Figure 7-4), which attaches to the digital transceiver SHARCPAC site, has been developed to support the anticipated uses of the digital transceiver¹. This module is fitted with dual ADSP-21060L 40 MHz SHARC DSP processors and a large quantity (2 Mbits) of shared 48-bit wide fast (zero wait state) static random access memory (SRAM). The 40 MHz clock for the SHARC DSPs is supplied from the digital transceiver board via the SHARCPAC site. In order to minimise clock skew (a critical requirement for reliable multi-processor operation) a zero-delay clock buffer [ICS, 138] is used to phase lock to this signal and to generate the clocks

¹ Whilst commercial SHARPAC modules with one, two or four processors were commercially available, none had the large, high speed memory capacity expected to be needed for the real-time implementation of applications such as the channel sounder. For this reason, and given the experience that had to be gained in any case to implement the interface electronics for the SHARPAC site, it was decided to also develop the DSP module described.

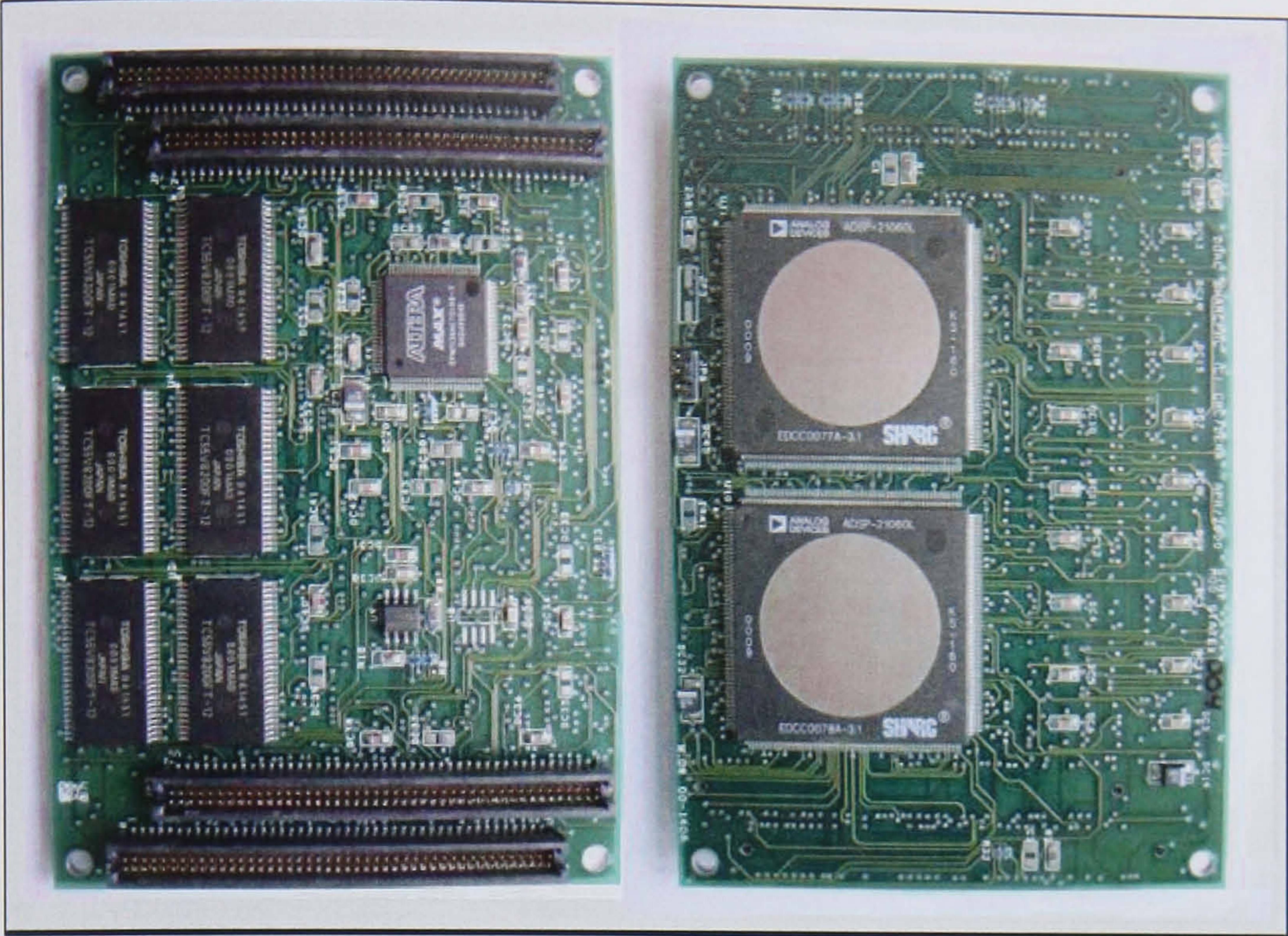


Figure 7-4 Dual SHARC Processor Module with 2Mx48 Shared Memory

Figure 7-5 illustrates how the two SHARC processors on the processing module are interconnected and which interfaces are fed through to the digital transceiver board. Table 7-1 shows how these are routed on the digital transceiver board.

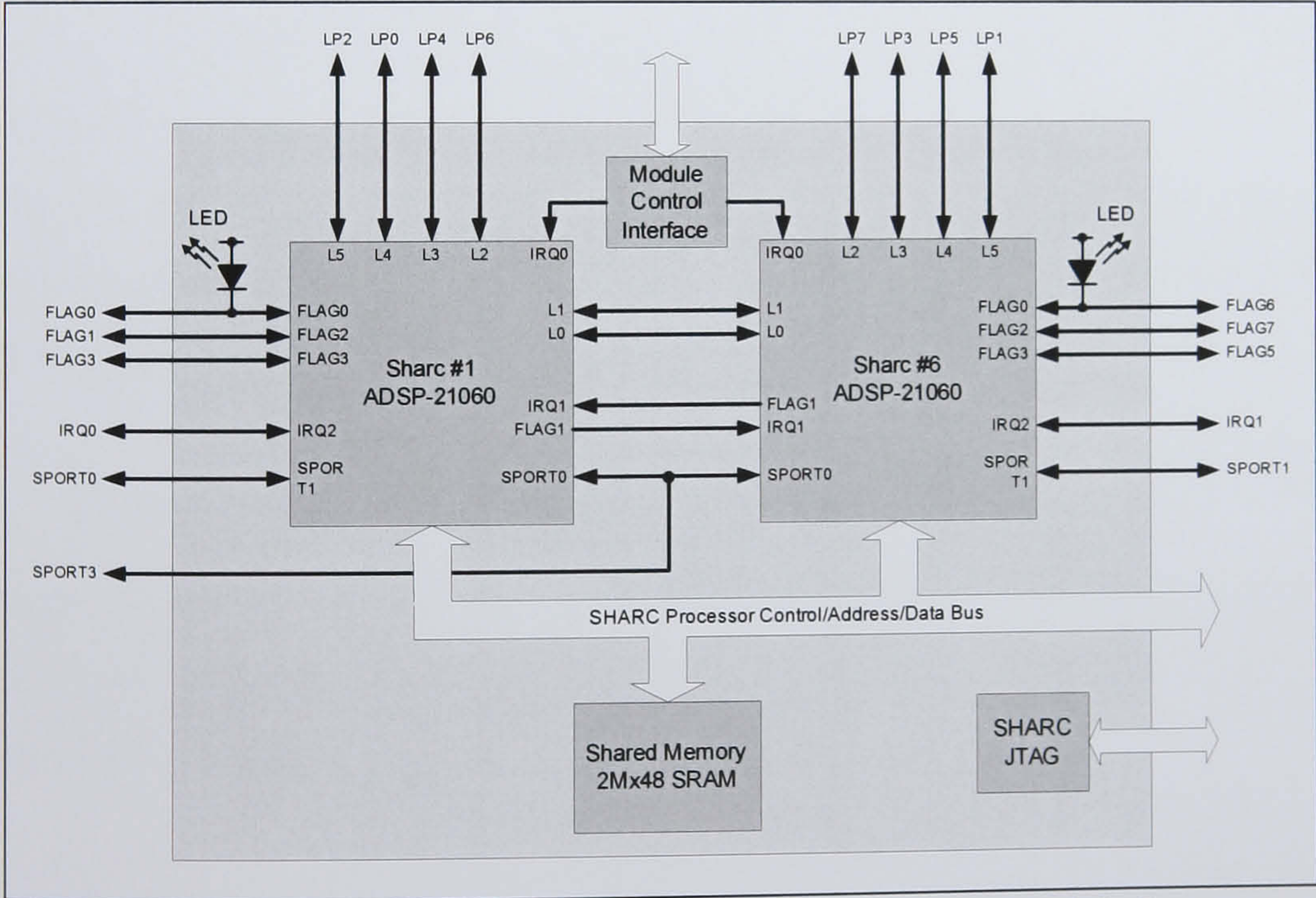


Figure 7-5 Dual SHARC Processing Module Interconnections

SHARCPAC Interface	Destination on Digital Transceiver Board
LP0, LP2, LP5	Processing FPGA
LP3	Connector (for off-board connections)
LP1, LP4, LP6, LP7	Not used.
SPORT0, SPORT3	Processing FPGA
SPORT1	Connector (for off-board connections)
FLAG0,1,3,5,6,7	Processing FPGA and LEDs
IRQ0	Bus Arbitration CPLD, Processing FPGA
IRQ1	Processing FPGA

Table 7-1 Dual SHARC DSP Sub-System Module Interfaces

7.5.2 Module Control Interface

The module control interface (MCI) is defined within the SHARCPAC specification [Bittware, 136] to allow a carrier board to determine the functionality of the module installed and then to control it. The MCI controls the multiprocessor identification (MID) number¹, interrupts, and resets of each SHARC DSP. Interrupts can also be generated and masked using the MCI for debugging purposes. The boot mode of all non-primary SHARC DSPs is controlled by the MCI. Access to an EEPROM containing information on the connections and functionality of the SHARCPAC module is gained through a register in the MCI. The MCI has been implemented as a set of eight registers in a small Altera CPLD on its own (MCI) bus which the digital transceiver is able to access and interact with (via the digital receiver bus arbitration CPLD).

7.6 Digital Transceiver Configuration and Software Download

The digital transceiver configuration hardware architecture is illustrated in Figure 7-6. It provides a number of mechanisms by which the system’s PLDs, DSP processors and memory can be configured.

¹ A multiprocessor identification (MID) is allocated to each SHARC processor within a cluster (from 1 to 6) and is used for inter-processor communications.

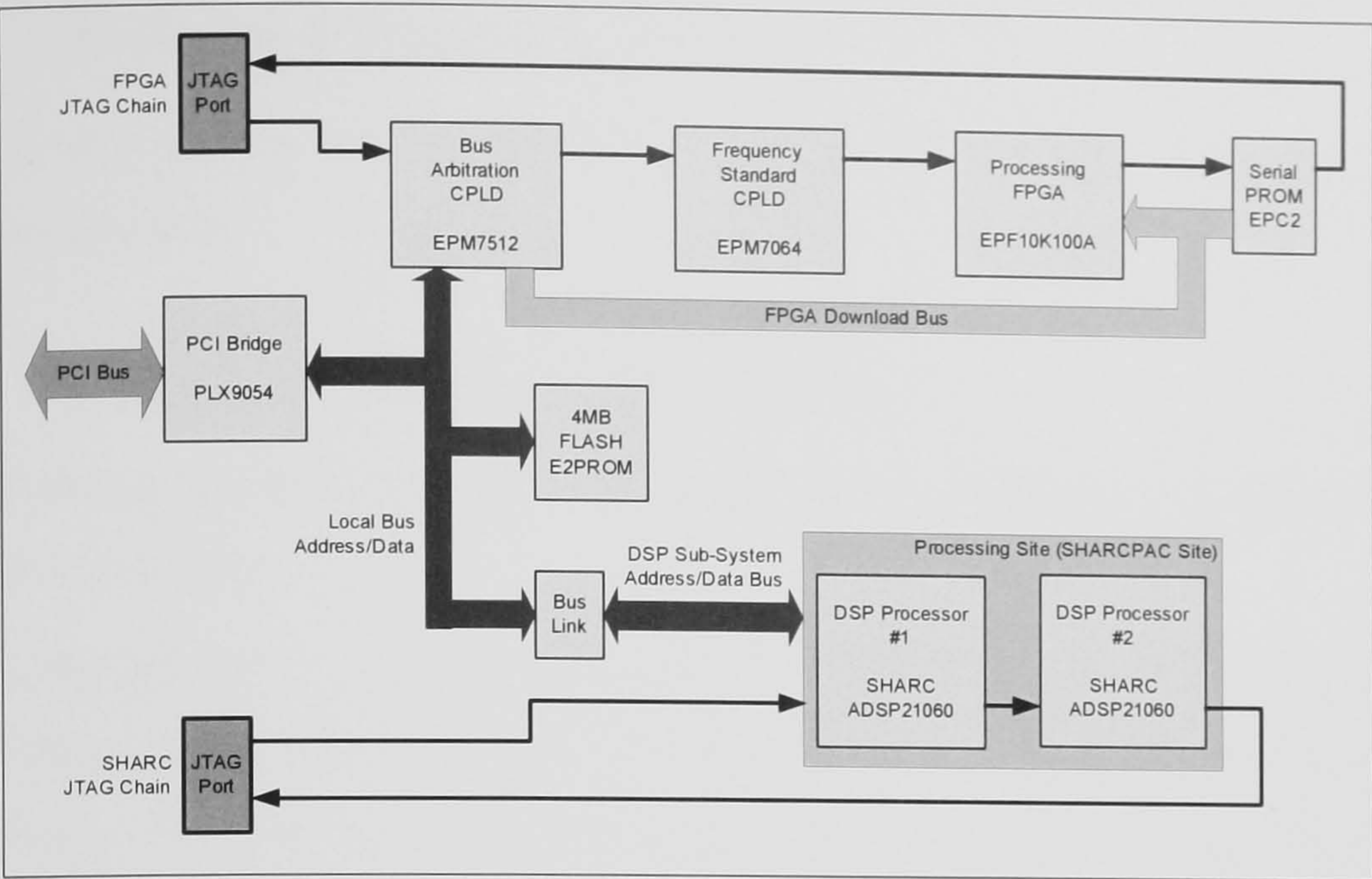


Figure 7-6 Digital Transceiver Configuration Architecture (Simplified)

7.6.1 Configuring Transceiver Programmable Logic Devices

There are three Altera PLDs in the digital transceiver and an EPC2 PROM [Altera, 139] that, if fitted, can configure the processing FPGA from a pre-stored bit stream. These devices are all connected in series on a single JTAG [IEEE, 134] programming chain. This is the primary (and only) means of programming the bus arbitration CPLD, the frequency standard CPLD and the serial PROM. The EPC2 PROM was included in the design as a back-up for the software download interface and to allow the transceiver to be configured for use without a host PC. However, the primary means of programming the processing FPGA is via a memory mapped interface implemented via the bus arbitration CPLD allowing a host initiated software download of the FPGA configuration file.

7.6.2 Software Download (DSP Sub-system)

The primary means of downloading programs and data to the DSP sub-system software is via the host which can directly access the shared memory, and in the case of SHARC processors, the internal processor memory. A secondary means of programming the processors is via a 4 MByte serial electrically erasable PROM (E2PROM) which would allow the digital transceiver to be pre-configured for use outside of a PC. The DSP sub-system also has its own JTAG chain which can be used in the development and testing of software.

7.7 Transceiver Digital Interfaces

This section summarises the external digital interfaces available from the digital transceiver platform.

7.7.1 Link Ports / High Speed Serial Ports

The following SHARC compatible high speed interfaces are brought to connectors on the transceiver board:

- **LP0, LP1, LP2** – These interfaces which are directly connected to the processing FPGA and are nominally intended to be used as additional SHARC processor Link Ports. They may also be re-configured as SHARC compatible serial ports or for user-defined input/output.
- **SHARC LP3** – This provides a link port interface which is directly routed to the SHARCPAC site. If required this link port may either be routed to another board or looped back to LP0-2 to increase the number of high speed data paths between the SHARC processors in the DSP sub-system.
- **SHARC SP1** – This provides a SHARC serial port interface which is directly routed to the SHARCPAC site.

7.7.2 Auxiliary Digital I/O

Three un-committed digital logic lines are routed from the processing FPGA to a connector and their use is user defined. It is one of these signal lines that is used to provide a one-pulse-per-second synchronisation input in the channel sounder application described in a later chapter.

7.7.3 Serial Interfaces

The wideband transceiver includes three onboard serial communications interfaces:

- **Sync/Async RS232** - RS-232 compatible synchronous/asynchronous serial interface using a highly configurable Zilog Integrated Universal Serial Controller [Zilog, 140]. The synchronous serial interface is included to allow the wideband transceiver to be developed as a modem test bed. It can be configured as data

communications equipment (DCE) allowing standard synchronous serial data terminal equipment (DTE) to be connected to it directly.

- **Async RS-232** - RS-232 compatible asynchronous serial interface utilising a National Semiconductors Universal Asynchronous Receiver/Transmitter (UART) type PC16550 [National, 141].
- **RS-485** - RS-485 compatible bi-directional differential signalling interface which can be configured (via a header and links) to either utilise the PC16550 UART or to interface to the FLEX FPGA for custom UART designs. The differential asynchronous serial interface is included to allow the wideband transceiver to directly control other equipments such as power amplifiers and antennas. Such an application has been developed to allow the digital transceiver to control a Harris Inc. HF power amplifier and antenna tuning unit (ATU). This work has been described by Chau [Chau, 142].

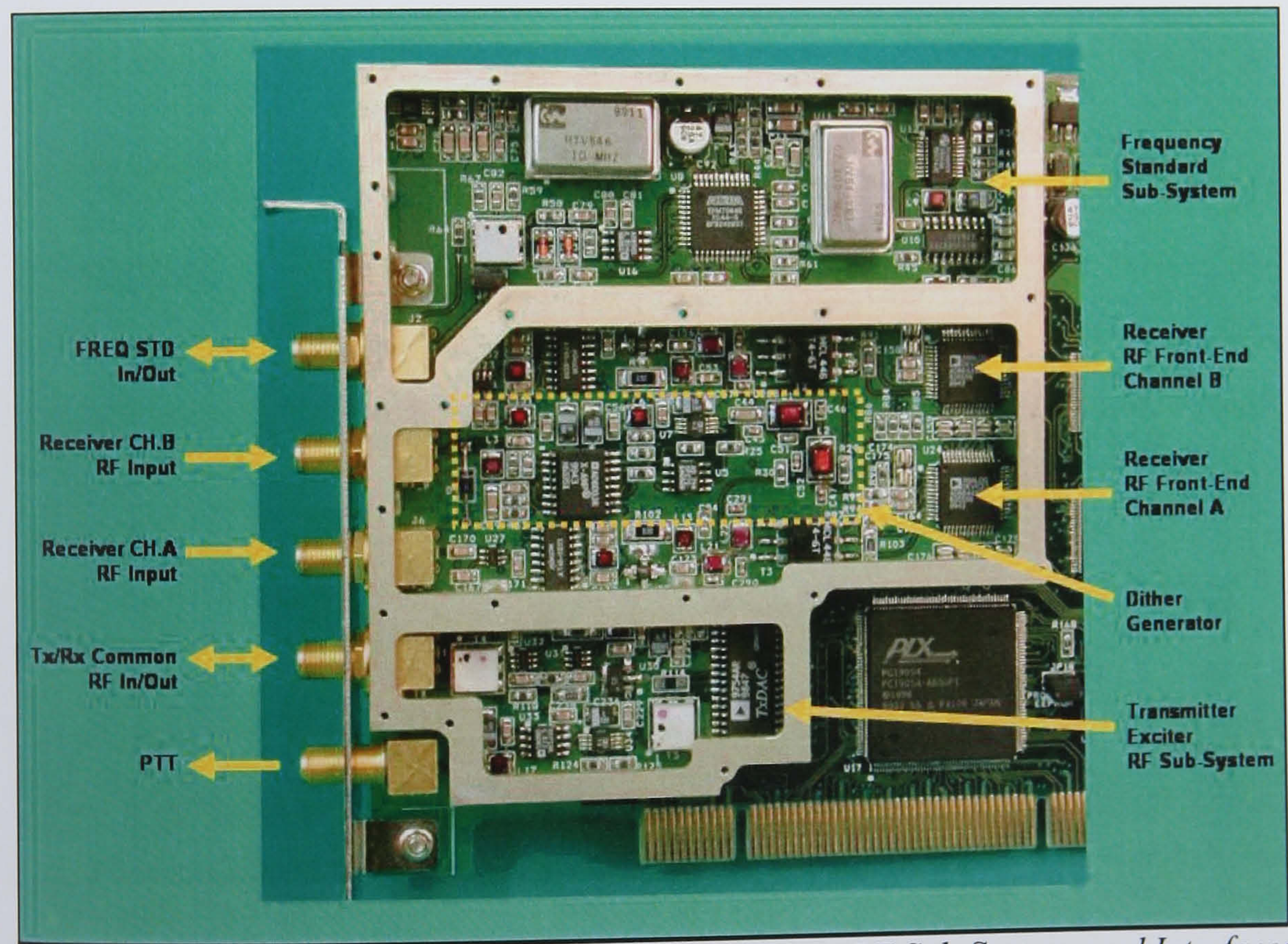


Figure 7-7 Photograph of Digital Transceiver RF Sub-Systems and Interfaces

7.8 Frequency Standard Sub-System

7.8.1 General Description

The frequency standard sub-system generates the low phase noise (low jitter) sampling clocks required by the digital transmitter and diversity digital receivers. It also sources a 10 MHz TTL clock which is used to generate the clocks used throughout the transceiver’s digital processing sections. A sampling clock frequency of 62.208 MHz is chosen because it is close to the maximum rate supported by the ADCs, DDC and DUC and it is a common integer multiple of the most popular modem symbol rates (e.g. 75, 2400, 16k, 28k8) and the 10 MHz reference. A block diagram of the frequency standard sub-system is given at Figure 7-8.

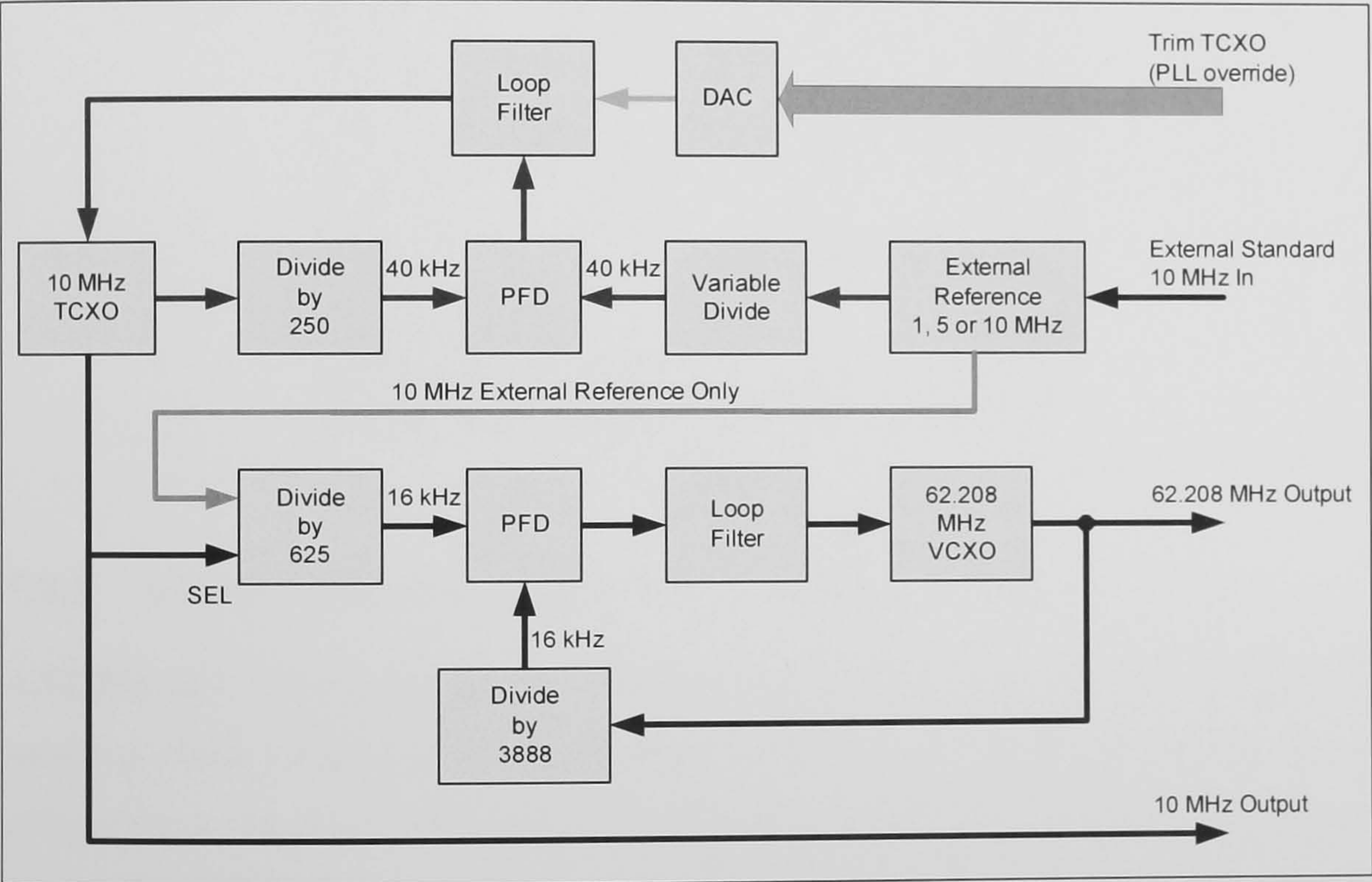


Figure 7-8 Block Diagram of Digital Transceiver Frequency Standard Sub-System

The sampling clocks are generated by a high quality 62.208 MHz voltage controlled crystal oscillator (VCXO). The sampling clocks generated are designed to have a phase noise of better than -70 dBc/Hz at 10 Hz offset, -120 dBc/Hz at 100 Hz and -155 dBc/Hz at ≥ 1 kHz commensurate with the required receiver performance. The VCXO is phase locked to a more accurate frequency reference which is normally the on-board 10 MHz temperature compensated crystal oscillator (TCXO) which has a frequency accuracy of better than ± 4.6 parts-per-million (PPM). The TCXO, which is

the transceiver frequency reference, can be phase locked to an external 1, 5 or 10 MHz frequency standard (nominally a 0 dBm 50 Ω sinusoidal source). Alternatively the TCXO frequency may be trimmed using an on-board, software controlled, DAC to an accuracy of better than 0.02 PPM. The transceiver has a single frequency standard input/output port which can be software configured to output the TCXO 10 MHz reference frequency. Figure 7-9 shows the graphical user interface (GUI) for user control of the frequency standard. In addition to controlling the system the GUI also displays the lock status of the VCXO and TCXO phase locked loops (PLLs) and whether an external reference is present.

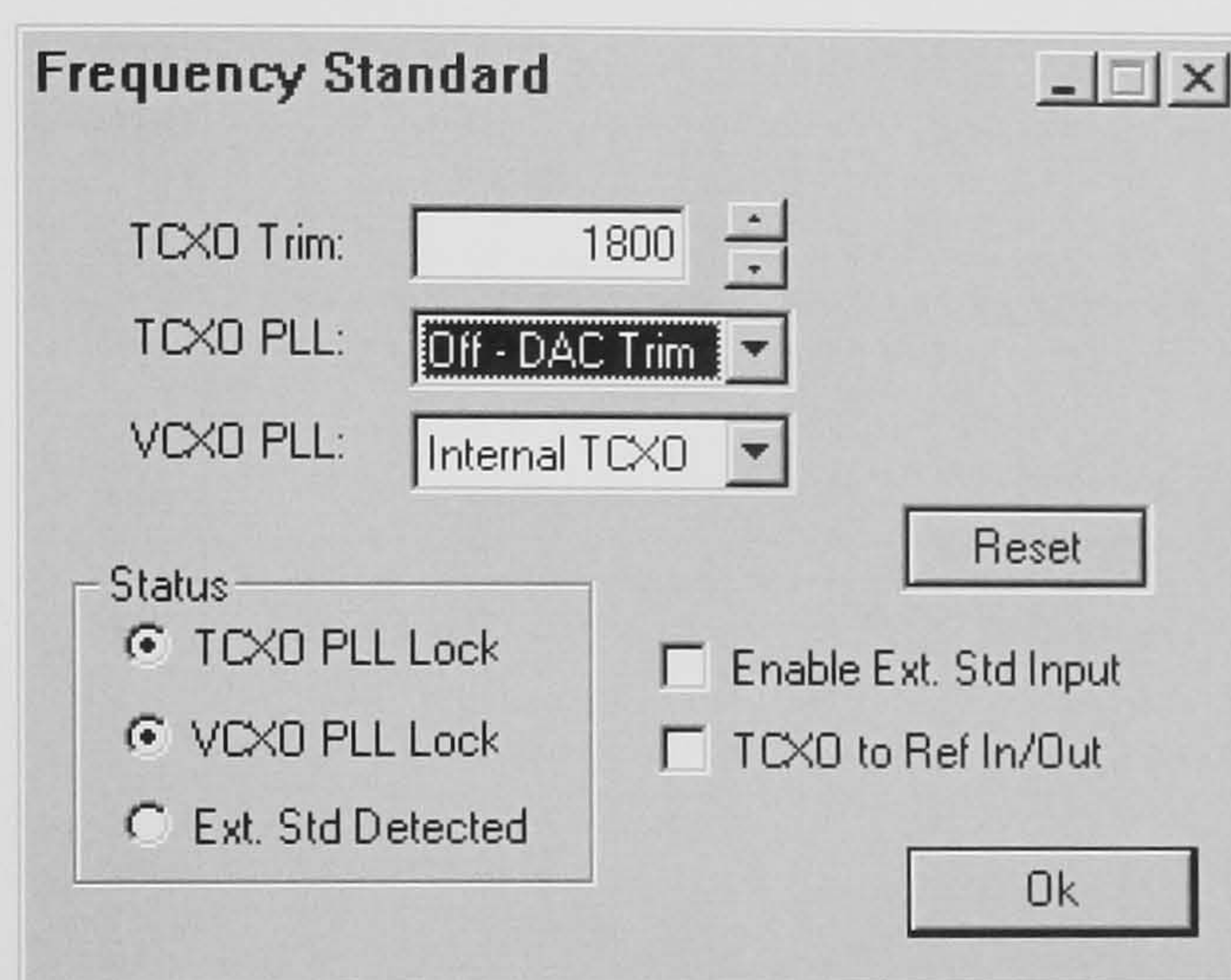


Figure 7-9 Frequency Standard User Interface

7.8.2 62.208 MHz Low Phase Noise Sampling Clock

A 62.208 MHz VCXO is used as a voltage controlled oscillator (VCO) to supply the sampling clock because of its good inherent phase noise performance. The VCXO utilised has a frequency pull range of ± 110 PPM controlled by applying 0-4 V to its frequency adjustment pin. With a constant 2 V control input it has a frequency tolerance of about ± 20 PPM. The VCXO is designed as part of a PLL that can be locked to the TCXO. The VCXO PLL uses a PFD reference frequency of 16 kHz which is the highest integer reference frequency common to 10 MHz and 62.208 MHz. The loop filter for the VCXO PLL, which is a classical third order design ([Rohde, 143]; [Keese, 144]) was chosen with a natural frequency, ω_n , of 25 Hz. This provides > -120 dBc of attenuation from the loop filter at 16 kHz. Being that this is a single frequency synthesiser, lock time is not a critical parameter of the design and fast-locking is sacrificed to provide more attenuation to the low reference frequencies. Lock

is always achieved within ~ 0.5 s. The VCXO output feeds an ECL comparator which provides a very low jitter differential 50Ω impedance feed to the two receiver ADCs. The output is also fed to a special clock buffer which provides the clock to the transmitter DAC and to any digital circuits that may need it. Each destination is driven by a single buffer output and source terminated to minimise signal reflections.

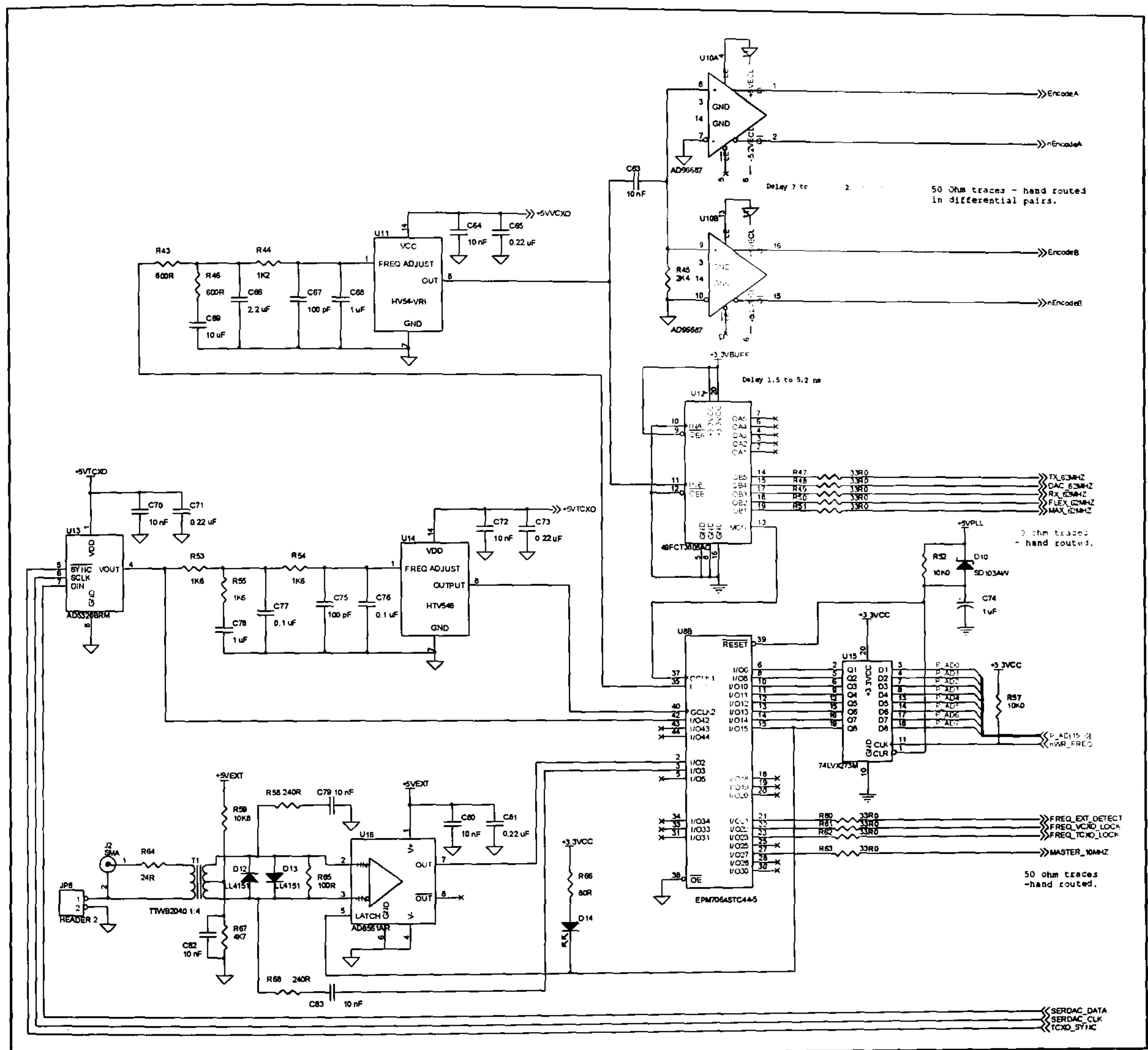


Figure 7-10 Excerpt of Frequency Standard Sub-System Schematic

7.8.3 10 MHz TCXO Frequency Standard

A low-phase noise 10 MHz TCXO is used as the transceiver's internal frequency reference. The TCXO has a pull range of ± 10 PPM using a voltage of 0.5-4.5 volts applied to its frequency adjustment pin. With a constant 2.5 V applied its stability is ± 4.6 PPM (± 46 Hz). The TCXO is configured to be used in a second PLL when a more accurate external frequency reference is available. The TCXO PLL uses a PFD reference frequency of 40 kHz (though this could readily be changed by re-

programming the PLD). The loop filter has $\omega_n=100$ Hz and, as for the VCXO PLL, a classical third order passive filter design is utilised.

A digital-analogue converter (DAC) is incorporated into the design to control the TCXO frequency when the TCXO is not being locked to an external standard. The DAC and PLD charge pump output can be independently set to a high impedance (Z) state. This allows both outputs to be wired together (wired-or) before the loop filter. Programming the DAC output voltage allows the TCXO frequency to be trimmed. The DAC has a resolution of 12-bits with a voltage range of 5 V. This translates to a TCXO frequency setting accuracy of ± 0.061 Hz.

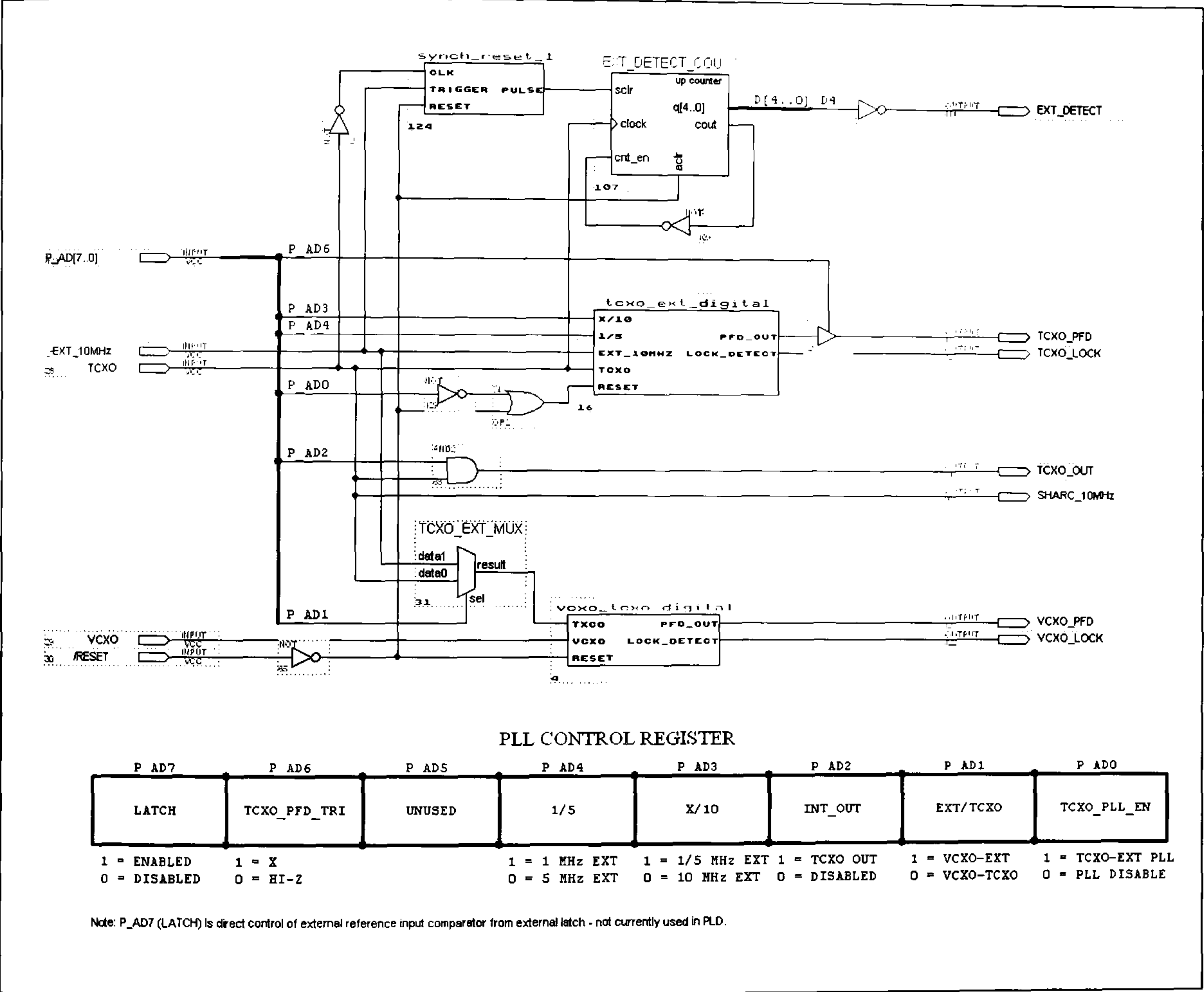


Figure 7-11 CPLD Design for Frequency Standard Showing Control Register

7.8.4 CPLD Dual Synthesiser Implementation

Rather than using a special device or building a synthesiser from discrete components an elegant solution has been formulated using a CPLD. The synthesiser for both the VCXO and TCXO PLLs are implemented in a single small-footprint Altera EPM7064 CPLD which contains the necessary frequency dividers, PFDs and some control logic

(Figure 7-11). The PLL phase-frequency detector (PFD) is based on a standard logic design [Best, 145]. However, this is modified so that the conventional digital PFD controls two tri-state buffers in order to implement a charge pump giving outputs of zero volts, five volts or high impedance (Z). The CPLD PFD design is shown in Figure 7-12.

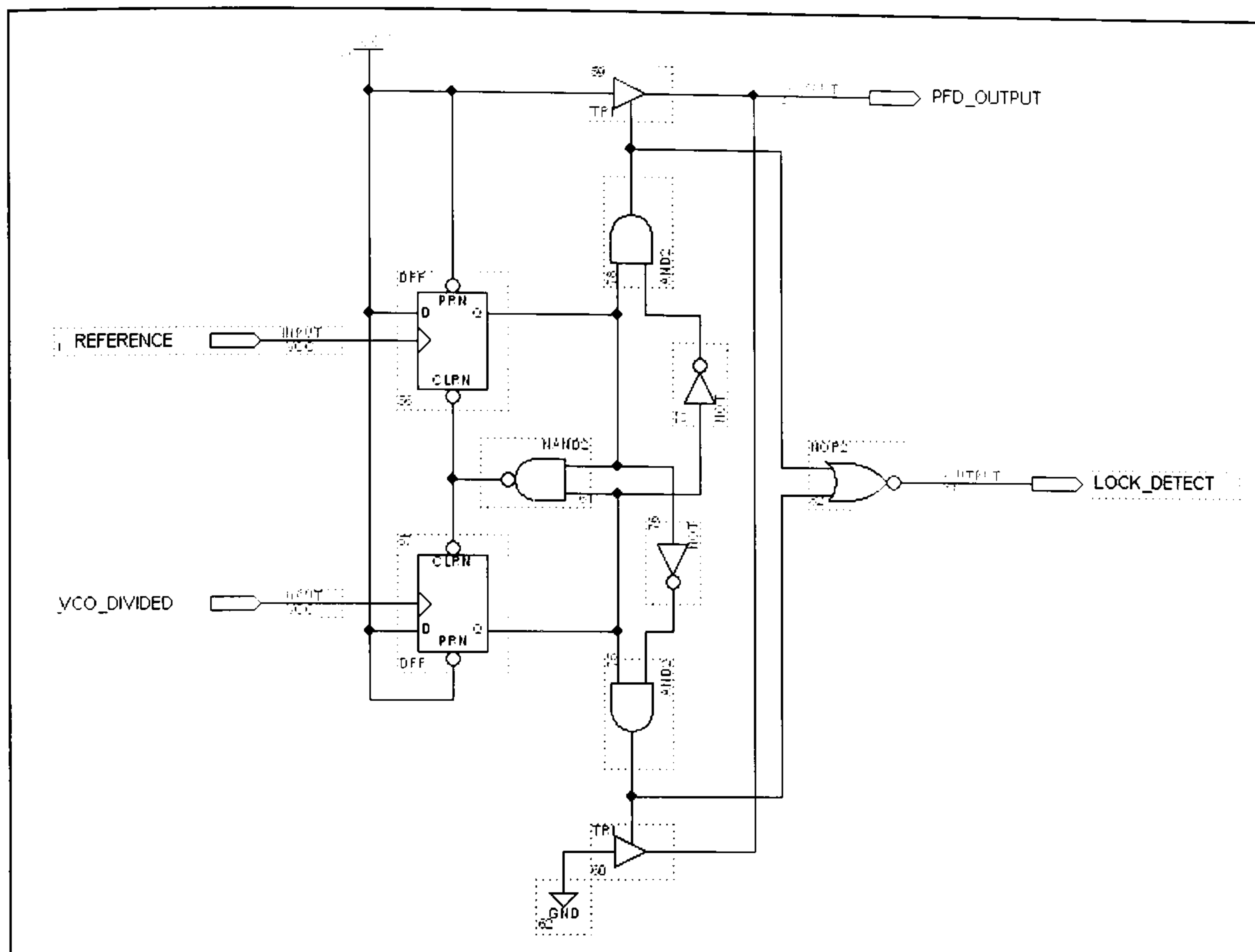


Figure 7-12 CPLD Implementation of Phase-Frequency Detector (PFD)

The state machine of Figure 7-13 shows the operation of the PFD [Best, 145]. All transitions occur on the rising edge of the clock specified for the transition. In lock both signals should clock at the same time. Thus the state machine will stay in state Z. The state cannot change directly between *Zero* and *One*. This improves lock time by only allowing the PFD to output voltage corrections that drive the VCXO towards the desired frequency. The output is always related to the frequency error between the two signals, which leads to the term frequency detector. The PLL will reach the locked state when both flip-flops clock at the same time (zero phase error). The outputs of the flip-flops will then be zero. This is used to generate a lock detect signal using a NOR gate.

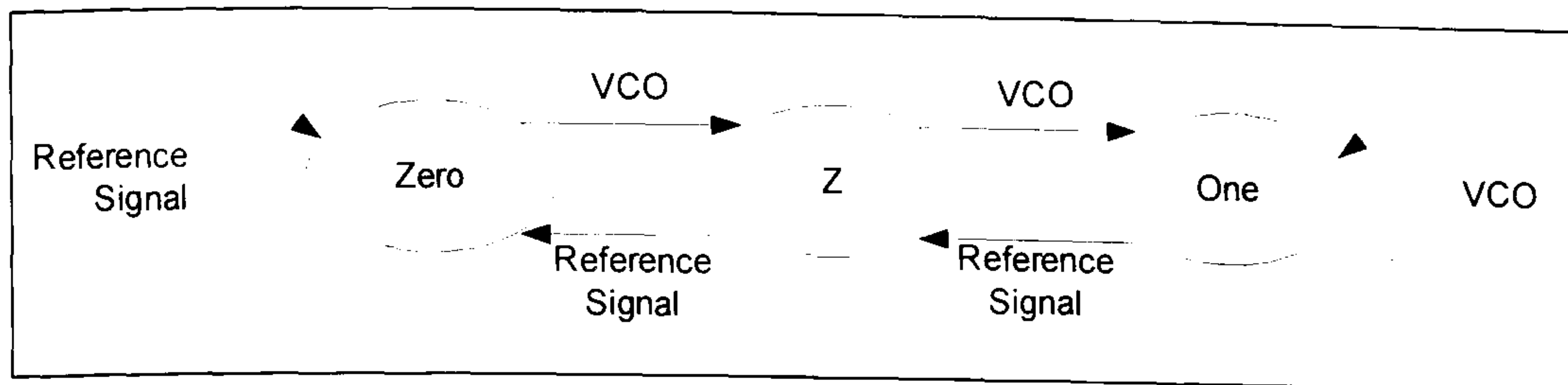


Figure 7-13 Phase-Frequency Detector (PFD) State Machine

7.8.5 External Reference Input/Output Interface

The frequency standard sub-system accepts a 1, 5, or 10 MHz 0 dBm nominal 50Ω input. The external reference signal input circuitry (shown in the lower left hand part of Figure 7-10) steps-up the input signal level using a 1:4 transformer and feeds the signal to an ultra-fast differential comparator which converts the low-level signal to TTL levels. This creates the square wave clock required by the CPLD.

If desired the 10 MHz TCXO clock can be provided as an output under software control (when no external reference is connected). This allows other systems to be phase locked to the digital transceiver TCXO. The clock is output from the frequency standard CPLD through a resistor to one side of the transformer secondary. The transformer steps the voltage down from the 5 V CPLD output to 1.25 V. The resistor value is chosen to provide a 0 dBm output to the SMA connector. When the TCXO is not being output the clock line is grounded within the PLD. An equal value grounded resistor is connected to the other arm of the transformer secondary to balance this resistance and thus not effect the differential comparator's input. The comparator has a latch enable input. The latch enable allows the comparator to be disabled and the current output held. This is beneficial when the internal 10 MHz clock is being output to minimise noise within the CPLD (the comparator would otherwise create a 10 MHz clock signal that is out-of-phase with the internal 10 MHz clock).

7.8.6 Memory-mapped Control Interface

The different operating modes available in the frequency standard sub-system are selected using an 8-bit memory mapped interface (register bit assignment shown in Figure 7-11). The options available include the ability to select a 1, 5 or 10 MHz external reference for the TCXO, to select whether the VCXO is phase locked to the TCXO or an external reference and to enable the 10 MHz reference output.

7.8.7 Construction Techniques to Minimise Noise and Interference

Experimentation with prototype circuits demonstrated that the relatively simple design described can give very good performance as long as the use of multiple, isolated power supplies, good construction and grounding techniques are rigidly adhered to. It was found that the CPLD that incorporates the PFD, which is essentially an analogue modulating current source, cannot be used for any other logic functions without compromising its performance. In order to minimise noise and interference on the clocks generated by the frequency reference sub-system the major circuit functions were provided with separate power supplies (via miniature surface-mounted linear regulators). The need for this was verified during the initial design and prototyping stages. In addition power supply decoupling capacitors were provided for all active devices. All the noise sensitive devices in the sub-system are mounted on the top of the PCB within an RF shield. The PCB internal ground planes provide shielding beneath the components. All control lines from the transceiver digital section are buffered to minimise interference. Power supply regulators and digital interface devices (buffers) are mounted on the rear of the PCB.

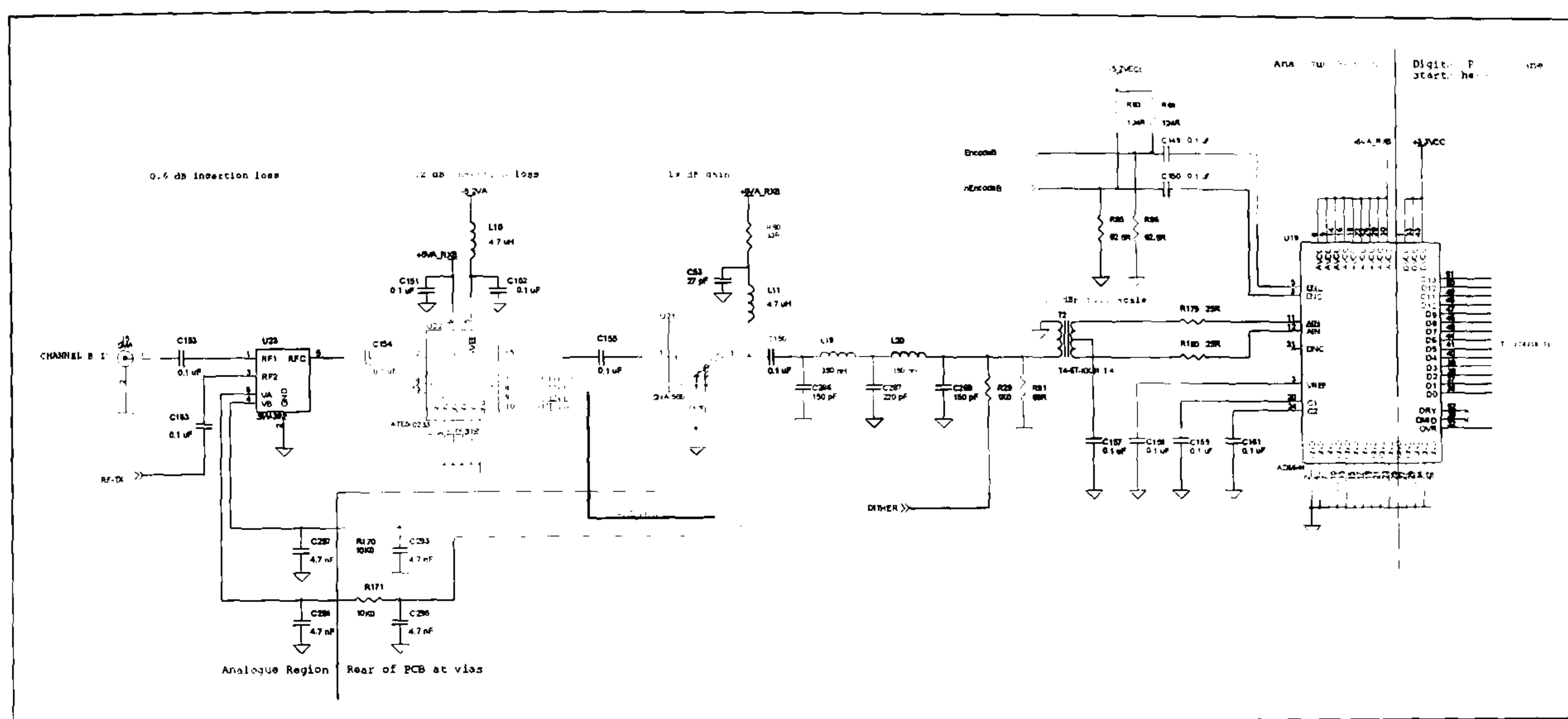
7.9 Digital Receiver Sub-System

The receiver sub-system supports the simultaneous capture and digitisation of signals from two sources using a dual (diversity) RF front end. Four digital receiver channels may be independently allocated to either input to allow the reception of signals of interest.

7.9.1 Diversity Digital Receiver RF Front-End

The digital transceiver board includes two receiver RF front ends each with its own digitiser. This has been done in order to allow diversity reception using multiple antennas if desired¹. The physical receive channels have the nomenclature ‘Channel A’ and ‘Channel B’. Figure 7-14 is an excerpt from the digital transceiver schematic drawings showing the implementation of one receive channel (the other is essentially identical). A digitally controlled RF switch allows the input to be sourced from either the channel’s RF input connector, the common RF input/output or the attenuated output of

the transmitter. The input then passes through a programmable 0-30 dB attenuator and on to the RF amplifier which is a GaAs MMIC gain block (with matched 50Ω input and output). This provides ~20 dB of gain to the signal. Following the amplifier is a harmonic filter with a 30 MHz cut-off which reduces the impact of both harmonics generated by the amplifier and also defines the noise bandwidth at the ADC input. The filter output is terminated with 50Ω formed from a 68Ω resistor in parallel with the 1:4 transformer which steps up the signal voltage and converts it to the differential signal which is applied to the AD6644 14-bit ADC sampling at 62.208 MSPS. The dither signal is added to the received signal at the input to the transformer. To maximise performance the ADC uses a terminated differential ECL clock feed sourced from the frequency standard sub-system.



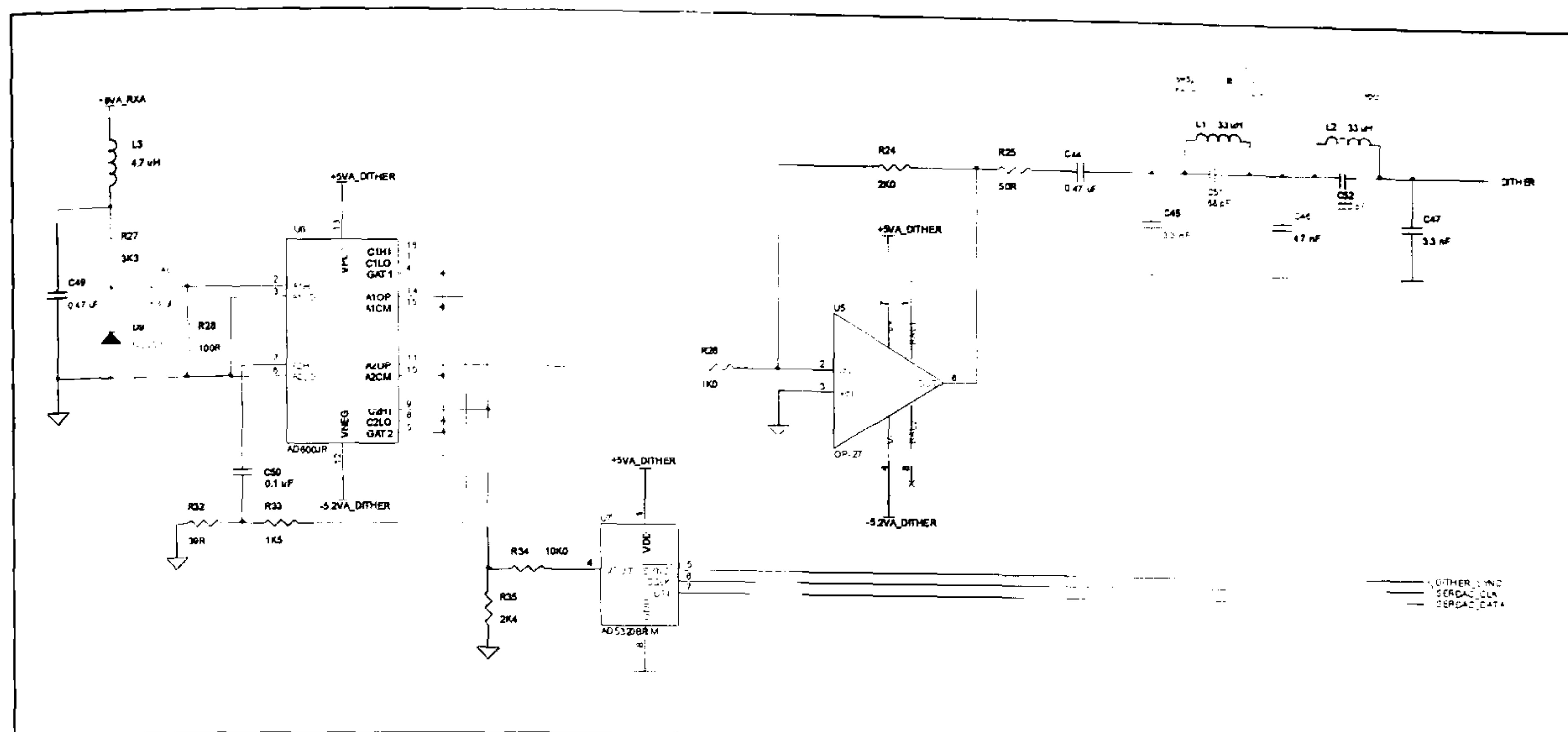


Figure 7-15 Dither Generator (Schematic Excerpt)

7.9.3 4-Channel Digital Receiver

A digital receiver ASIC [Graychip, 124] is used in the digital receiver (illustrated in Figure 7-16). It contains four DDC channels that may be used independently. A cross point switch allows either of the two digitised RF receive channels to be directed to any DDC. The digital input to a DDC is mixed down to complex baseband and then decimated and filtered using a five stage cascaded integrator-comb (CIC) filter followed by fixed and programmable decimating FIR filters. Each DDC may be programmed (via a memory mapped interface) to set the required receiver frequency and channel bandwidth. The gain through each stage of the DDC is programmable so that despite the restricted output word length (16-bits) ~115 dB of useful dynamic range can be realised.

The DDC baseband output is finally formatted as required (real or complex baseband) and output to four synchronised serial ports or a single high speed Link Port [Analog, 135]. When link port output is used and multiple channels are in use the data from the active channels are multiplexed together. To maximise flexibility both the baseband outputs and the DDC ASIC control port are interfaced via the processing FPGA on the digital transceiver. This allows the received baseband signal to be processed or routed as required. Most usually the FPGA is programmed to simply forward the received samples to one of the Link Ports on the SHARC DSP processing module. The DDC is normally controlled via software (via a memory mapped interface decoded in the processing FPGA address space). However, the ability to control it directly from the

implement a multi-band receiver.

FPGA allows applications including features such as synchronised frequency hopping and frequency sweeping to be readily implemented.

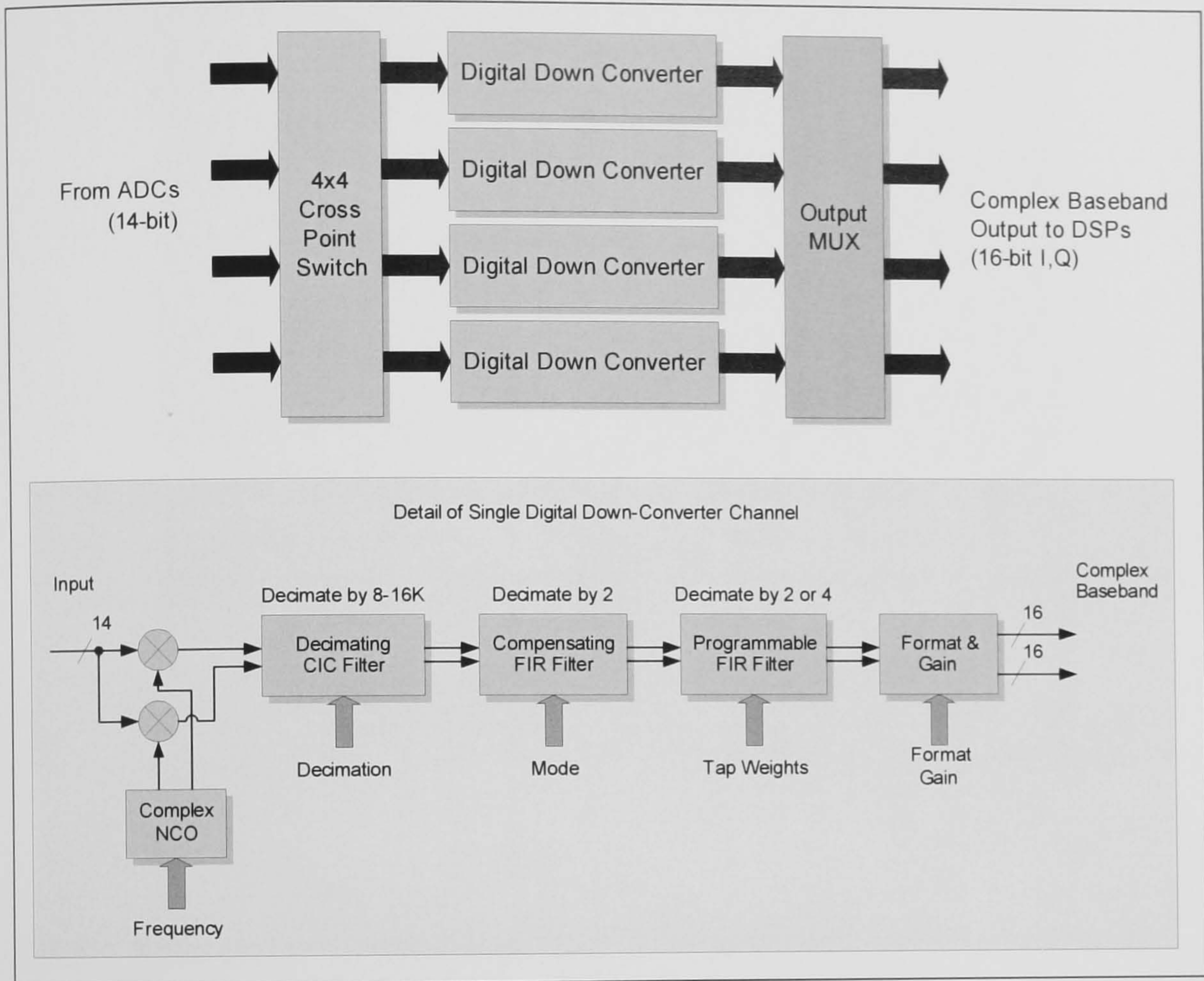


Figure 7-16 Block Diagram of 4-Channel Digital Receiver ASIC [Graychip, 124]

7.9.4 Software Control of Receiver

The receiver GUI is reproduced in Figure 7-17 demonstrating the comprehensive software control available.

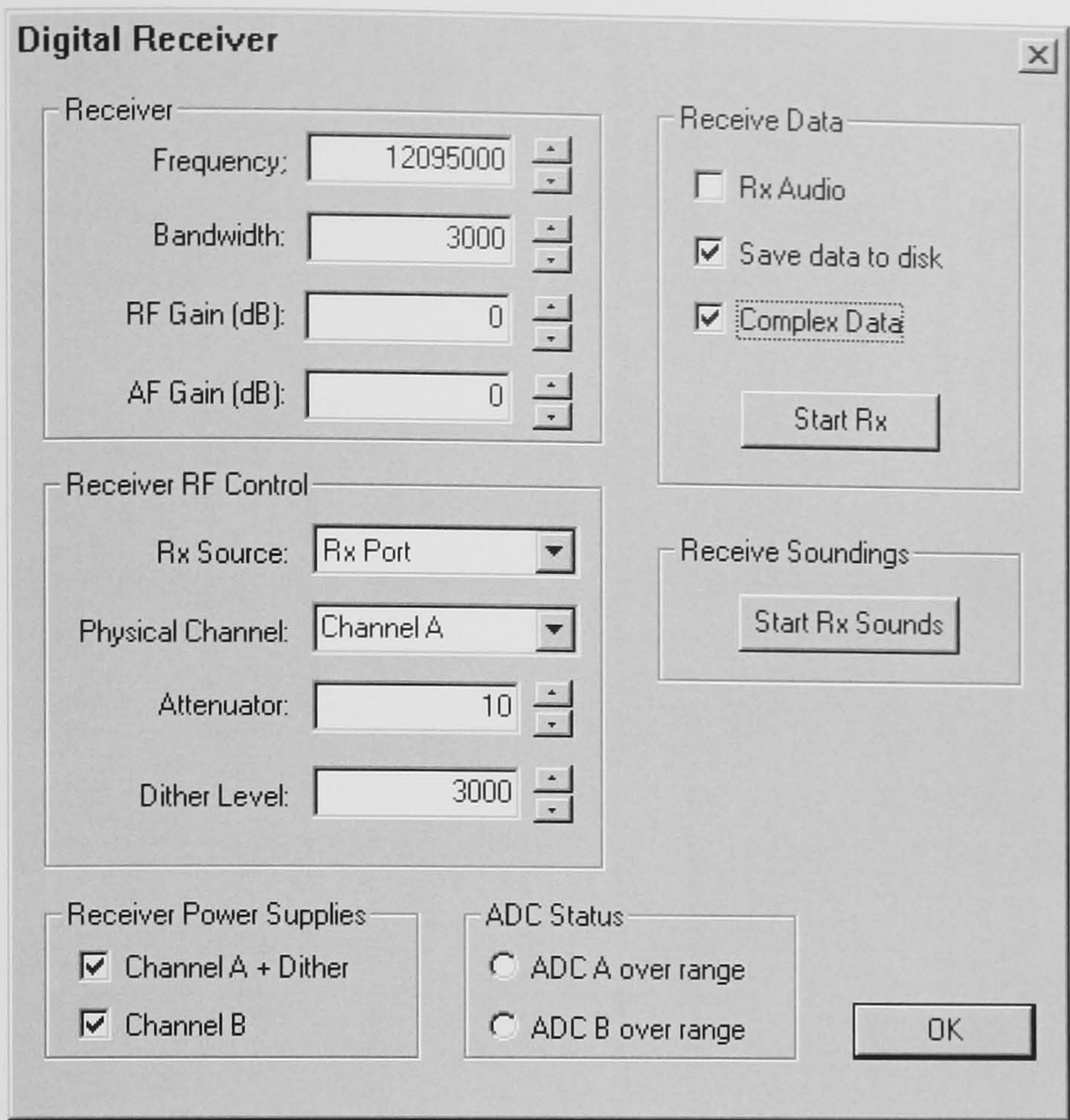


Figure 7-17 Digital Receiver Graphical User Interface

7.9.5 Summary of Digital Receiver Characteristics

The principal characteristics of the wideband, multi-channel digital receiver implemented in the digital transceiver are summarised in Table 7-2.

Receiver Specification	Design Performance
Number of channels:	Diversity (2) RF input channels 4 digital receiver channels
Direct Sampling Frequency range:	2 to 31 MHz (2 to 28 MHz w. practical anti-aliasing filter)
Under-sampling input range:	To ~250 MHz (w. harmonic filter bypassed)
Channel Bandwidth:	900 Hz to 1.9 MHz
Sensitivity (10 dB SINAD):	-113 dBm (3kHz bandwidth)
ADC SFDR (using dither):	> 110 dB
Instantaneous dynamic range (IDR):	> 115 dB
3 rd Order Intercept Point (IP3 _{IN}):	+19 dBm
2 nd Order Intercept Point (IP2 _{IN}):	+27 dBm

Table 7-2 Summary of Wideband Digital Sub-system Characteristics

7.10 Transmitter Exciter Sub-System

The transmitter exciter sub-system supports the digital generation of four independent transmit channels that are summed together before being digital-to-analogue converted, amplified and output.

7.10.1 4-Channel Digital Transmitter Sub-system

The transmitter supports up to four independent channels. A GC4114 four channel DUC ASIC [Graychip, 146] takes transmit samples from the DSP sub-system at complex baseband, filters and up-converts the signals to the required frequency (Figure 7-18). Each DUC consists of a programmable interpolating (factor 2 or 4) FIR filter, a compensating FIR (CFIR) filter and a programmable CIC interpolating filter. The CFIR compensates for droop in the following CIC stage. The interpolated signal is then at the required output sampling rate (62.208 MSPS). A complex mixer translates this signal to the required transmit frequency. The gain for each DUC channel is programmable. The up-conversion process described is undertaken for all four channels independently and the outputs are finally summed together.

Separate high speed serial interface are used to supply each DUC channel with baseband samples. These are normally sourced from the DSP processing sub-system. They are physically connected via the digital transceiver processing FPGA to allow alternative routing and, if required, processing to be undertaken within the FPGA. This design choice was fortuitous since during testing a design fault was discovered in the DUC ASIC (confirmed in correspondence with the manufacturer). This required additional digital circuitry to control the length and timing of a synchronisation pulse which was readily implemented in the FPGA. An alternative implementation would have likely required the production of a modified PCB. The memory-mapped control interface is also routed via the FPGA. As was the case for the digital receiver this allows high speed, tightly coupled control of the FPGA allowing the implementation of features such as frequency agility (frequency hopping and sweeping).

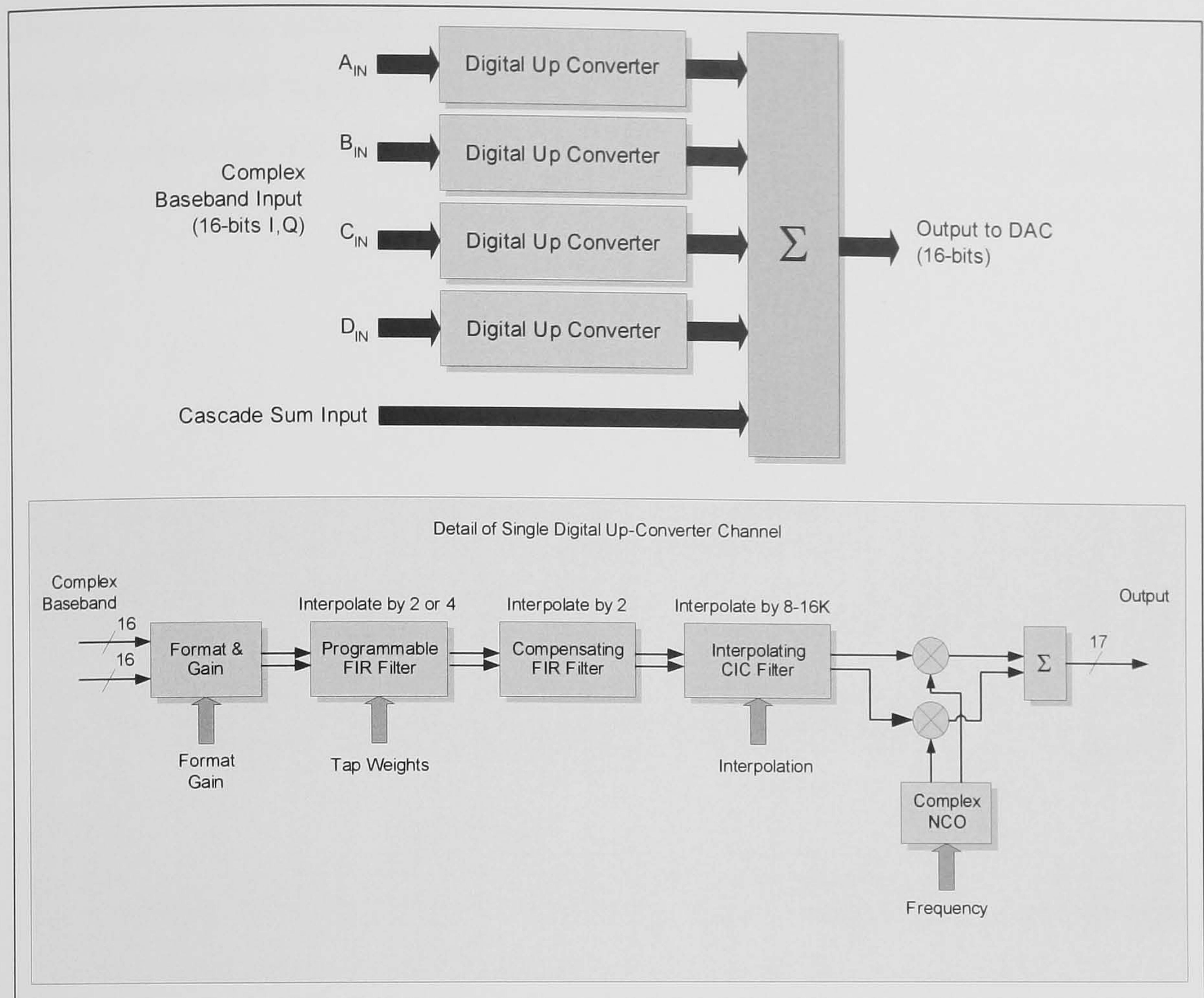


Figure 7-18 Block Diagram of 4-Channel Digital Transmitter ASIC [Graychip, 146]

7.10.2 Transmitter Exciter RF Output Stage

The DUC ASIC digital output is fed to a high performance AD9754 RF DAC [Analog, 147]. The RF DAC, which uses the same low phase noise 62.208 MHz sampling clock signal as the receiver digitisers, converts the signal to the analogue domain. The DAC full scale output power may be adjusted by applying a control voltage to a designated pin. A digitally controlled voltage reference (implemented using a control DAC and a voltage reference) has been implemented to allow the available RF DAC output power and therefore its dynamic range to be maximised for any given output level. A control pin also allows the DAC to be placed in a sleep mode (under software control).

The RF DAC output is converted from a differential signal into a single ended one, amplified using 50Ω gain block, and finally connected to the RF output port via an isolation transformer and RF routing switches (illustrated in Figure 7-19). The first RF switch (U31) allows the transmitter output to be routed to the common transmit/receiver RF port or to a low power dummy load (an attenuator). A second RF switch (U32)

allows one of the diversity receivers to select either the common RF port or the attenuated transmit signal as an input. This latter configuration allows 'loop-back' testing in which the transmitter output may be received by one of the digital receivers.

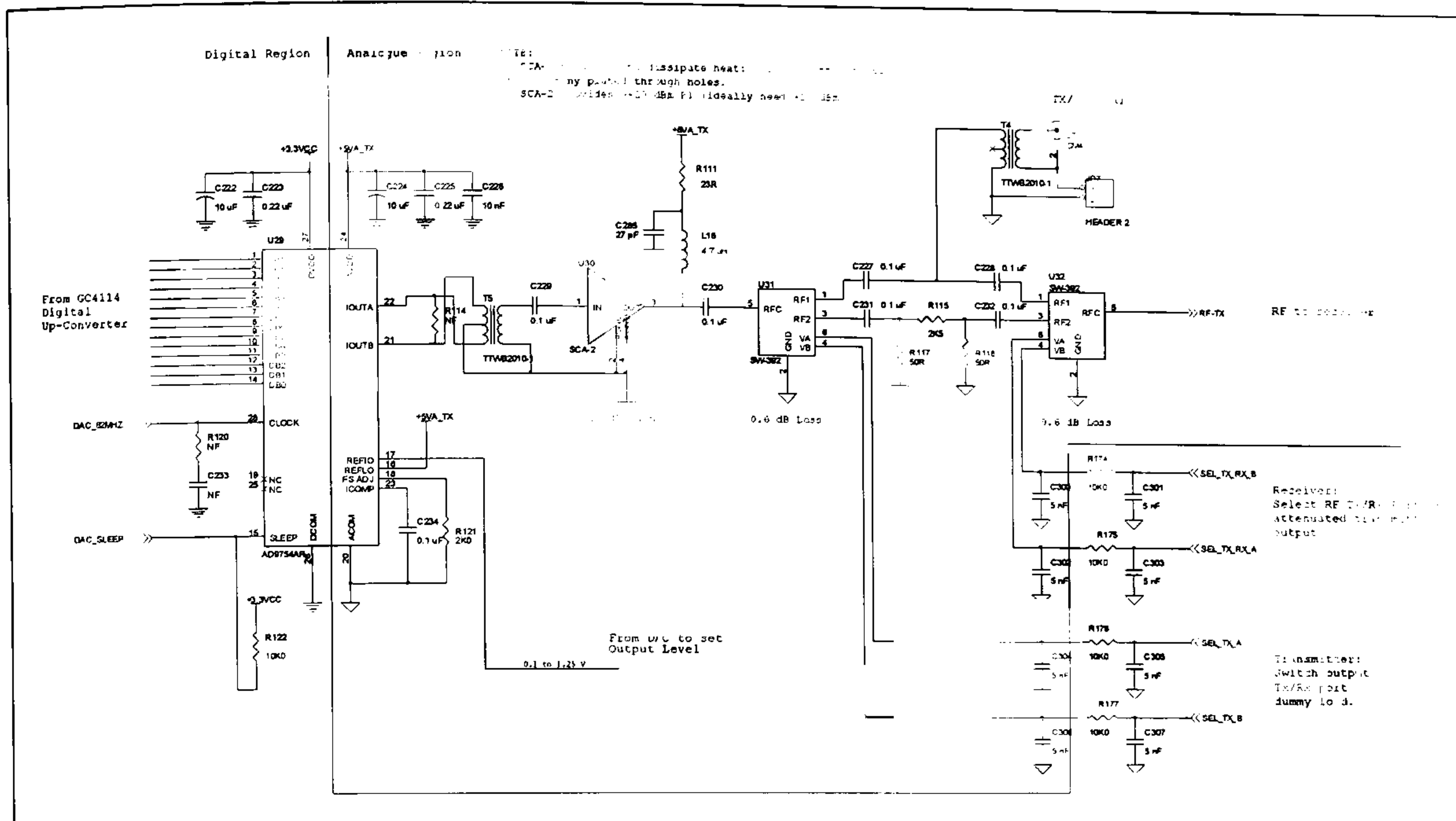


Figure 7-19 Digital Transmitter DAC and RF Chain (Excerpt from Schematic)

7.10.3 Push-to-Talk (PTT) Output

The digital transceiver provides a ‘volts free’ contact closure at a separate output port. The PTT output is formed by the contact closure of a reed relay which is controlled by the processing FPGA. This is primarily intended as a PTT output to signal to an external power amplifier or other device that transmissions are in progress.

7.10.4 Software Control of Transmitter

The transmitter GUI is reproduced in Figure 7-20 demonstrating the comprehensive software control available.

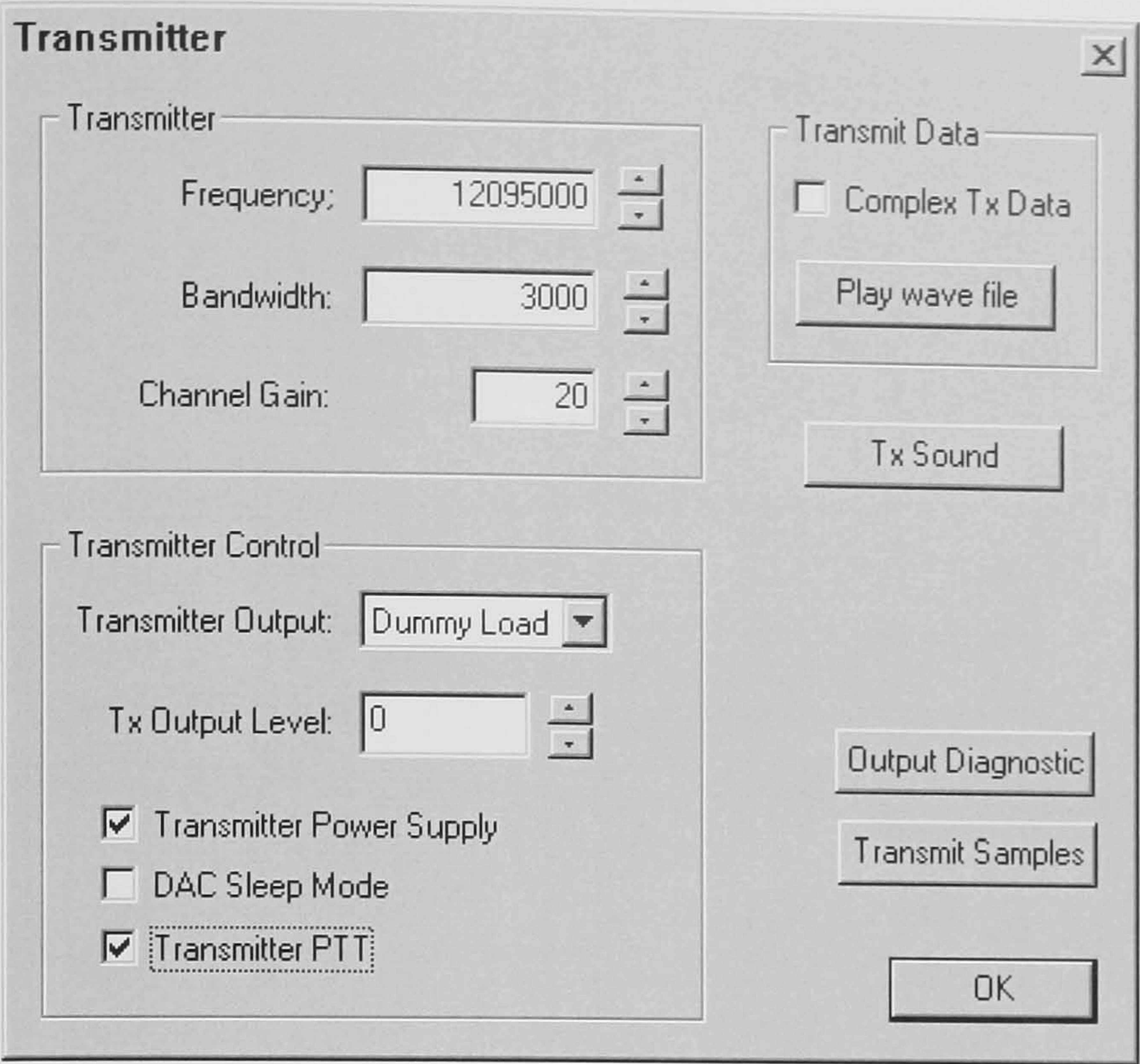


Figure 7-20 Digital Transmitter Graphical User Interface

7.10.5 Summary of Digital Transmitter Exciter Characteristics

The principal characteristics of the wideband, multi-channel digital transmitter exciter implemented on the digital transceiver are summarised in Table 7-3.

Specification	Design Performance
Number of channels:	4 digital transmit channels
	Single RF output
Direct Frequency range:	2 to 28 MHz
Channel Bandwidth:	900 Hz to 1.9 MHz
SFDR:	<-75 dBc (typical)
Wideband noise:	-160 dBc
Instantaneous Dynamic range:	115 dB
Harmonics:	<-40 dBc
IMD:	<-65 dBc
Output Power:	+12 dBm (P1dB = +21 dBm)

Table 7-3 Wideband Digital Transmitter Performance Summary

7.11 Power Supplies for Analogue Sub-Systems

In order to obtain the high performance required for the analogue sub-systems (i.e. the receiver, transmitter and frequency standard) well regulated power supplies which are noise and interference free are required. The principal source of power for the digital logic on the transceiver board is all obtained from the PCI interface and this interface provides +3.3 V, +5 V, +12 V and -12 V. However, given the need to filter and regulate the incoming power (to isolate it from noise etc due to the transceiver and host PC digital logic circuitry) the analogue power supplies are obtained from +12 V. The PCI connector is not specified to provide the required current (of the order of 1.5 A) to meet this requirement. Therefore an additional +12 V power connector, compatible with standard PC peripherals such as disk drives, has been included. Linear voltage regulators are used to produce the necessary clean analogue supplies. In order to achieve a practical design which was able to supply sufficient power and achieve acceptable thermal (i.e. heat dissipation) properties it was necessary to develop a special topology employing regulators in series. The incoming +12 V supplies four primary regulators which each produce +9 V outputs to power the frequency standard, the diversity receiver front-end and the transmitter sub-systems. The transmitter and receiver primary regulators are digitally controlled so that they may be switched-on independently. The +9 V power for each sub-system is then distributed and regulated again using miniature surface mount linear regulators to the required voltage where it is needed. Where a supply is used without further regulation, and it is warranted, low pass inductor-capacitor filtering techniques are used to minimise noise and interference. In any case capacitor de-coupling of power supplies is widely applied.

7.12 Front End Protection and Filtering Module

A separate external front end protection and filtering module was constructed to provide the digital transceiver with the required high order Nyquist filtering to prevent aliasing for both the transmitter and receiver. It also provides secondary lightning protection (using 90 V spark gaps) and protection from over-voltage and over-current (greater than +20 dBm) that might otherwise damage the receiver RF chain. The over-voltage protection is provided using biased protection diodes. A combination of high voltage (90 V) but slow switching diodes and fast acting (4 ns) diodes (50 V) provide the necessary protection. The input circuit also includes a replaceable one amp fuse. Three

separate filters are constructed side-by-side on a single PCI card as illustrated in the photograph of Figure 7-21 (with the RF screen removed from one filter). The PCI interface connector is only included to provide power (which is then regulated) to bias the protection diodes and to provide a mechanical mounting so the module can be inserted in the same PC as the digital transceiver board.

Each anti-aliasing filter consists of two separate sections. The first is a 7th order elliptic LPF [Williams, 148] with a corner frequency of 28 MHz which provides an attenuation of 60 dB at 36 MHz. Screened, ferrite cored tuneable inductors are used to allow the best compromise between insertion loss, pass-band corner frequency, and transition to be found. The second filter section is a 9th order elliptic LPF with a corner frequency of 28 MHz and an attenuation of 85 dB at 36 MHz. In this section air cored inductors are used for their high Q to provide the greatest possible overall attenuation. To achieve the high selectivity required RF shielding is an important aspect of the design. A shield milled from solid aluminium provides separate screened compartments for the input protection circuit and each of the two LPF sections.

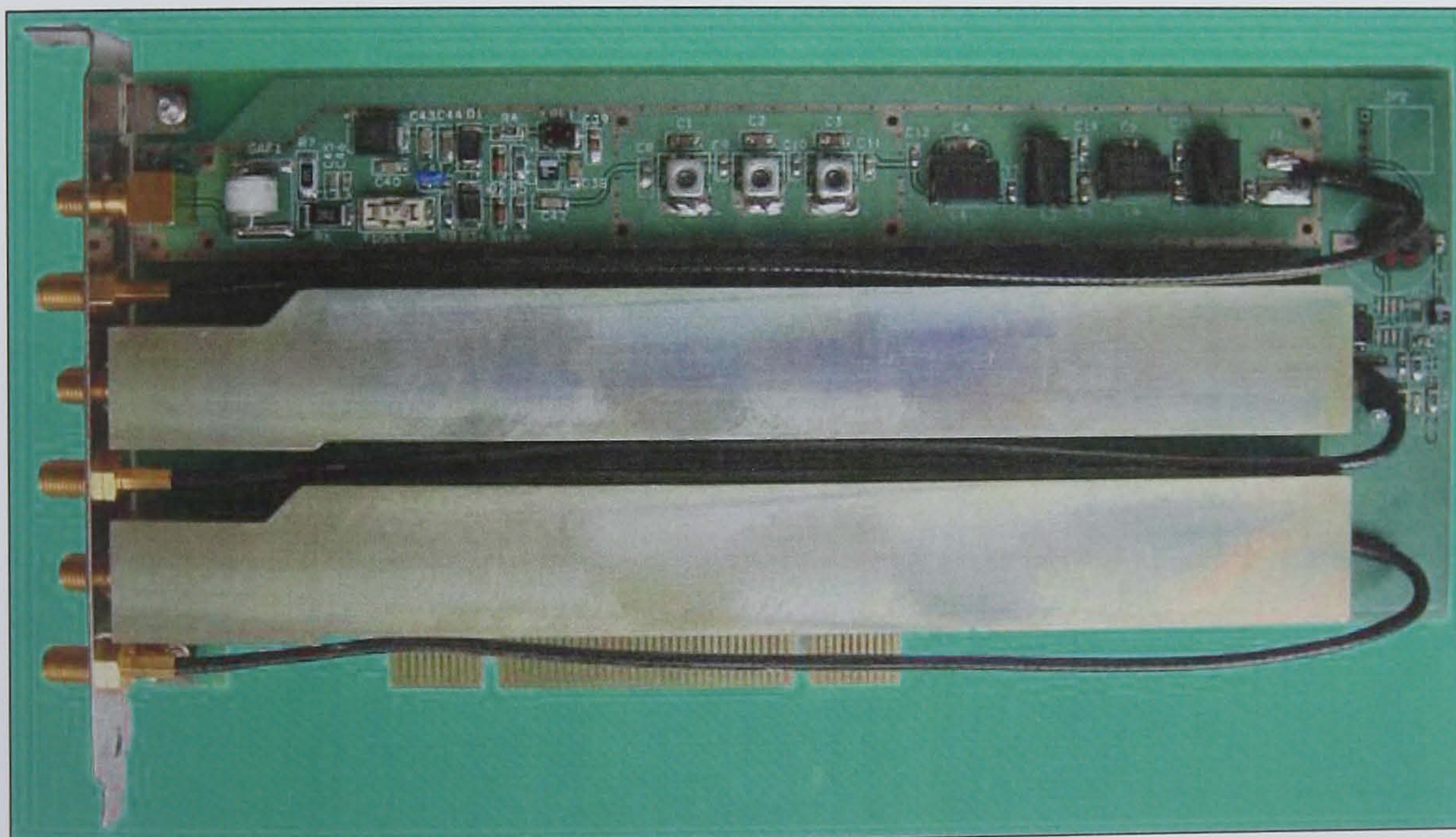


Figure 7-21 Triple PCI Front End Protection and Filtering Module

7.13 Construction Techniques

In order to ensure that the prototype transceiver performance was maximised great care was taken during the circuit design and PCB layout process. The design is virtually 100% surface mount (SMT). Small SMT component geometries (short lead lengths etc)

minimise stray inductance and capacitance. A ten layer PCB was utilised with the ‘stack-up’ shown in Figure 7-22 made from FR4 material. High speed signal design techniques (e.g. [Johnson, 149]) were applied including alternating ground planes, the use of a 50Ω controlled impedance routing layer for fast clocks and signal termination to minimise reflections.

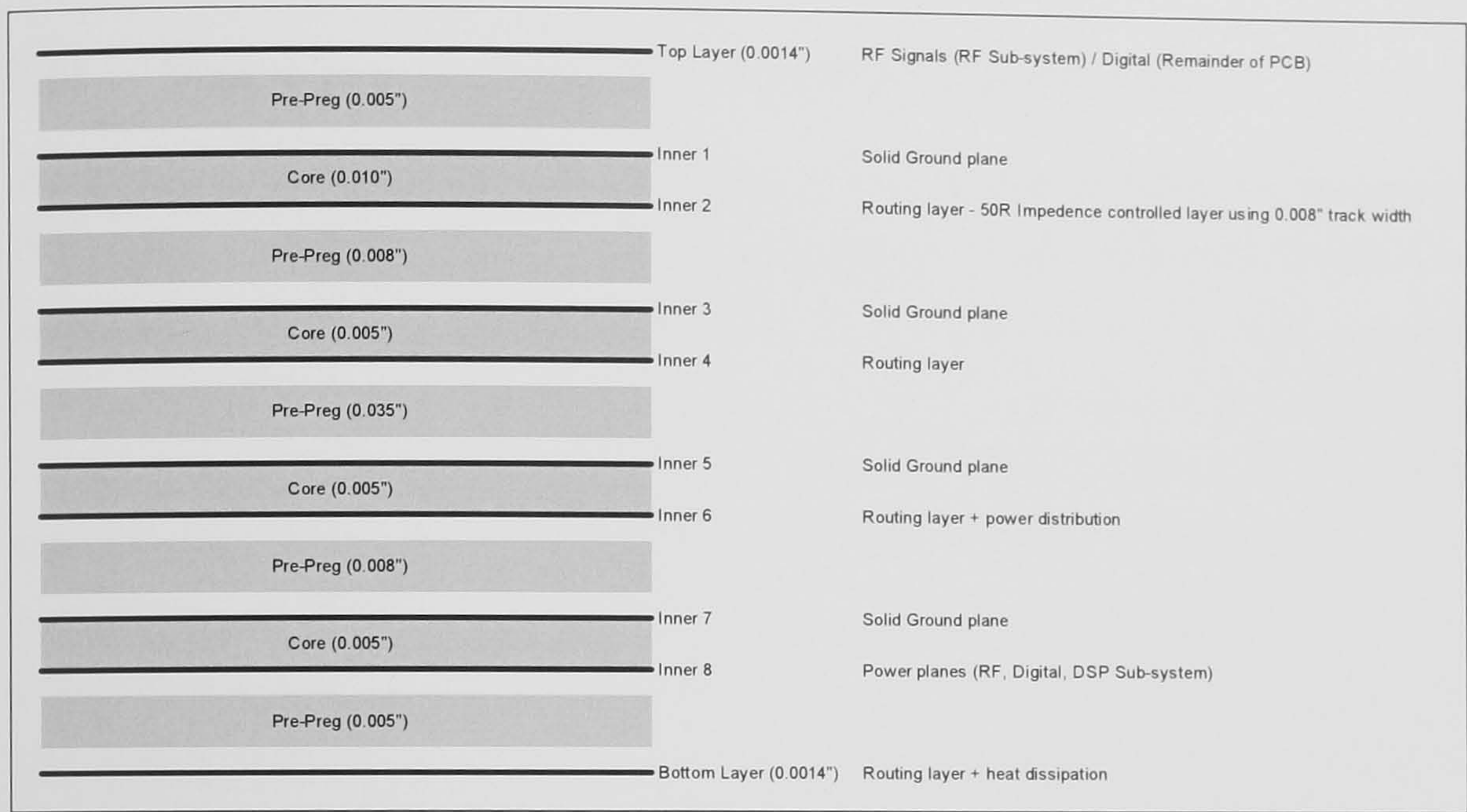


Figure 7-22 Digital Transceiver PCB ‘Stack-up’ (0.062”±0.008 Finished Thickness)

A solid ground plane was utilised as the second layer of the board over the entire RF section. All RF traces were run on the top of the board, which was laid out in the direction of the signal flow to minimise circulating currents. Unused portions of the top layer then had a grounded copper ‘pour’ applied. Additionally provision was made to allow an RF screen to be fitted over each receiver channel. Following careful investigation it was decided to implement the entire board using a single solid ground plane rather than separating analogue and digital sections. To prevent circulating ground return currents induced by noisy digital circuits from impacting the performance of sensitive analogue components a ‘cut’ into the ground plane was made around the lower right hand corner of the analogue section of the board.

Digital control lines running to components in the analogue section were run beneath the ground plane until directly at the applicable device. In a number of cases it was found that additional filtering measures were required to prevent noise being induced (e.g. control lines to RF switches as shown in Figure 7-14). The ADC sampling clock lines were routed as 50Ω differential pairs in a grounded ‘channel’ (i.e. surrounded by copper on all sides).

Multiple, separate power supplies were used to prevent interaction between analogue portions of the circuit. All digital power supplies were completely separate. Decoupling capacitors were mounted as close as possible to all appropriate devices. In a number of cases additional filtering in the power supply lines was used to improve noise immunity.

7.14 Digital Transceiver Control Software Architecture

The host control software for the digital transceiver is implemented in C++ [Stroustrup, 150] using a strongly object oriented methodology. The Microsoft Visual C++ development environment has been used. The abstract class *CBoard* describes a generic PCI board and defines a common API but not its implementation. The derived class *CPlx9054Board* adds the necessary specialisation for a PCI board with a PLX9054 interface device (and can be instantiated). This class includes implementations of the methods required to access and utilise the board (including accessing the board through a memory mapped interface, establishing DMA transfers, controlling interrupts etc). The further derivation *CI2OPCIBoard* adds the functionality for an I²O based messaging suite which is described more fully in the next chapter. The digital transceiver is encapsulated in a class called *CDigitalTransceiver* derived from *CI2OPCIBoard*. Figure 7-23 shows the class hierarchy in a standardised unified modelling language (UML, [OMG, 151]) diagram. An object of type *CDigitalTransceiver* is instantiated for each digital transceiver board installed in the host PC.

A *CDigitalTransceiver* object contains object definitions for all of the functional peripherals within the transceiver such as the frequency standard (*CFreqStd*), the DSP sub-system (*CProcessorSite*) etc. This allows each of them to be controlled via a logical, well defined, API. This technique abstracts the application software from the details of both the peripheral implementations and any hardware specific (i.e. host/digital transceiver board) interactions. For example to set the frequency of a receiver channel the applications software method would simply be:

```
my_transceiverObj.m_receiver.SetFrequency( channel, frequency );
```


Where applicable a logical peripheral may be made up of a number of elements which may map to physical elements. For example the receiver peripheral (*CReceiver*) contains a Graychip GC4014 (*CGC4014*).

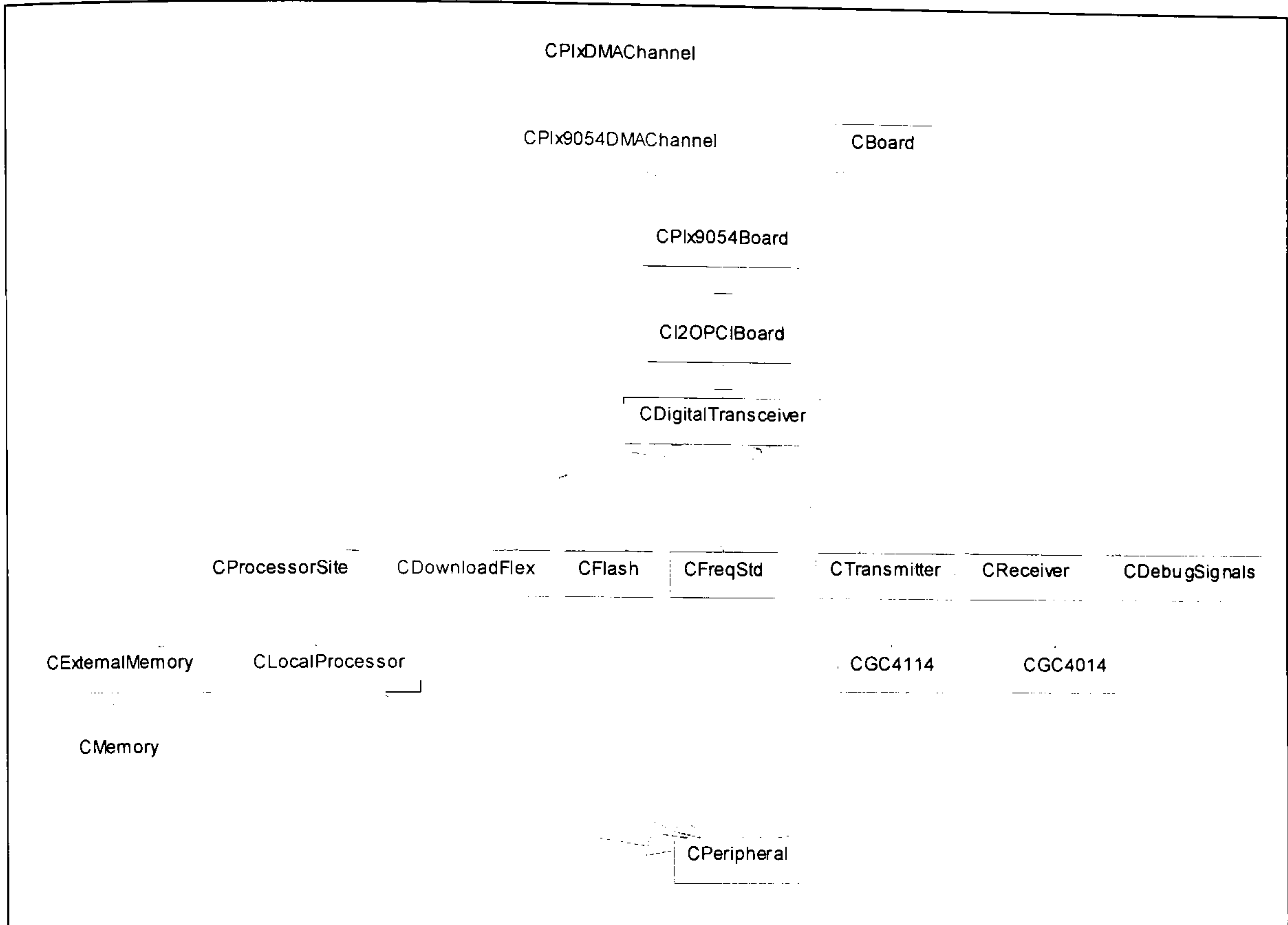


Figure 7-23 Class Diagram for Digital Transceiver (*CDigitalTransceiver*)

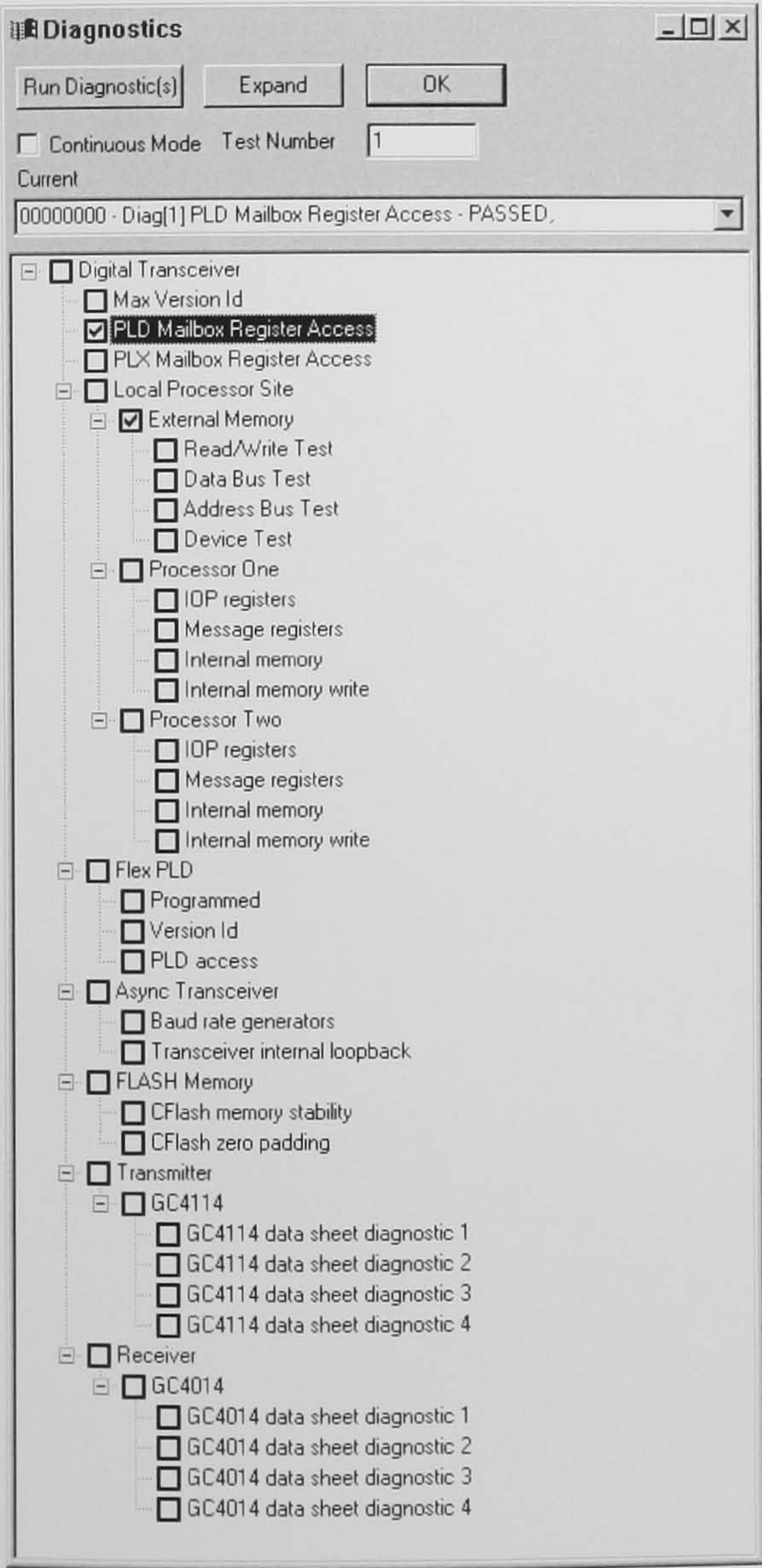
7.15 Built-in Self Test and Diagnostics

An important capability of the wideband transceiver board is its ability to be re-configured by software. This, together with the C++ class-based object oriented implementation encourages test and diagnostic methods developed during the development of logical peripherals to be retained within that class. A number of confidence and performance verification functions have been implemented allowing all the major transceiver sub-systems to be tested. The self test options include:

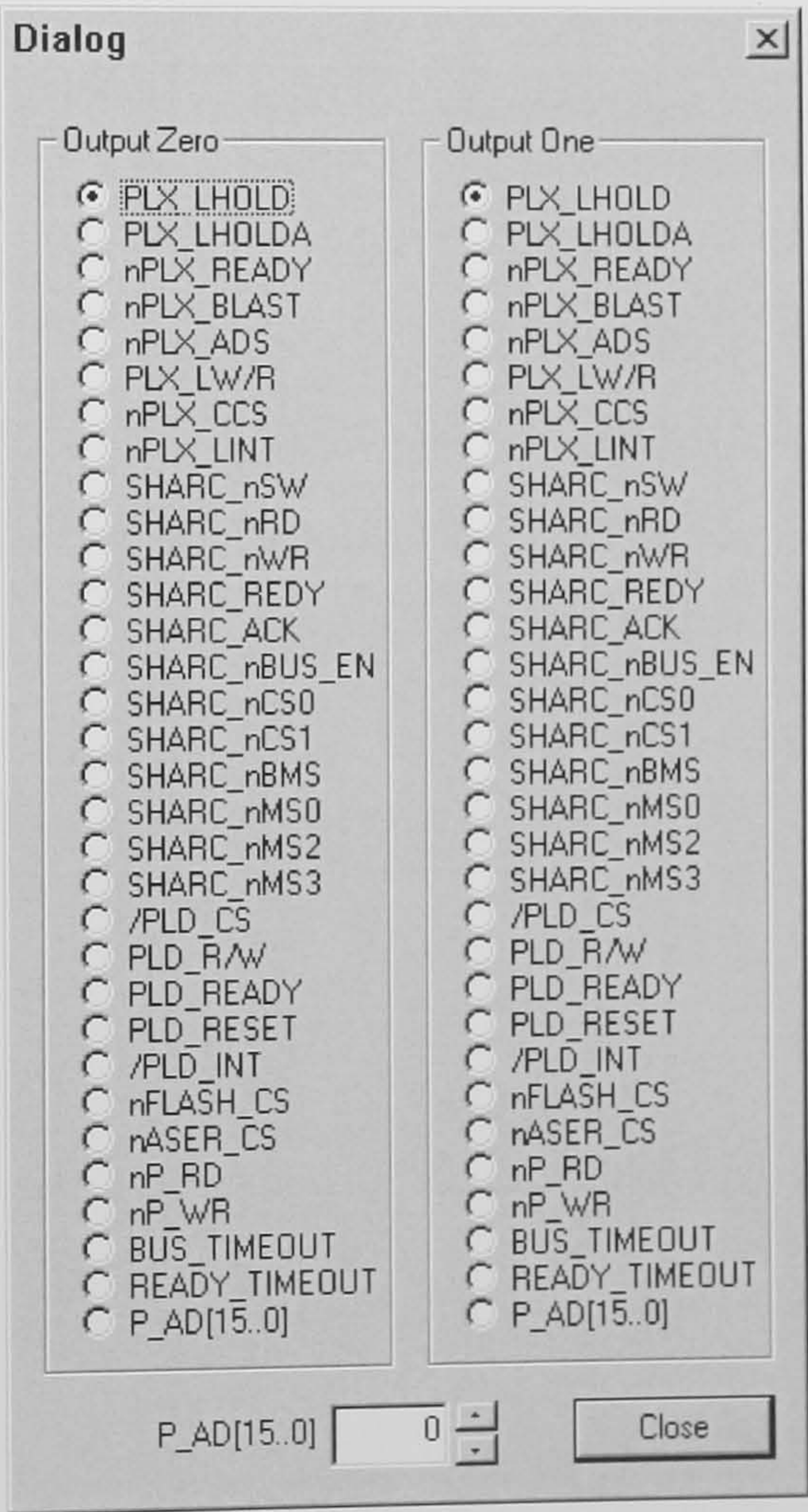
- Ability to loop back transmitter RF output to receiver RF input;
- DUC and DDC self test functions;
- Digitally controlled attenuators and gain control stages;
- Master Oscillator PLL;
- DSP Sub-system (SHARCPAC Site) configuration tests;

- Memory tests; and
- PCI Interface verification.

An elegant solution to managing these diagnostic routines has been developed. All the functional elements within the *CDigitalTransceiver* (including itself) are derived from a base class *CPeripheral* which provides a common set of methods primarily used to manage the diagnostic capabilities. *CPeripheral* provides a series of methods to identify, enumerate and instigate the available test methods. It is then straightforward to implement a function to automatically navigate the *CDigitalTransceiver* class hierarchy and build a diagnostic tree of all the available diagnostics for the board. The resulting GUI (shown in Figure 7-24a) allows any combination of tests to be run. If all of the tests are run a ‘pass/fail’ indication for the whole board is returned.



a. Digital Transceiver Diagnostic Tree



b. Support for Hardware Analysis

Figure 7-24 Diagnostics for Digital Transceiver Platform

The wide use of PLDs in the digital transceiver implementation has been exploited to make the development and debugging of new capabilities easier. By incorporating a digital multiplexer in both the bus arbitration CPLD and the processing FPGA with outputs that go to (currently) unused pins on one of the digital interface connectors it is possible, under software control (Figure 7-24b), to select and monitor a wide range of internal signals using a multi-channel digital oscilloscope or logic analyser.

7.16 Chapter Summary

This chapter has described the implementation of a wideband, multi-channel digital HF transceiver (HF software radio). In the next chapter the development and implementation of a new, event based processing architecture for the digital transceiver will be presented. Chapter 9 describes a wideband HF channel sounder application that utilises the digital transceiver.

Chapter 8.

A High Performance Event Driven Processing Architecture

The previous chapter described the architecture and implementation of a wideband digital HF transceiver (software radio). The transceiver's highly programmable heterogeneous processing architecture (as configured) employs dual DSP processors, an FPGA and can also make use of the host PC processing capability. The PC host control software, which is strongly object oriented, and written in the C++ language was introduced.

This chapter presents a new high performance, event driven processing architecture and its implementation on the digital transceiver platform¹. It has been specifically designed to allow applications to make effective use of the disparate processing resources available whilst abstracting many of the complexities of the hardware implementation and associated data transfers from application software.

The work presented in this chapter focuses on the deployment of software and its subsequent interaction in a heterogeneous architecture. Other relevant work considering deployment of processing across different radio architectures includes the European Union Configurable Radio with Advanced Software Technology (CAST) project (e.g. [Madani, 152]). This is also considering techniques applicable to FPGAs including advanced ideas such as partial re-configuration [e.g. Lund, 153]. Other major areas of work in the area of application deployment (waveform download) include the software communications architecture (SCA, [DOD, 154]) being developed for the US Joint Tactical Radio System (JTRS) programme² [DOD, 155]. The JTRS SCA specifies a framework for the deployment of waveform applications on software radios. The ultimate goal is to allow the same waveforms to be deployable on multiple different hardware platforms (waveform portability).

¹ This architecture was jointly conceived, refined and implemented by the author and Mike Bova of CRC as part of the UK/Canada research collaboration.

² The first issue of the JTRS SCA was made public in May 2000. Waveform deployment has grown to become a major software radio research area since around that time (the EU CAST programme started in April 2000).

8.1 Asynchronous, Event Based, Processing Architecture

A processing architecture has been developed to provide the mechanisms and supporting infrastructure to allow the deployment of applications on the HF digital transceiver (software radio) which are able to make efficient use of its heterogeneous processing capabilities.

Interfaces to the real analogue world, via ADCs or DACs, are based on sampled time. Solutions that react to the arrival of each sample, processing them and then waiting for the next sample are generally very inefficient. This is because the amount of code required to orchestrate the processing (e.g. register saving, context swapping) is often much greater and more complex than the processing itself. Worse still, in a sampled based approach, if the processing time ‘window’ for a sample is missed then it results in an unrecoverable error. For this reason it is usually more efficient to design a system to collect a number of samples and then to process these as frames of data. The size of the data frames is determined by a number of constraints including the size required to achieve acceptable efficiency, acceptable delays (i.e. latencies) in the system and available memory resources.

In many cases the processing required by an application can be functionally decomposed. Where it is sufficiently complex it may need to be spread across a number of processors to achieve the required throughput. Although this is a simple idea conceptually it can be particularly difficult to implement in a heterogeneous processing architecture or one that does not support effective mechanisms for passing data between processors.

A new processing architecture has been implemented, developed from ideas employed in existing homogeneous event based processing models (e.g. the message pumps used in Microsoft Foundation Classes, [Microsoft, 156]). In order to maximise processing capability whilst maintaining the system responsiveness required for real time processing, tasks are broken up into manageable ‘processing chunks’ encapsulated in functions with defined input/output interfaces. An event based processing scheme is implemented in which these functions are triggered by the arrival of a message accompanied by any required input data (active messaging). The last action of a processing function will normally be to dispatch a message to trigger the next stage of processing supplying its output as the next function’s input. A foreground ‘message

pump' on each processor repeatedly takes messages from its input queue and then calls the required processing function. In a simple system with a single processor this effectively results in each processing function being undertaken in turn. In a more complex system the processing functions can be spread across several processors and external events may queue messages to be processed at any time (i.e. from processing contexts). In a system that is nominally single threaded the queue is processed in the order that messages arrive. This architecture is an effective way of implementing complex processing across a heterogeneous network of processors particularly if the mechanisms required to transfer messages between different processors can be abstracted (virtualised).

On first inspection the need to package the output data from one function into a message and then to send it onward appears inefficient. However, in a single processor implementation, the actual data need not be transferred and the message need only pass a pointer to the data. In a multi-processor system with shared memory resources (such as the DSP sub-system in the digital transceiver) the same technique is applicable. Where processors do not share a memory space a data transfer of some kind is required in any case.

The proposed architecture is not conceptually complex and, with a lightweight implementation, allows the processors in a system to run applications with minimal overhead. The use of queues to schedule the processing associated with each message means that, even if a particular event occurs which results in a processor falling behind, as long as it has a sufficient mean processing capacity it will catch up and satisfy the demanded load. The message based processing architecture also offers a straightforward way of distributing the processing load across a number of processors in a system. This is done manually in the current implementation but it would be possible to extend this to a more dynamic scheme where messages are passed to the most lightly loaded processor. As a future enhancement it would potentially be possible to dynamically change the system's function, for example using memory overlays and partial reconfiguration, whilst it continues to run.

8.2 Digital Transceiver Platform

The asynchronous event based processing architecture has been implemented on the digital transceiver introduced in the previous chapter. The host (PC) software is

implemented in the C++ language under the Microsoft Windows NT operating system (OS) which supports multi-threading and interrupt/event based processing. Although the Windows OS was found to be responsive it is not considered to be a true real-time OS [Jorgenson, 157] and software needs to allow for this. For example, there are no guarantees about the response time to a particular event (it depends on what other activities are in progress).

The local bus processor (i.e. SHARC processor) software was almost wholly implemented in C-language¹ with just one short routine having to be implemented in assembly language (to trigger an interrupt). The local bus processors did not run an underlying real-time operating system (RTOS).

The key goals of the implementation were as follows:

- To virtualise the hardware interfaces between host and local bus processors;
- To provide an event driven, asynchronous message processing architecture employing a 'push' messaging model;
- To allow local bus processors to act as servers fulfilling host PC (client) requests;
- To be an efficient, light-weight implementation that provided high performance using background (DMA) transfers;
- To effectively support asynchronous 'real-time' processing under a non-real time host OS (Windows NT) and without a local bus real-time operating system (RTOS);
- To not preclude traditional data transfer strategies (e.g. data 'pull model) if required;
- To provide sending agent methods to allow both 'blocked' (return after sending message) and 'non-blocked' (fire-and-forget) message dispatching;
- To support direct inter-local bus processor and potentially host side inter-object messaging; and

¹ The local bus processor software was implemented in C because at the time the software development was undertaken (Spring/Summer 2000) no C++ compiler was available. C++ would have been the language of choice.

- To use pre-defined user message types (with well formed payloads defined as C-language structs) and wherever possible to use implicit addressing to make the messaging and location of processing tasks largely transparent to user applications.

8.3 Intelligent Input/Output (I₂O) Messaging

8.3.1 Introduction to the I₂O Messaging Standard

Intelligent Input/Output (I₂O, [I2O-SIG, 132]) is a high performance messaging system that has been developed and standardised by the PC industry, specifically the I₂O special interest group (I₂O-SIG). It is intended as a protocol to support fast data transfers between a PC and hard disks, network cards etc. I₂O is a low level protocol intended for use with DMA engines over fast buses (e.g. PCI). It is defined using a layered model which includes a hardware driver module (HDM) which interfaces to a specific hardware implementation, an operating system (OS) specific Module (or OSM) which provides a low level API and a standardised I₂O messaging layer. It includes a series of defined messages to support transactions to common PC peripherals (e.g. hard disk controller, network interface cards).

The aspect of I₂O that is of specific interest is its low level data transfer architecture. It is an asynchronous, frame based ‘push’ messaging model where the sending agent (data source) is responsible for delivering messages to a destination (data sink). This is achieved by reserving memory for multiple, fixed size (*a-priori* defined) data frames at all potential data sinks to hold arriving messages. A series of queues is maintained to allow a sending agent to be allocated a free memory frame at the destination, transfer a message to it and only then to inform the sink that a new message frame is waiting for it to process. Where the variation in message size is limited and DMA transfers are used to send the messages this makes for a highly efficient (high speed and low overhead) transfer protocol. It is this aspect of I₂O that has been leveraged for use in the new asynchronous event based processing architecture presented in this thesis.

8.3.2 PLX9054 I₂O Messaging Unit Implementation

The PLX9054 PCI interface device that has been used in the digital transceiver implementation provides hardware support to implement a low level I₂O transfer

engines. Specifically it supports queues (circular buffers) for message frame address (MFA) management. The standard nomenclature that is used views the system from the local bus (i.e. in our case transceiver local bus) side of the PCI interface. Hence inbound refers to transfers from the host to the local bus processors and outbound those towards the PC host. The following circular buffers are defined which hold the memory addresses of message frames:

- **Inbound Free List** – Addresses of unused frames (unused MFAs) in local bus memory for inbound transfers.
- **Inbound Post Queue** – MFAs containing inbound messages awaiting processing by a local bus processor.
- **Outbound Free List** – Unused MFAs in host (PC) memory for outbound transfers.
- **Outbound Post Queue** – MFAs containing outbound messages awaiting processing by the host.

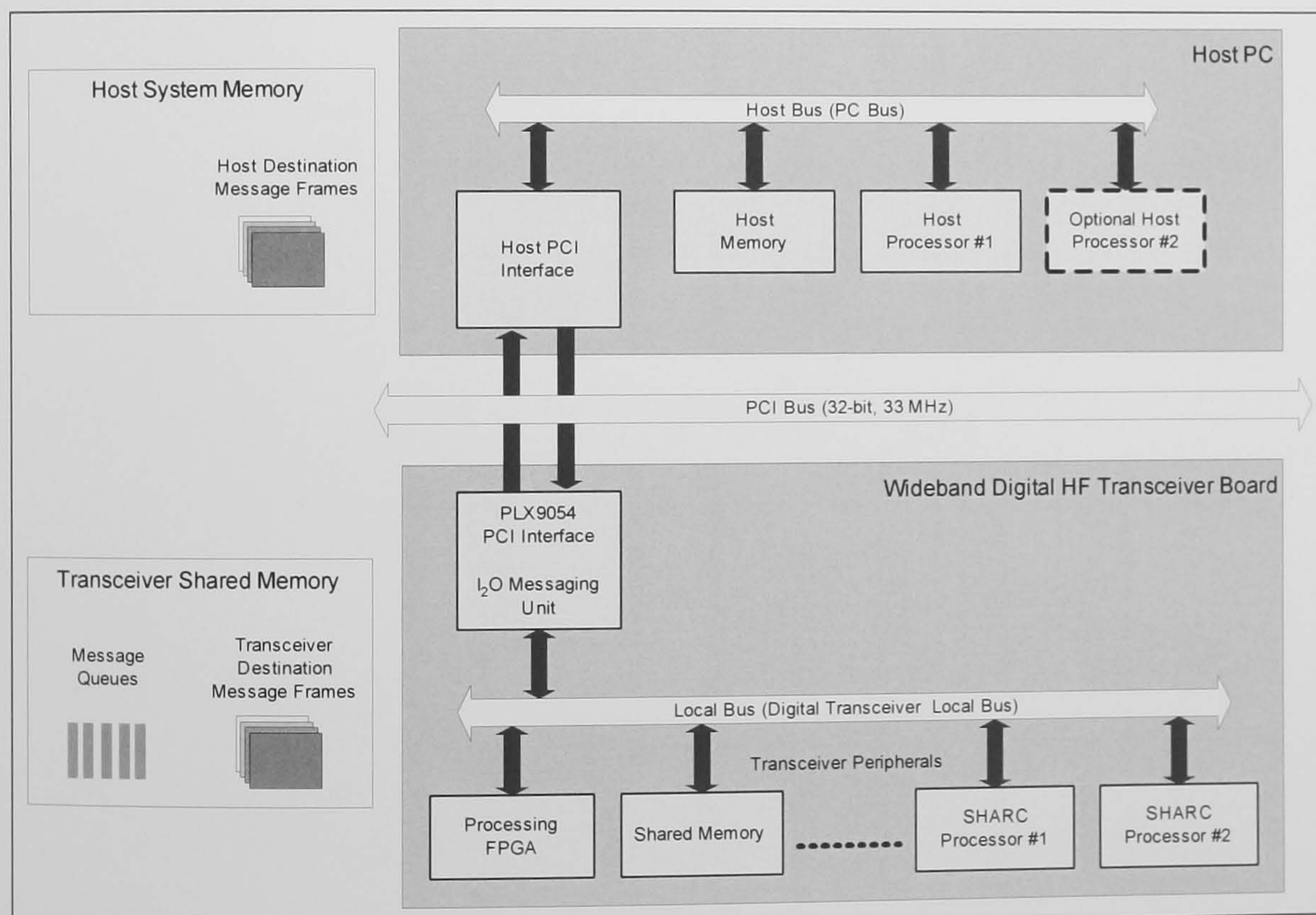


Figure 8-1 Implementation of I₂O Messaging using PLX9054

The queues are all held in memory on the local bus (shared external memory in the DSP sub-system on the transceiver board). The PLX9054 I₂O messaging unit is designed to automatically manage the queues and their pointers (Figure 8-2). Pointers associated

with host access to queues are managed automatically whereas the pointers to queues accessed from the local bus must be locally managed. In use, if a free list is read and an MFA is available its address is returned else -1 (0xFFFFFFFF). To transfer a message the sending agent obtains an MFA from a free list, initiates a DMA to transfer the message to it and then enters the MFA into the appropriate post queue. The action of placing an MFA in a post queue causes an interrupt (IRQ) to be generated at the destination, alerting it that a new message is pending.

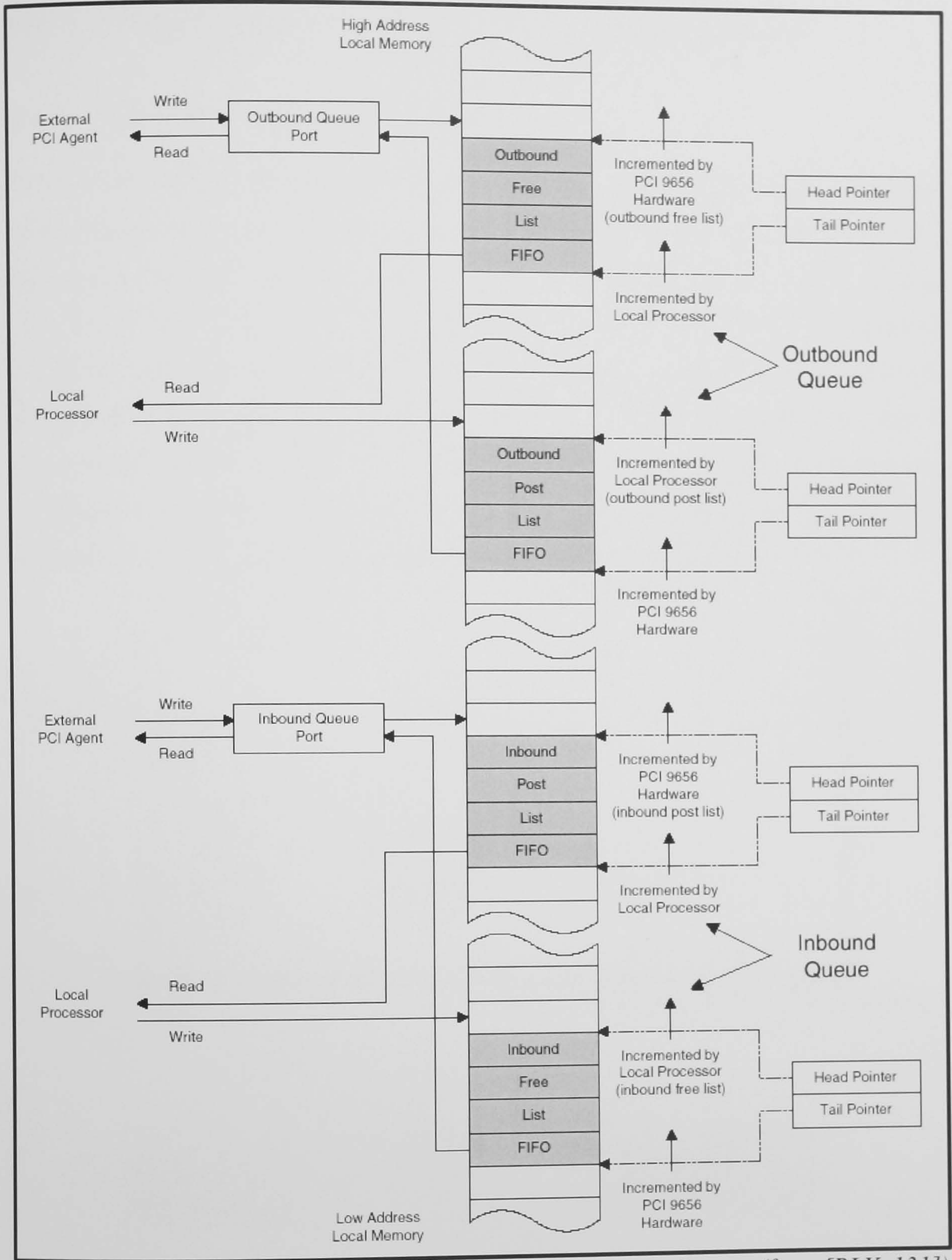


Figure 8-2 Organisation of I2O Messaging Queues (from [PLX, 131])

8.4 Asynchronous Messaging - Software Implementation

8.4.1 Message Format and Addressing

The message structure defined consists of a header and an optional payload. The format of the message header is shown in Figure 8-3. A key field is the ‘Id’ which determines the message routing. The ‘Message’ field (Figure 8-4) is a unique *a-priori* defined value that is used by both the host and local bus processors to determine which function should be initiated by a message. The lower 16-bits of this field are manually enumerated with a unique message identifier (ID). The next 4-bits are used to determine the destination processor. The top 12-bits are currently unused. A common ‘.h’ header file, shared between the host and local processor software implementations, contains a list of the supported message IDs for a particular application.

```
typedef struct _MSG_ENTRY
{
    struct Id
    {
        U32 Class;           // ID of host PC user class
        U32 Object;          // ID of object in host user class
        U32 Message;         // Message ID
    };
    U32 InUseCount;          // MFA in use count (allows multiple sinks for a message)
    U32 SGLFlag;             // Scatter-gather DMA flag (deprecated)
    U32 WordSize;            // Size of payload in 32-bit words
    U32 Pending;             // Is the MFA routing pending? (used when retries required)
    U32 bAutoReturn;         // Auto return MFA on completion of processing?
    U32 Reserved[2];         // Reserved fields
    U32* pPayload;           // Pointer to message payload
} MSG_ENTRY;
```

Figure 8-3 Structure of Message Header

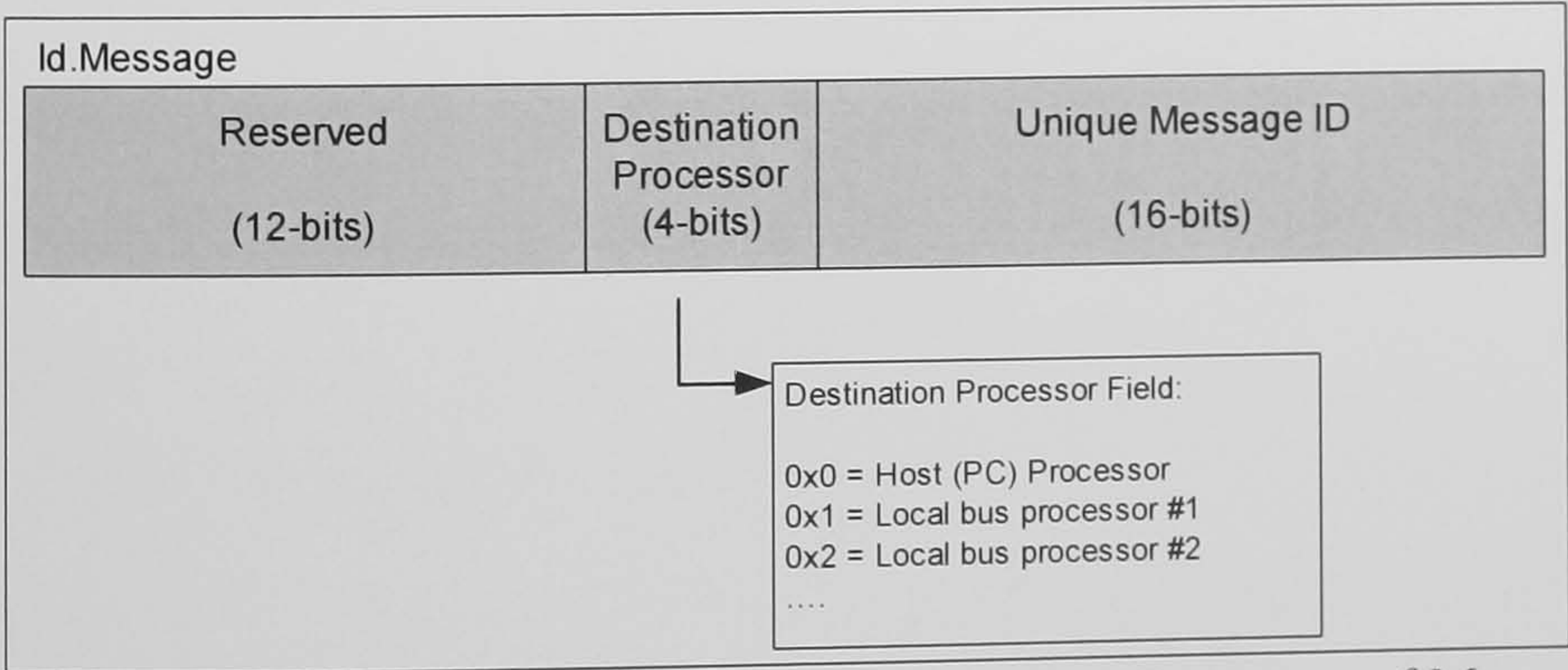


Figure 8-4 Structure of Message ID Field

The processing architecture is designed so that all activities are initiated by the host. This effectively makes the digital transceiver platform a server for the client host.

Enumeration of the class and object that initiates a sequence of processing is undertaken automatically by the architecture. Once an initial message has been sent to a local bus processor the class/object can be retained to allow it to send a message back at any time in the future. Hence asynchronous messaging can occur in multiple directions.

The payload of a message is usually defined as a C-language structure (defined in the same header file as the message IDs) allowing well formed messages to be exchanged.

8.4.2 Message Transfers and Memory Management

As has been seen a message consists of two parts – a header and a payload. With the ‘push’ messaging model implemented, arriving messages are stored in pre-allocated memory frames pointed to by MFAs. This bounds the maximum size of a message (and is coded as a constant). However, a message may be any size smaller than this maximum. In the extreme case (e.g. control signal messages) they may have no payload. In general when a message is sent the user application provides the payload and indicates the message ID. The sending agent then builds a header and sets up a scatter-gather list (SGL) DMA transaction to transfer the header and then the payload to the destination as a single ‘chained’ operation. In host-to-local bus transfers the architecture is intended to allow the posting of the message to the local bus inbound post queue to be appended as a third part of the chained SGL-DMA¹.

8.4.3 Local Bus Processor to Host Messaging

For a local bus processor to send a message to the host (PC) the following actions take place:

- The message is queued for routing by the main local bus message handler. The handler examines the message ID and finds that the destination is on the host PC.
- A destination MFA is obtained from the outbound free list
- A chained scatter-gather DMA transfers the message (header + payload) to a destination MFA (the header contains the message ID and necessary addressing).

¹ However due to bugs in supplied PLX9054 driver software and the device itself this did not work correctly in the system implemented. The work-around that had to be implemented is described later in this chapter.

- The MFA is written to the outbound post list. This action automatically triggers an interrupt (IRQ) at the destination routing processor (the host).

The actions that occur at the host (PC) when a message arrives is as follows:

- When the sending processor writes an MFA to the outbound post list to send a message an IRQ automatically triggers the main message handler which runs as a separate thread, defined in *CHandler*. There is a single main message handler for each transceiver object (i.e. board) in the system.
- The main message handler reads the pending MFA from the outbound post list, examines its address field, and then routes the message to a class message handler (entering it into a queue and triggering an event).
- There is one class message handler per messaging enabled class. This is defined in the templated class *CMessageHandler<T>*. The class message handler, which again runs as a separate thread, examines the message addressing field and routes the message to the specific destination object (again entering it into a queue and triggering an event).
- The object message pump (thread), defined in the templated class *CMessagePump<T>*, processes incoming messages sequentially using the message ID to causes the correct method (member function) to be called.
- When processing within the object method is completed the MFA is returned to outbound free list.

8.4.4 Host to Local Bus Processor Messaging

When a host sends a message with an ID that marks its destination as a local bus processor the following actions take place:

- An MFA is obtained from the inbound free list.
- A chained scatter-gather DMA transfers the message (header + payload) to this destination MFA (the header contains the message ID and necessary addressing).
- The MFA is written to the inbound post list. This action automatically triggers an interrupt (IRQ) at a designated local bus processor which runs the main message handler responsible for all message routing.

The actions that occur when a message arrives in the local bus inbound queue are as follows:

- The single handler running on the designated local bus processor examines the message address field. If the destination processor (which may be the processor running the handler) is recognised and it has registered its message pump (each local bus processor must do this on start-up) then the message is simply queued to that processor's message pump. If it is not recognised an error message is generated and the message is dropped.
- The message pump of each local bus processor runs in the foreground on that processor and simply processes messages in turn calling the designated function associated with the message.

8.4.5 Inter-Local Bus Processor Messaging

An important feature of the asynchronous messaging architecture developed is the ability for local bus processors to make use of the same communication facilities to themselves and between each other. This is key to achieving effective event based processing. A local bus processor may send a message to another local processor or itself using exactly the same function call as it would use to send a message to the host. The message is placed in the routing queue of the main local bus message handler (which runs on a single designated local bus processor). The message ID allows the handler to determine that the destination is a local processor and then simply adds the message to that processor's message pump queue. As all the local bus processors share memory the payload does not need to be copied. This makes the overhead of this architecture minimal.

8.4.6 Host-to-Host Messaging

Whilst the architecture (and indeed the implementation with some minor extensions) readily lends itself to supporting host-to-host messaging this has not yet been implemented. This is because no performance benefits would be realised since the host runs a sophisticated multi-threading operating system (Windows NT) with mechanisms which natively support event based processing.

8.4.7 Host Software Implementation

Figure 8-5 is UML class diagram showing how, in the digital receiver application, the messaging environment is related to the basic control software. The key classes are as follows:

- *CI2OPCIBoard* – This class is a derivation of *CPlx9054Board* and adds methods to utilise its I₂O messaging unit.
- *CHandlers* – A single (static) handler of this type (per process, i.e. per board) is declared within the *CMessageHandlerBase* class. This is responsible for routing messages to the message handlers associated with each class. It is called to perform this routing function whenever a ‘message arrived’ interrupt is triggered.
- *CMessageHandler<class T>* – This templated class is derived from the virtual base class *CMessageHandlerBase*. It results in a routing thread running for each message aware class. Its primary function is to route messages to specific objects (based on addressing in messages). The class message handlers register with the single *Chandler* object.
- *CMessagePump<class T>* – This templated class is derived from *CMessagePumpBase* which is a virtual base class that provides the I₂O messaging capabilities for classes associated with a *CI2OPCIBoard* object. *CMessagePump<class T>* provides a specific object with a message pump thread to undertake event based message processing.

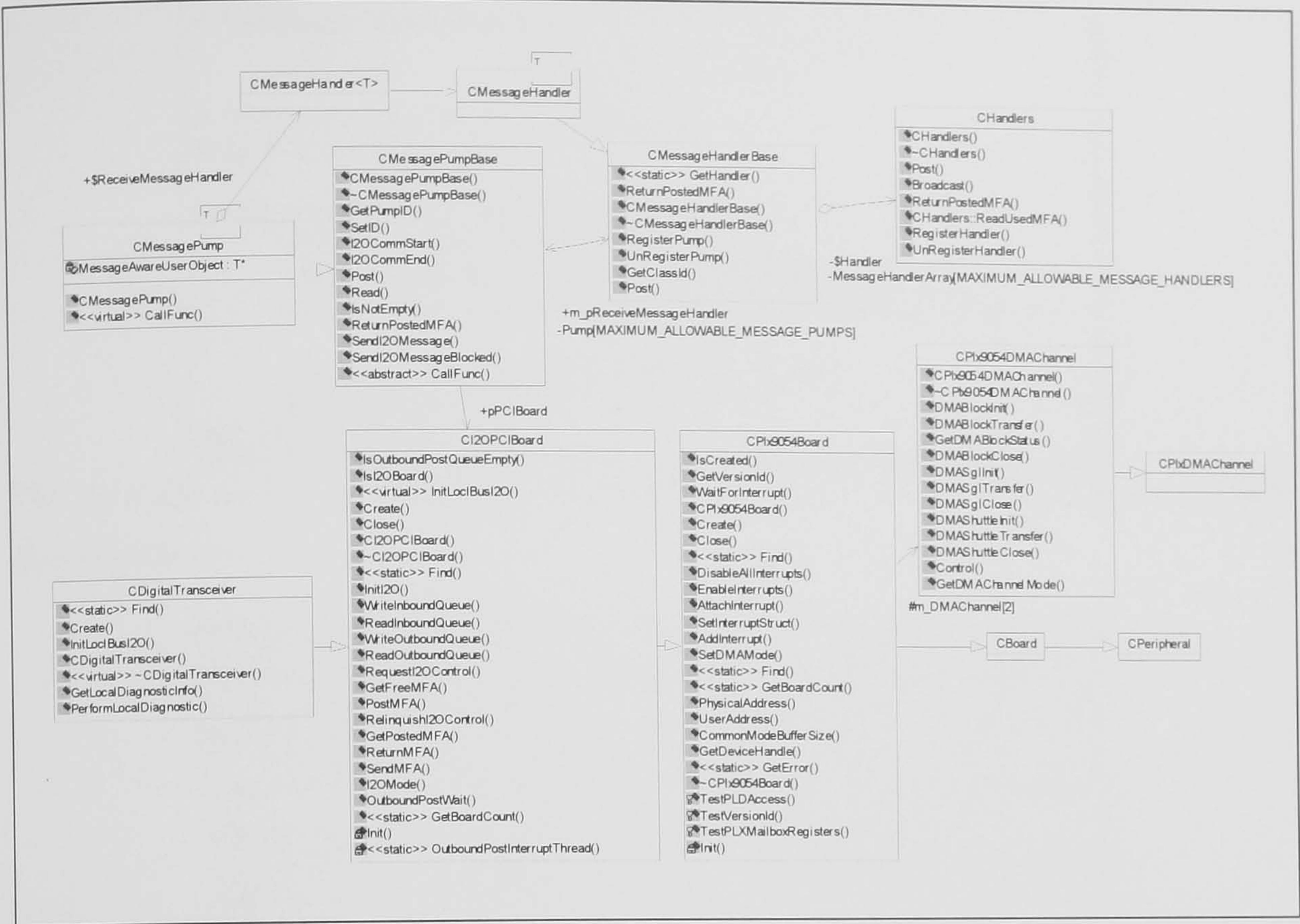


Figure 8-5 UML Diagram of Asynchronous I₂O Messaging Implementation

In order to add the asynchronous messaging capability to a host user class the following code is required to enable messaging:

```
////////////////////////////////////
// CUserDlg dialog

class CUserDlg : public CModelessDlg
{
// Construction
public:
    CUserDlg(CWnd* pParent = NULL);    // standard constructor
    ~CUserDlg();

    ...

protected:
    DECLARE_MESSAGE_MAP()                // Windows message map
    DECLARE_I2O_MESSAGE_MAP(CUserDlg)    // I2O message map
};
```

where the new macro is defined as follows:

```
#define DECLARE_I2O_MESSAGE_MAP(newClass)\
public:\
    BOOL I2OLink(CI2OPCIBoard*);\
    CMessagePump<newClass>* pMessagePump;
```

Then a message map must be added to describe what event should be triggered on the arrival of a particular message type:


```
// PrintfDlg.cpp : implementation file
...
...
// I2O Message map entry for CPrintfDlg class
#include "Board/I2OHandler.h"
...
BEGIN_I2O_MESSAGE_MAP(CPrintfDlg)
   //{{AFX_I2O_MSG_MAP(CPrintfDlg)
    ON_I2O_MESSAGE( USR_MESSAGE_PUTSTR, PutStr, char* )
    ON_I2O_MESSAGE( USR_MESSAGE_ENABLE_PUTSTR, PutStr, char*
)
    ON_I2O_COMMAND( USR_MESSAGE_CLS, Cls )
//}}AFX_I2O_DATA_MAP
END_I2O_MESSAGE_MAP()
```

The message map is defined as a series of simple C++ macros that cause a switch statement to be built:

```
#define BEGIN_I2O_MESSAGE_MAP(newClass)\
CMessageHandler<newClass> CMessagePump<newClass>::ReceiveMessageHandler;\
template<class T>\
void CMessagePump<T>::CallFunc(UINT Id, void* Payload )\
{\
    switch(Id) {\
\
#define ON_I2O_MESSAGE( MessageId, MemberName, TypeCast )\
        case MessageId: MessageAwareUserObject->MemberName((TypeCast)Payload );\
            break;\
\
#define ON_I2O_COMMAND(MessageId, MemberName)\
        case MessageId: MessageAwareUserObject->MemberName();\
            break;\
\
#define END_I2O_MESSAGE_MAP()\
        case -1:\
            default: break;\
    }\
}
```

To enable messaging for an object it must register itself with the messaging system of the board it wants to communicate with. The message sinks are event triggered methods (member functions) belonging to the I₂O enabled class:

```
////////////////////////////////////
// CPrintfDlg Constructor
CPrintfDlg::CPrintfDlg(CWnd* pParent /*=NULL*/) : CModellessDlg(CPrintfDlg::IDD, pParent)
{
    ...
    I2O_REGISTER(CPrintfDlg, &m_pl2OBoard )
}

////////////////////////////////////
void CPrintfDlg::PutStr( char *pString )
{
    m_PrintfScreen.AddString( pString );
}

////////////////////////////////////
void CPrintfDlg::Cls()
{
    m_PrintfScreen.ResetContent();
}
```

The action required to dispatch (send) a message is straightforward. Once a class is I₂O message enabled, defined messages can be simply sent as required:


```
// Send a request message  
void CPrintfDlg::OnRequeststring()  
{  
    I2O_SEND_MESSAGE_BLOCKED( USR_MESSAGE_DO_PRINT );  
}
```

Two alternative send message macros are defined as follows in the I2O messaging implementation:

```
// I2O_SEND_MESSAGE macro definitions  
#define I2O_SEND_MESSAGE          pMessagePump->SendI2OMessage  
#define I2O_SEND_MESSAGE_BLOCKED pMessagePump->SendI2OMessageBlocked
```

The two options allow messages to be sent with the calling routing waiting for the message to complete dispatch (termed a blocked call) or by a ‘fire and forget’ mechanism where the message is queued for dispatch and the calling function returns immediately.

8.4.8 Local Bus Processor Software Implementation

The local bus implementation of the messaging solution is very similar to that for the host side. The principal exceptions are that, because the software is written in C-language and being run on processors with no inherent support for multi-tasking (i.e. no RTOS), each local bus processor has a message pump associated with it rather than the host which has one per class. The message pump and all message processing takes place in the fore-ground. The only activity that takes place in another thread (implemented as an interrupt) is the main message handler (message router) which is triggered whenever a new message arrives to be routed (from a local processor or from the host).

8.5 Implementation Issues

A number of problems were encountered in the implementation of the event based processing architecture. In particular the following issues required additional work to find acceptable solutions:

- A number of errors (bugs) were found in the Windows device driver supplied with the PLX9054 software development tools. Most serious of these was an error that prevented the reliable use of DMA transfers between the host PC and the local bus (digital transceiver board). Insufficient time was available to fully investigate and

resolve this problem so software transfers from host to local bus were utilised but with DMA transfers in the opposite direction.

- An error was discovered in the design of the PLX9054 PCI interface device itself [PLX, 158]. This meant that if both host PC and local bus processor happened to access an I²O queue pointer register at the same time the pointers could be catastrophically corrupted. This problem was overcome by implementing a semaphore using the PLX9054 mailbox registers to ensure only one access occurred at a time.

8.6 Practical Demonstration of Event Based Processing Architecture

Figure 8-6 is a screen dump taken from the host PC with five separate host processes (threads) orchestrating simultaneous processing on the digital transceiver platform. In this demonstration three host objects are independently exchanging data with one local bus processor and two more host objects are independently exchanging data with the other local bus processor. The total achieved throughput is 15 Mbytes/s with the bandwidth evenly distributed (ranging between 2.95 to 3.09 Mbytes/s). The system was found to work well when configured to support 64 message frames each of 4096 32-bit words.

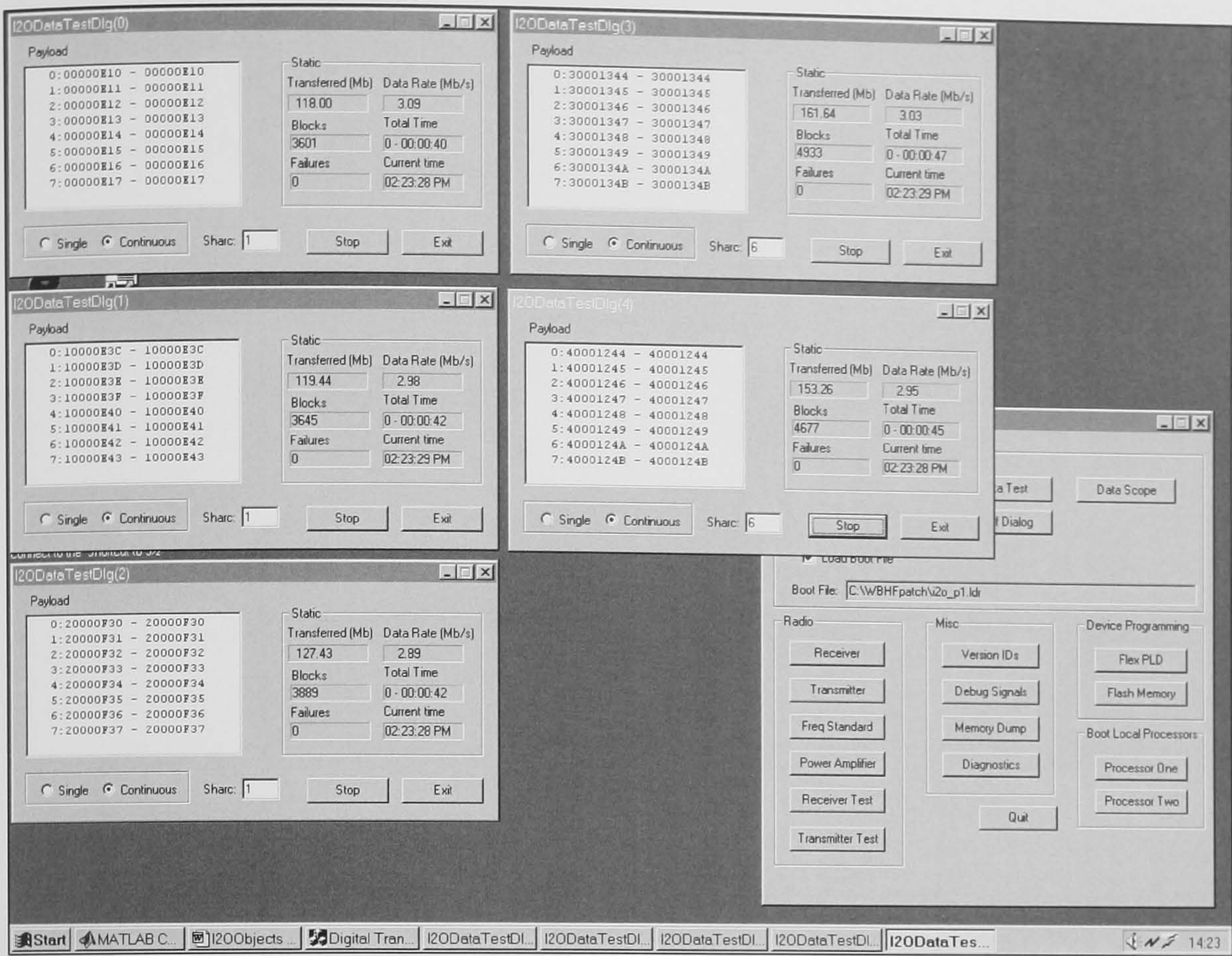


Figure 8-6 Five Simultaneous Processes Running on Digital Transceiver

8.7 Possible Extensions to the Event Based Processing Architecture

A number of possible improvements and extensions to the processing architecture have been identified. These include:

- The local bus processor code is currently written in C because a SHARC C++ compiler only became available after the implementation was complete. It would be interesting to translate the existing code to C++ (which should better mirror the host side software) and to determine if this activity suggests any improvements in the processing architecture. At the very least an object oriented implementation would be more robust because more extensive encapsulation (virtualisation) could be employed. Having multiple dynamically instantiated objects on the local bus processors would likely require a more complex approach to addressing.
- The local bus processor code was written for a cluster of SHARC processors without the benefit of a multi-threaded RTOS. The provision of a multi-threaded environment would be expected to simplify the messaging software infrastructure (but not its efficiency) and may suggest further extensions in capability.

- An improved (i.e. bug-free) Windows driver for the PLX9054 PCI bus interface device to allow DMA transactions to be employed in both directions between host and local bus processors would realise the throughput the architecture is capable of.
- It would be relatively straightforward to extend the capability of the message pumps that process pending message queues to allow messaging with different priorities. This would allow processing of higher priority messages to be expedited.
- Whilst processing functions are manually allocated to a particular processor it might be possible to develop light-weight techniques to allow messages to be routed to the processor that is most likely loaded at any given time based on metrics for historic processing load and (automatic) benchmarking of the time taken to process particular messages.
- The work presented here concentrates on the deployment of application software across multiple heterogeneous processors. It would be interesting to extend the work to look at more flexible ways of configuring both the DSP processors and the PLDs (e.g. [Lund, 153]).

8.8 Chapter Summary

A particular challenge in complex systems such as software radios (e.g. wideband digital HF transceiver) is the deployment of software across a number of heterogeneous processors. This chapter has presented a new asynchronous, event-based, processing architecture which employs lightweight (very low overhead) messaging to allow processing tasks to be effectively distributed across multiple processors and buses. The processing has been implemented on the digital transceiver hardware (Chapter 7) and its effectiveness has been demonstrated. Suggestions for further developments and improvement have been made. The next chapter presents a new wideband HF channel sounder and its implementation on the digital transceiver using this processing architecture.

Chapter 9.

Application of Digital Radio to HF Channel Characterisation

There is an ever increasing demand for high throughput communications for all bearers including the high frequency (HF) radio channel. Significant advances have recently been made in improving throughput for conventional narrowband channels. However, as identified in Chapter 2, work is still required to provide an accurate, well validated characterisation of the wideband HF channel that is able to describe both the large scale features (such as multiple modes, Doppler shift, Doppler spread etc) and, significantly for modem designers, the detailed time varying properties of these channels such as the correlation of fading at different delays within a mode.

This chapter provides a brief introduction to channel sounding techniques before introducing a new oblique Wideband HF Ionospheric Sounder for Propagation Environment Research (WHISPER). This is a low power, pulse-compression sounder based on software radio techniques, and implemented as an application on the wideband HF transceiver introduced previously. The WHISPER sounder theory of operation is presented and its implementation described. The design of sounding waveforms suitable for an investigation of wideband (~80 kHz) channel characteristics over mid-latitude Skywave propagation channels is discussed. Finally results of back-to-back measurements performed at RF are analysed to confirm the performance of the sounder.

9.1 Introduction to Ionospheric Channel Sounding

This section provides a brief introduction to channel sounding approaches and techniques.

9.1.1 Sounding Geometries

There are three basic geometries applicable to ground based ionospheric sounding (Figure 9-1):

- **Vertical Sounding** – In vertical sounding a signal is launched directly upward and is received in the same location. This allows direct measurement of the ionospheric layer heights.
- **Oblique Sounding** – In this case the transmitter and receiver are separated and the path is sounded obliquely. Oblique measurements can be made directly over the same path that will be used for communications. Special measures have to be taken to remotely synchronise the transmitter and receiver.
- **Backscatter Sounding** – In backscatter sounding the transmitter and receiver are closely located (or co-located). The path is sounded obliquely and signals are returned to the receiver by ground scattering at the far end.

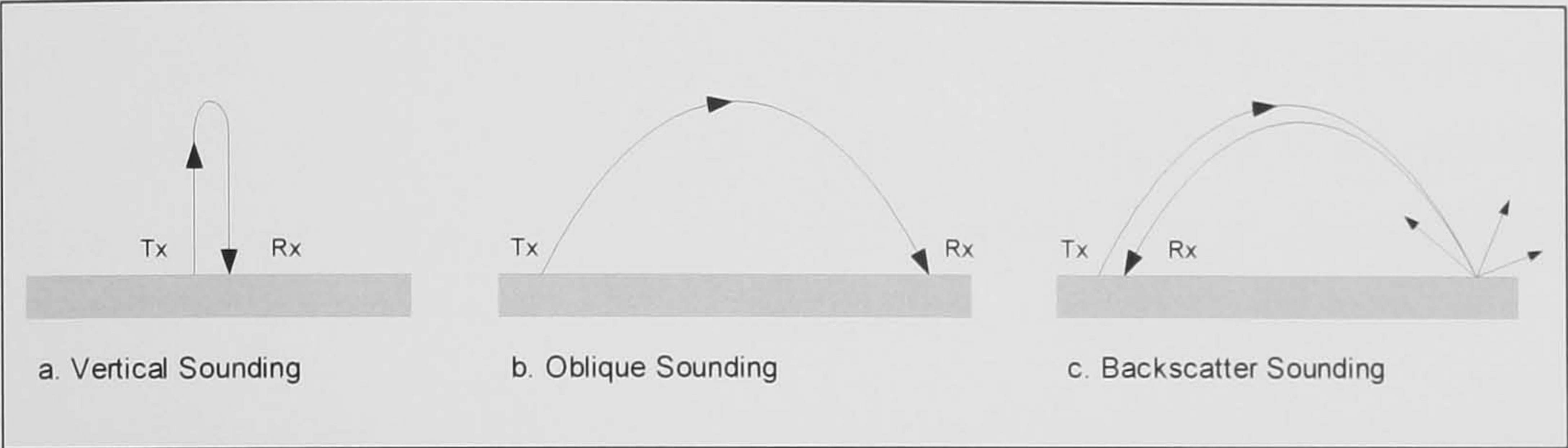


Figure 9-1 Alternative Sounding Geometries

9.1.2 Sounding Techniques

The most widely used sounding techniques at HF are pilot tone sounding, pulse sounding and Chirp sounding:

9.1.2.1 Pilot Tone Sounding (CW Sounding)

A basic technique for investigating the effects of Doppler shift and Doppler spread on an HF channel is to transmit a single tone at the frequency of interest. Fourier analysis can be used to obtain the received signal’s power spectrum [Davies, 3]. This technique has been widely use by workers such as Warrington [Warrington, 159]. Whilst it has the benefit of simplicity it does not directly allow information on propagation delays and individual modes to be extracted.

9.1.2.2 Pulse Sounding

In pulse sounding a pulse approximating an impulse is transmitted in order to measure a channel’s impulse response. In order to increase the SNR of measurements a pulse

compression waveform [Skolnik, 160] can be sent instead of a short pulse realising processing gain when processed at the receiver [e.g. Wilkinson, 161]. The principal requirements of the sounding waveform are that it has good time resolution (ideally approaching the reciprocal of the channel bandwidth), has a large dynamic range (i.e. good peak-sidelobe ratio) and adequate tolerance to Doppler offsets for the channel being investigated. Common pulse compression waveforms include Barker sequences [Barker, 162], periodic pseudo-noise (PN) sequences [Fan, 163], Frank sequences [Frank, 164] and complementary sequences [Golay, 165].

Pulse sounders are commonly operated in one of two basic ways. Where the time varying properties of a single channel are to be investigated repeated measurements need to be made on that channel at a rate exceeding the Nyquist rate of the channel (i.e. at a rate equivalent to the largest Doppler frequency). As will be seen a time series of complex channel impulse responses (CIRs) can be analysed to obtain an estimate of the channel scattering function [Bello, 166] which describes how the transmitted pulse is distributed in delay time and frequency (Doppler) by a dispersive channel.

In an alternative mode of operation, by making measurements on a large number of frequencies, an ionogram can be constructed (e.g. Figure 9-2).

Examples of HF pulse compression sounders include:

- **DAMSON** – The DAMSON sounder [Davies, 49] employs pulse compression waveforms make measurements of the channel scattering function on oblique paths. It is generally operated in a bandwidth of 3 kHz using a Barker-13 pulse compression waveform to allow measurements of highly dispersive channels.
- **ITU Measurement System** – As part of an ITU HF measurement campaign [ITU, 167] a system which includes a narrowband (3 kHz) pulse sounding capability has been developed by Darnell et al [Darnell, 168]. This system utilises complementary sequence sounding waveforms.
- **Digisonde** – The Digisonde Digital Portable Sounder (DPS) [Reinisch, 169] operates in a bandwidth of 20 kHz. It may be operated vertically, obliquely or in a back-scatter mode.
- **Wideband Pulse Sounders** – Results from work with wideband pulse sounders (between 20 kHz and 1 MHz bandwidth) have previously been reported by [Perry,

21], [Basler, 170] and [Wagner, 20]. These have included investigations of the channel scattering function under a range of propagation conditions and at different latitudes. However, no systematic analysis of the time varying characteristics of individual propagation modes has been presented.

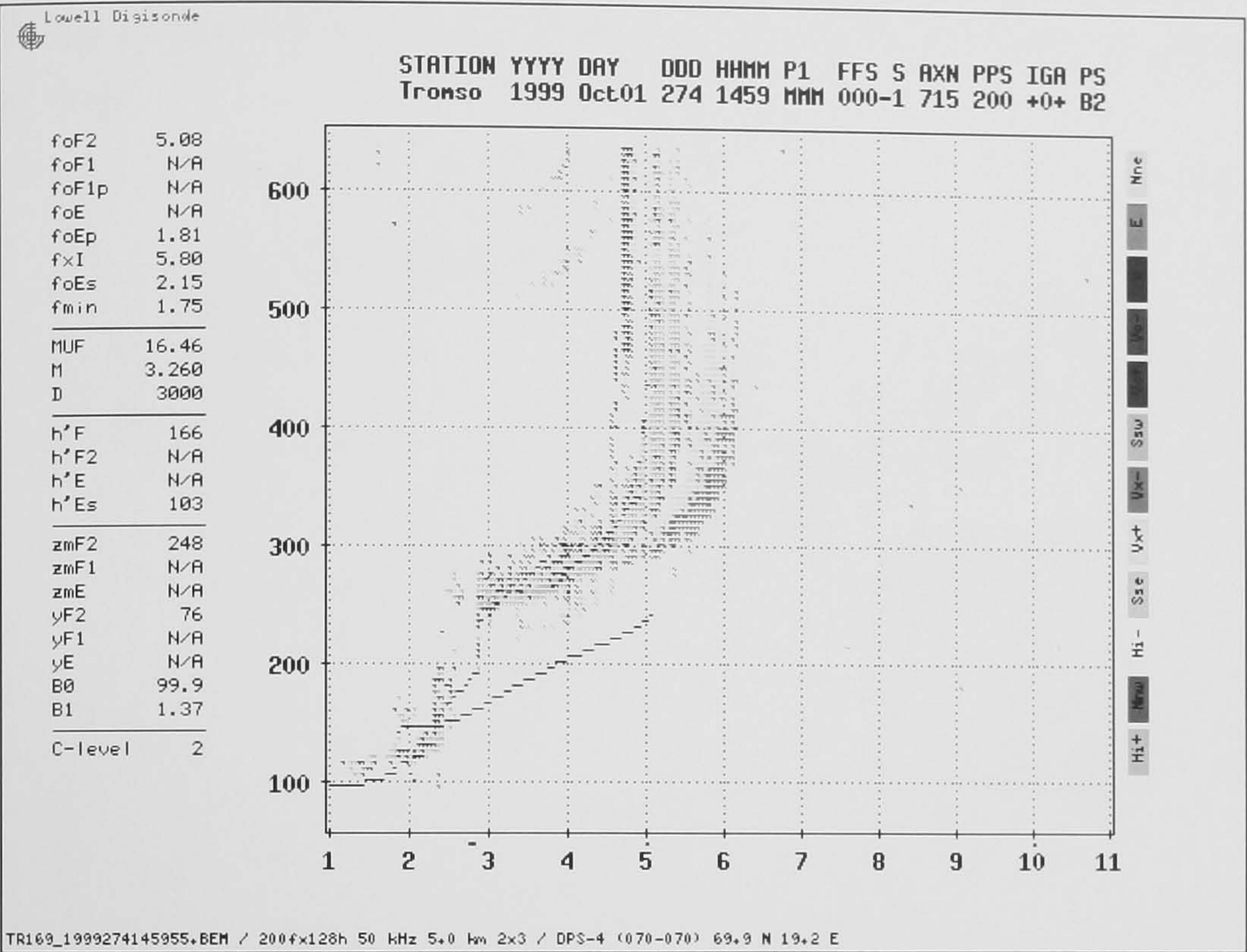


Figure 9-2 Vertical Ionogram Produced by a Digisonde Pulse Compression Sounder

9.1.2.3 Chirp Sounding (Linear FM Sweep)

An alternative technique to pulse sounding is Chirp sounding [Barry, 171] in which a (normally linear) frequency modulated continuous wave (FMCW) signal is transmitted. Typically Chirp sounders sweep across the whole HF band (2-30 MHz) at a rate of 100 kHz/s. This is typically generated phase coherently sweeping a local oscillator or using a direct digital synthesiser (DDS). The obliquely located receiver is synchronised so that it starts sweeping its LO at the same time (and at the same rate) as the transmitter. The received signal is mixed with the receiver LO giving a signal with frequency components that are proportional to the propagation delays present on the channel (see Figure 9-3). Fourier analysis can be used to obtain the frequency of each tone and, given the known sweep rate, this can be translated into a delay. This process is repeated regularly during the sweep resulting in an ionogram (e.g. Figure 2-9).

Path delay resolutions of $\sim 7 \mu\text{s}$ are possible with modern sounders employing digital signal processing [Arthur, 11] since the time resolution is determined by the frequency range swept rather than the instantaneous bandwidth (as it would be in pulse sounding). Whilst mode structures can be visualised in detail it is not easily possible to determine the Doppler characteristic (shift/spread) of the received signals. Doppler characteristics may be investigated by using more sophisticated multiple sweeping techniques (e.g. [Poole, 172]).

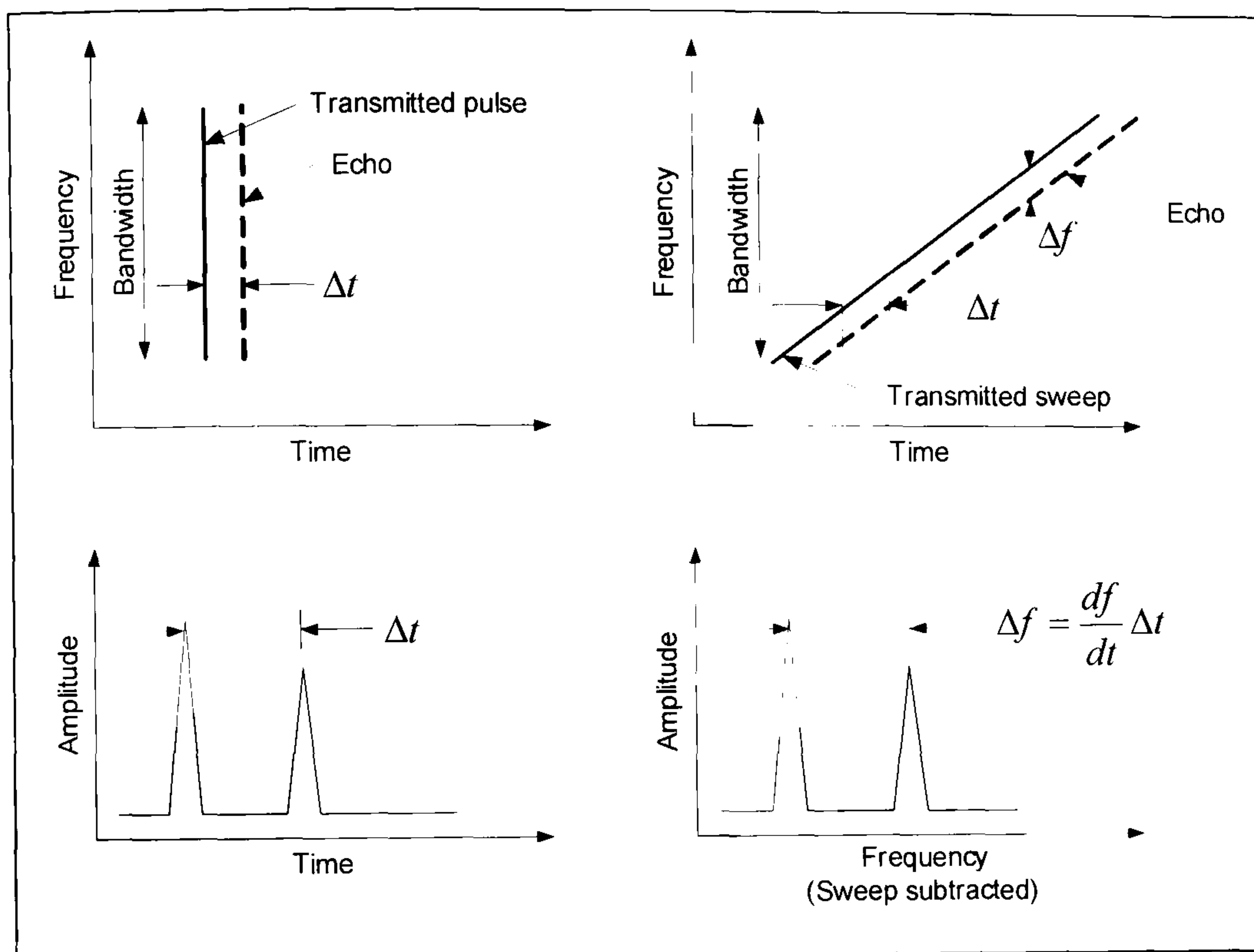


Figure 9-3 Comparison between Pulse and Chirp Sounding [Barry, 171]

9.2 Measuring the Time Varying Complex Channel Impulse Response (CIR)

Following Bello [Bello, 166] the signal, $r(t)$, received via a communications channel, such as the HF channel, with a finite impulse response (signal delay times between T_{L-} and T_{L+}) can be given by:

$$r(t) = \int_{T_{L-}}^{T_{L+}} h(\tau, t) s(t - \tau) d\tau + n(t) \quad (9-1)$$

where

$s(t)$ is the transmitted signal;

$h(\tau, t)$ is the impulse response of the channel as a function of delay time, τ , and

$n(t)$ represents the additive noise (assumed to be zero mean and variance σ_n^2).

Assuming the channel impulse response is essentially constant over the length of the transmitted signal, T_s , it can be shown that the received signal correlation function (RCF) is given by:

$$\phi_c(\tau) = \int_0^{T_s} r(t)s(\tau - t)dt = \int_0^{T_s} h(\tau)\phi_{ss}(\tau - t)dt + v(\tau) \quad (9-2)$$

where ϕ_{ss} is the autocorrelation function (ACF) of the transmitted signal and $v(\tau)$ is a modified noise term with zero mean and variance:

$$\sigma_v^2 = \int_0^{T_s} |s(\tau - t)|^2 \sigma_n^2 dt \quad (9-3)$$

If the transmitted signal is carefully chosen such that its ACF, ϕ_{ss} , is close to impulsive, the RCF, ϕ_c , is a good approximation of the channel impulse response, $h(\tau)$.

By making repeated measurements of the channel impulse response, spaced by Δt seconds, it is possible to obtain $\phi_c(\tau, \Delta t)$, which is a stepped time measure of the channel's complex impulse response. This can be analysed to investigate the time varying nature of the channel's propagation modes at any value of τ . By taking the Fourier transform of $\phi_c(\tau, \Delta t)$ at each delay time we can obtain the channel scattering function, $S(\tau, \lambda)$:

$$S(\tau, \lambda) = \int \phi_c(\tau, \Delta t)e^{-j2\pi\lambda\Delta t} d\Delta t \quad (9-4)$$

This is a measure of how the channel disperses a received impulse in both delay time (multipath, delay spread) and frequency (Doppler shift and Doppler spread). The resulting scattering function can be integrated in either frequency or delay time to obtain the channel delay power profile, $\phi_c(\tau)$, or the channel Doppler power spectrum, $S(\lambda)$, respectively:

$$\phi_c(\tau) = \int |S(\tau, \lambda)|^2 d\lambda \quad (9-5)$$

$$S(\lambda) = \int |S(\tau, \lambda)|^2 d\tau \quad (9-6)$$

9.3 Implementation of WHISPER – A Wideband HF Channel Sounder

9.3.1 General Configuration

WHISPER is a high performance, low power, pulse compression sounder. It makes use of low power coded transmissions between remote transmit and receive sites to make measurements of the oblique wideband HF radio channel, on a pre-selected range of frequencies. By repetitively measuring the channel's CIR, the instrument can be used to study features including:

- Signal time of flight;
 - Number of distinct propagation modes present;
 - Mode time dispersion;
 - Mode frequency dispersion (Doppler spread) and Doppler shift;
 - Phase stability and fading statistics within modes; and
 - Absolute signal powers.
- During quiescent periods the system can also collect data that can be used to measure noise and interference.

WHISPER makes measurements of the channel using pulse compression sounding waveforms to increase the total energy available at the receiver whilst maintaining the time resolution that could be obtained for single pulses (equivalent to the compressed pulse width). The time resolution achieved is determined by the selected system bandwidth and the waveforms in use. Bandwidths between 1 kHz and 1.9 MHz may be selected.

WHISPER is implemented on a standard personal computer (PC) which hosts a wideband digital transceiver PCI card (see Chapter 7). This provides a digital signal processing (DSP) engine for waveform generation and processing as well as a high dynamic range wideband transmitter exciter and receiver. High accuracy system timing is provided by an external satellite global positioning system (GPS) receiver. This ensures that transmit and receive stations are accurately synchronised, thus allowing absolute signal time of flight measurements to be made. The configuration of the

receive system is shown in Figure 9-4 (the transmit system is identical but for the inclusion of a power amplifier).

In order to provide a high degree of flexibility the sounding waveforms are specified within text files, known as waveform control files (WCFs). This allows all the waveform characteristics (e.g. type, duration, modulation format, bandwidth, pulse repetition frequency (PRF), sequences in use, number of pulses etc) to be tailored to the required measurement. For greatest flexibility waveforms are generally described in complex baseband format.

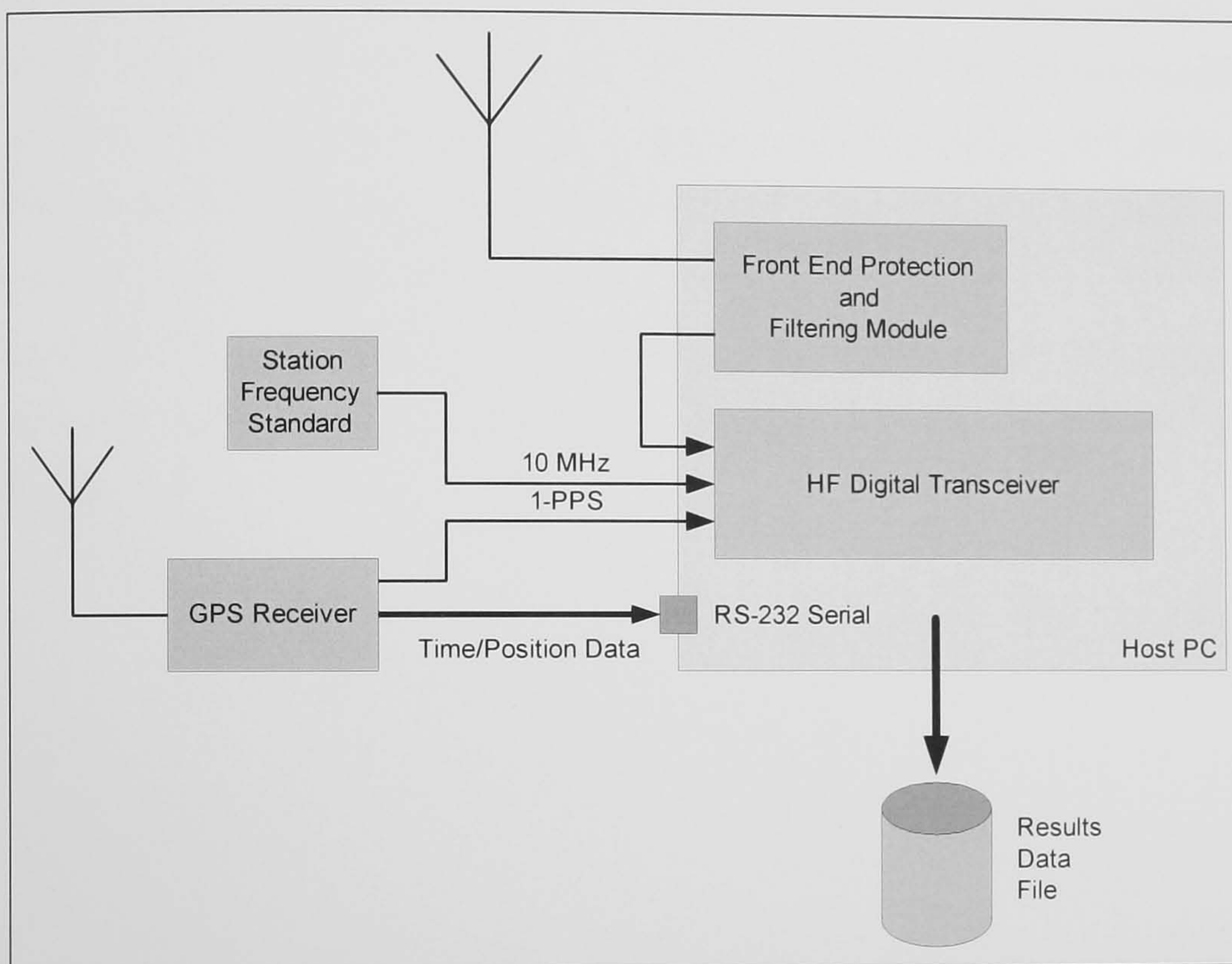


Figure 9-4 Configuration of WHISPER Receive System

9.3.2 Implementation of Sounder Application Software

The WHISPER sounder has been implemented as a software application using the digital transceiver platform. It uses the event based processing architecture introduced in Chapter 8. The following description relates to the operation of the sounder receiver but the transmitter is very similar (if not somewhat simpler). To provide maximum flexibility for measurement analysis the receiver captures complex data samples and streams them to a disk file unprocessed.

The user configures the sounder prior to starting a measurement. Parameters such as the required frequency and bandwidth are set as the user changes them on the GUI. When

the user starts a measurement (see Figure 9-5). the message *USR_MSG_START_RX_SAMPLES* is sent to the digital transceiver. This message is processed by the designated SHARC processor which configures a data flow from the DDC channel to be used, via a SHARC link port (which one is known *a priori*), to internal processor memory. This is done using a two dimensional chained circular SHARC DMA which fills a series of memory buffers in turn and then wraps around and starts filling the first buffer again. The DDC is programmed (by the host) to start supplying received complex data samples following a hardware trigger – the next GPS one pulse-per-second (1PPS) signal (which ensures an absolute time reference for the stored data samples). Once this trigger occurs data starts flowing automatically. Each time an input buffer is full an interrupt is triggered and the digital transceiver sends a *MSG_RX_SAMPLES* message to the host with the filled buffer as its payload. This process continues automatically streaming data until the user ends the measurement¹. The message *USR_MSG_STOP_RX_SAMPLES* simply stops the SHARC DMA engine and hence the data flow automatically stops once any outstanding buffers have been transferred.

¹ It is also technically possible for a buffer overrun to occur although the system is designed so that this does not normally occur. Overruns are trapped by marking buffers as 'pending' when they are queued to be sent to the host. If the same buffer is presented for transmission before it has been sent then an error is flagged.

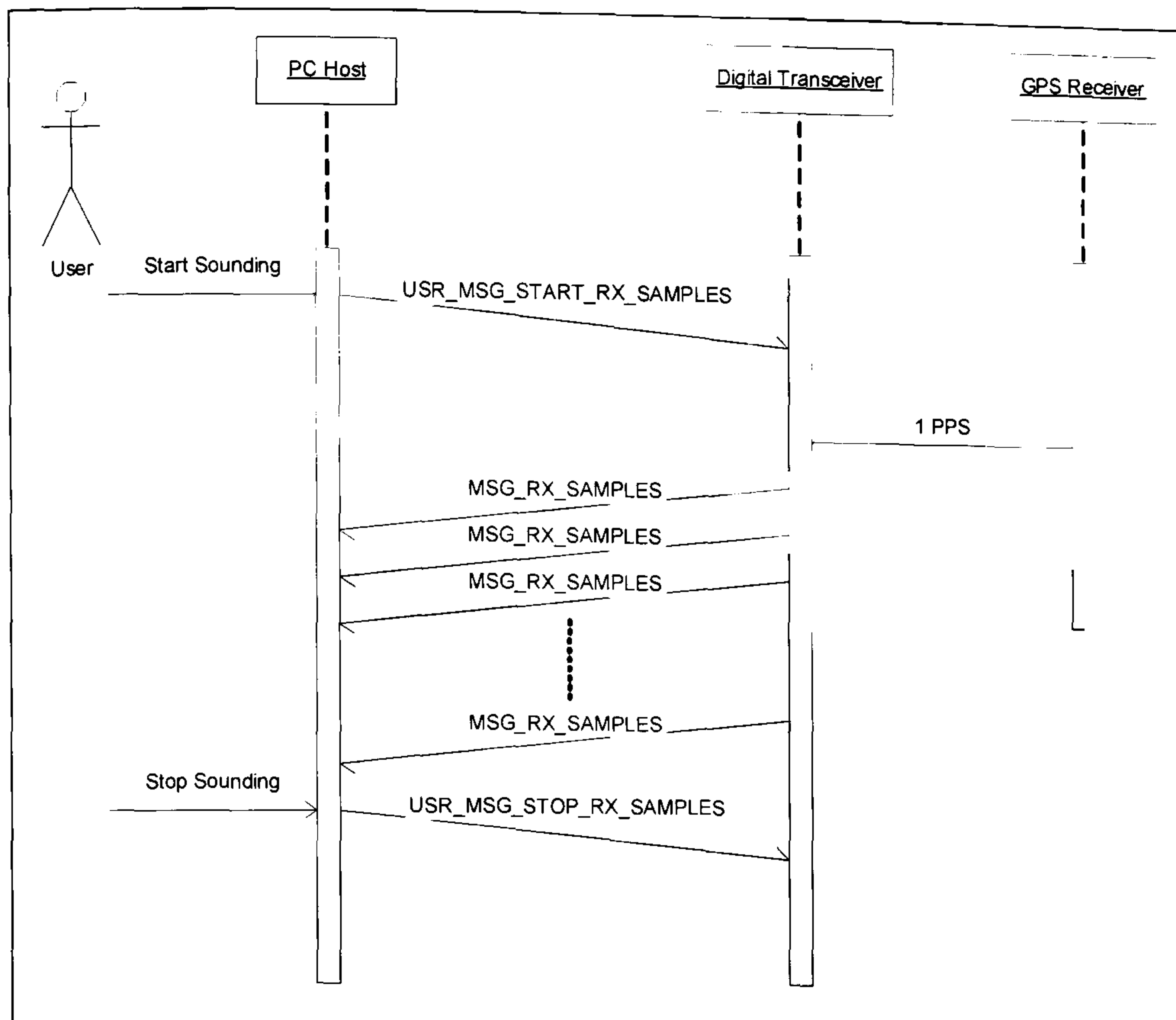


Figure 9-5 UML Sequence Diagram Illustrating Sounder Receiver

9.4 Pulse Compression Sounding Waveform Design

9.4.1 CIR Measurement - Range and Resolution

This section discusses how the CIR measurement parameters inter-relate and how they can be traded off to accommodate different measurement requirements. The maximum attainable timing resolution is determined by the system bandwidth, (typ. 80 kHz), which effectively limits the minimum pulse width through the system. The filtering applied to band-limit the transmitted sequence and control its time sidelobes has the unavoidable side effect of widening the compressed pulse. The useful instantaneous dynamic range of the sounder is limited by the peak-sidelobe ratio of the sounding sequences in use, including any additional degradation imposed by band-limiting and pass-band group delay variation etc. These limitations are highlighted in Figure 9-6. The delay range (multipath window) that can be investigated unambiguously can be no greater than the pulse repetition interval (PRI). Larger differential delays than the frame period will cause interference in subsequent frames as 'wrap-around' or time aliasing.

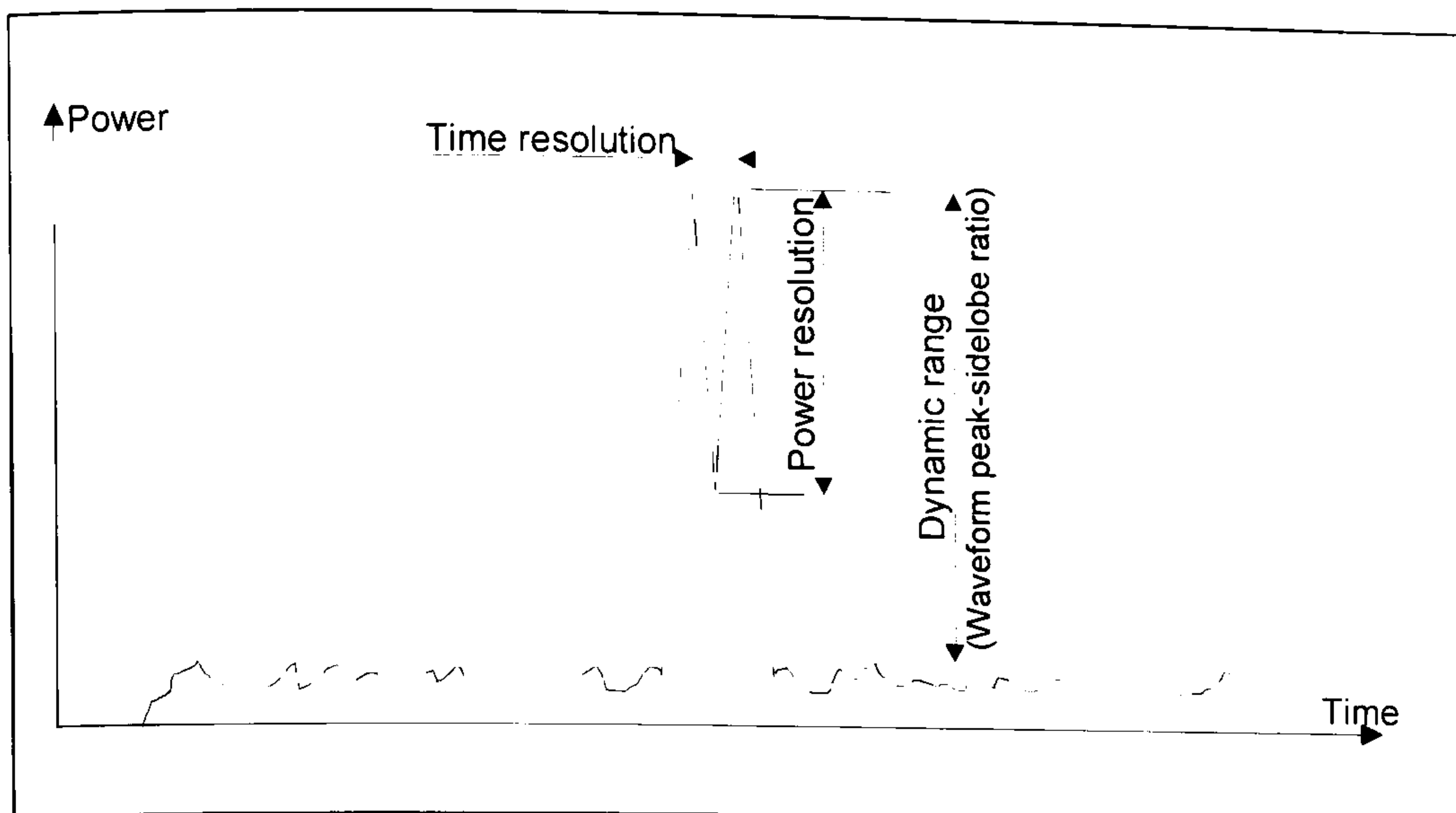


Figure 9-6 Pulse Compression Waveform Performance Metrics

The Doppler frequency range for a CIR measurement is also determined by the frame period; it is $\pm(\text{PRF}/2)$, the PRF being the reciprocal of the PRI. The presence of larger Doppler frequencies than this range will cause frequency aliasing that cannot be directly resolved. The unambiguous multipath (i.e. delay time) and Doppler ranges that can be measured simultaneously are, therefore, directly related.

The Doppler resolution of a measured channel scattering function is determined by the total measurement time. Where the required output of the CIR measurement mode is the channel scattering function, consideration must be given to the useful Doppler resolution that is actually obtained. It has been shown [Zuckerman, 173] that in order to measure the spectral content of a stationary random process, in our case a nominally Gaussian fading channel, with a given frequency resolution accuracy (i.e. to obtain a chosen degree of statistical stability in the results) the measurement time must significantly exceed the minimum time required to make a single observation. This can be resolved by averaging a number of scattering function measurements (incoherent integration). Unfortunately, no signal processing gain is realised and all phase information is lost. Alternatively the measurement time can be significantly increased which increases the number of frequency bins in each Fourier transform. Contiguous bins can be averaged to reduce the data to the useful Doppler resolution.

The CIR measurement processing gain over a single pulse channel estimate, for a general pulse compression waveform, is approximately given by:

$$PG(\text{dB}) = 10 \log_{10} (N_{SEQ} \times \text{Frames}) \quad (9-7)$$

where

N_{SEQ} is the number of symbols in the waveform; and

$Frames$ is the number of CIRs processed.

In frequency dispersive channels the achieved processing gain will reduce as a function of Doppler shift as coherence is reduced across the waveform length.

9.4.2 Requirements for Wideband Mid-Latitude Measurements

Before selecting a sounding waveform the basic measurement ranges and resolutions need to be established. The values in Table 9-1 have been chosen with a basic understanding of the HF paths to be investigated:

Parameter	Value
Transmission bandwidth	80 kHz
Multipath range	15 ms
Delay Time Resolution	<30 us
Useful Doppler Range	±10 Hz
Doppler Resolution	Determined by measurement length
Dynamic Range	>40 dB

Table 9-1 – Required CIR Measurement Performance

9.4.3 Design of Wideband Sounding Waveform

The principal pulse compression sounding waveforms that have been used in WHISPER are bi-phase shift keyed (BPSK) modulated maximal length pseudo noise sequences (PN-sequences). These exist for all sequence lengths 2^m-1 ($m>1, m\in\mathbf{N}$). These codes have the special property that when they are correlated cyclically, their correlation peak is equal to the sequence length (2^m-1) and the side-lobes are all -1 (see Figure 9-7), giving a useful nominal dynamic range of $20\log(2^m-2)$ dB. Binary PN-sequences may be generated economically using a clocked shift register with a number of feedback taps [Skolnik, 160].

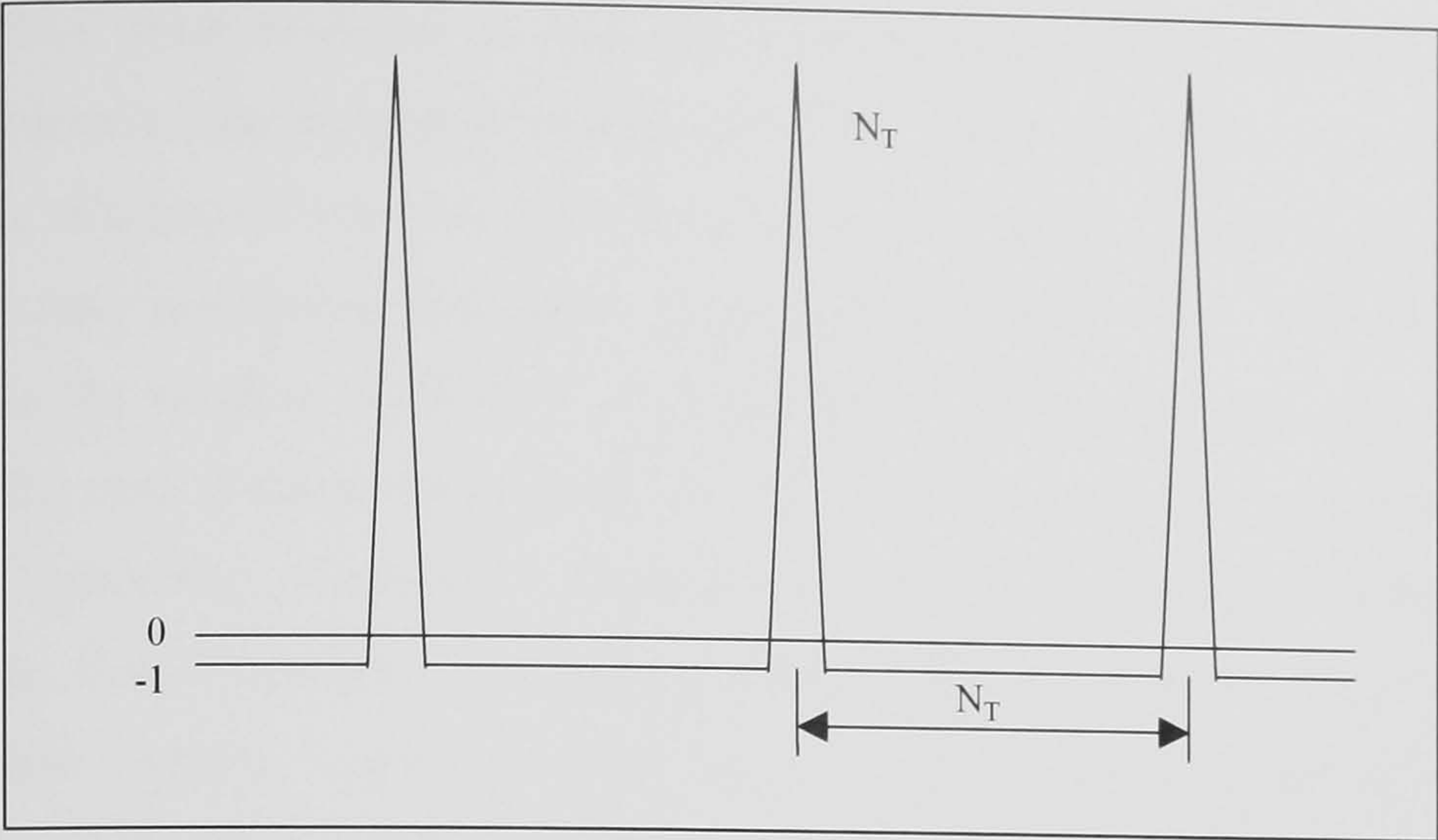


Figure 9-7 N_T Chip PN-Sequence Periodic Autocorrelation Function

Transmitting them back-to-back is also useful in that it allows a 100% transmit duty cycle, maximising signal power (some codes require gaps between sequences equal to the sequence length to preserve their good correlation properties). Given the bandwidths and delay time ranges of interest PN-sequences of lengths 511 and 1023 are appropriate. BPSK was chosen for a number of reasons. It is simply implemented at complex baseband in both transmitter and receiver, provides the maximum ‘distance’ between different symbols (thus providing good performance in the presence of Doppler and amplitude perturbations) and it is a nominally constant envelope signalling scheme which maximises the transmitted signal power. Table 9-2 summarises the structure and characteristics of a number of sounding waveforms (including one variant compatible with the narrowband DAMSON sounder for comparison). In each case the chip rate is ~80% of the sounding bandwidth.

Waveform (BPSK)	Chip-rate (kchip/s)	Delay Range (ms)	Multipath Resolution (μ s)	Doppler Range (Hz)	No. of CIRs	Doppler Resolution (Hz)	Measure Time (s)	Processing Gain (peak, dB)
PN-1023	81	12.6	~10	± 40	8192	0.01	103	70
PN-1023	61.4	16.6	~15	± 30	8192	0.008	136	70
PN-511	40.8	12.5	~35	± 40	8192	0.01	102	67
Barker-13	2.4	12.5	~600	± 40	128	0.6	1.6	32

Table 9-2 Characteristics of Various WHISPER Sounding Waveforms

If a digital sequence is transmitted with no pulse shaping through a band-limited channel such as a radio system the steep filter edges will cause ringing in the time domain. This is observed as inter-symbol interference on the received signal which in turn results in poor peak-sidelobe performance. This is overcome by using a pulse

shaping filter which is chosen to both maximise the obtainable peak-to-sidelobe ratio and yet minimise the inevitable broadening of the correlation peak. This problem is akin to the selection of windows for spectral analysis using the Fourier transform and, in fact, the same windowing functions are applicable [Harris, 175]. However, in this application the window coefficients must be used as the coefficients in a transversal filter. The time domain windowing function was selected after simulation of the sequence generation, transceiver band-defining filters and signal detection signal processing. For this purpose the digital transceiver filters, which are a combination of digital finite impulse response (FIR) and cascaded integrator-comb (CIC) filters [Hogenaur, 115], were modelled using a high order FIR filter with the appropriate cut-off frequency (Figure 9-8).

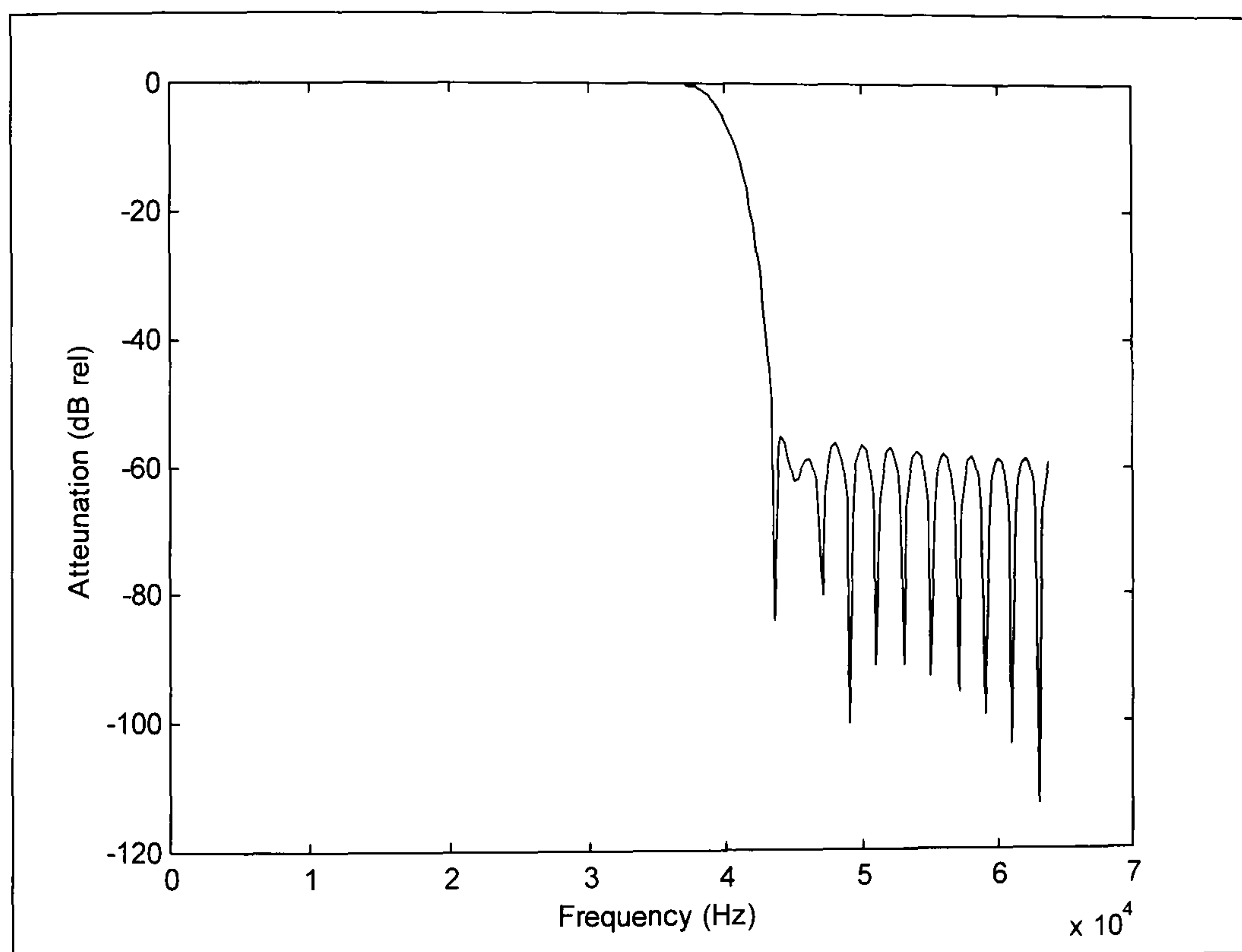


Figure 9-8 Simulated Radio Filters (80 kHz Complex Baseband)

A number of standard window functions were synthesised and the resulting performance examined. Figure 9-9 shows the simulation output for a PN1023 sounding waveform with no pulse shaping (rectangular window), with a Gaussian window, and with a 5-tap, 50 dB Chebychev window. It was concluded that the five tap FIR filter 50 dB Dolph-Chebychev window coefficients gave acceptable delay time sidelobes. An alternative approach to using fixed pulse shaping is to use a transversal equaliser to minimise the error between the transmitted signal and that received in a back-to-back calibration. The formulation is shown in Appendix F.

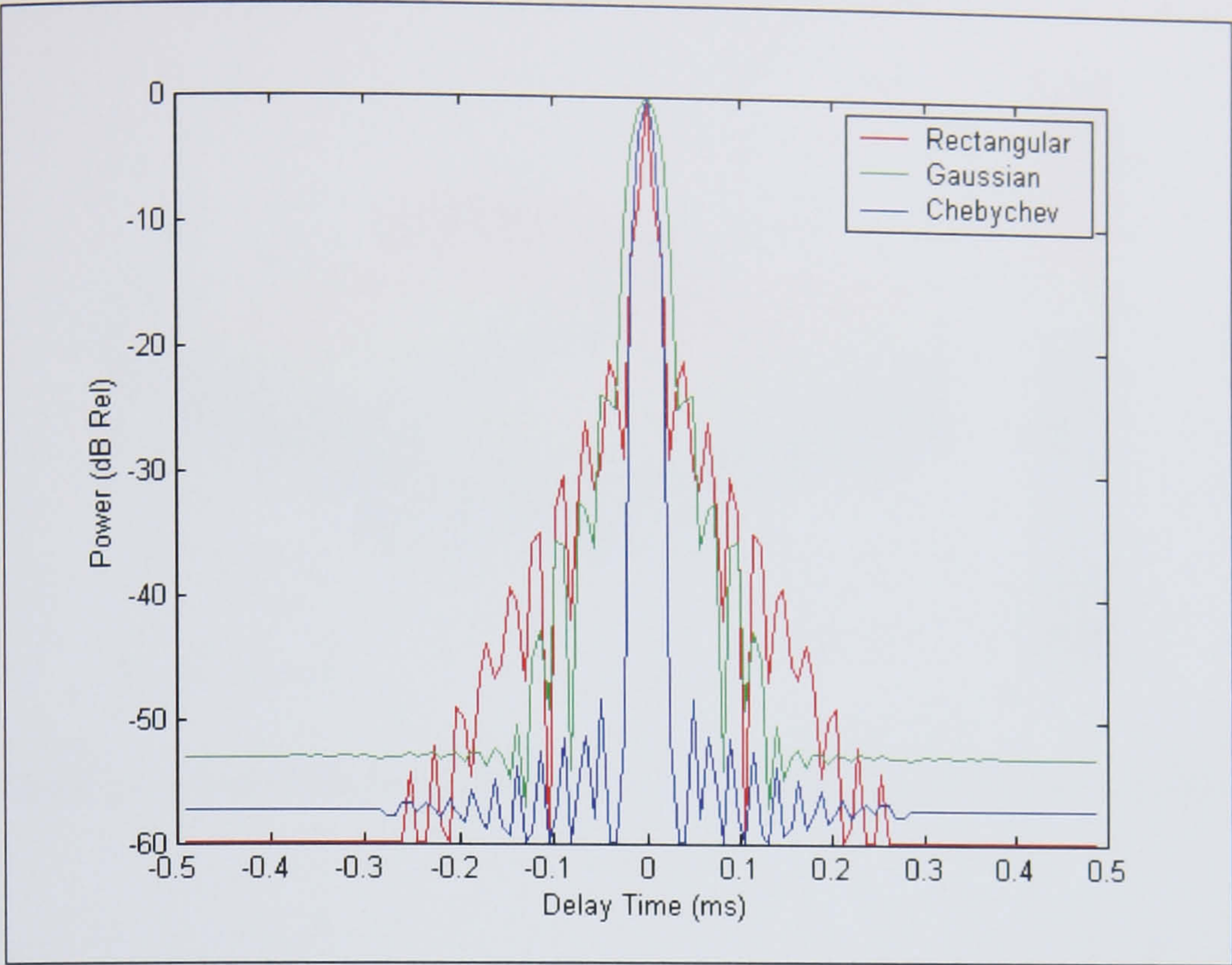


Figure 9-9 64 kchip/s PN-1023 Pulse Compression Waveform in 80 kHz Channel

As the sounding waveform is to be used to characterise a channel that is subject to both time and frequency perturbations it is necessary to ensure that the chosen sounding sequence will perform adequately over the expected operating range. This was verified by generating the signal’s correlation function with frequency shifted replicas at a specified delay time. A plot of the PN-1023 correlation function as a function of Doppler offset is presented in Figure 9-10 and Figure 9-11 (close in). These demonstrate how, as the Doppler frequency increases the correlation peak-to-sidelobe ratio, and to some extent the correlation peak, decreases. For Doppler offsets less than ± 10 Hz the peak to sidelobe ratio is adequate (always better than 45 dB) and the correlation peak is within 2 dB of its power under zero Doppler conditions (Figure 9-12). Scattering function measurements can easily be corrected for the decrease in correlation peak during post processing.

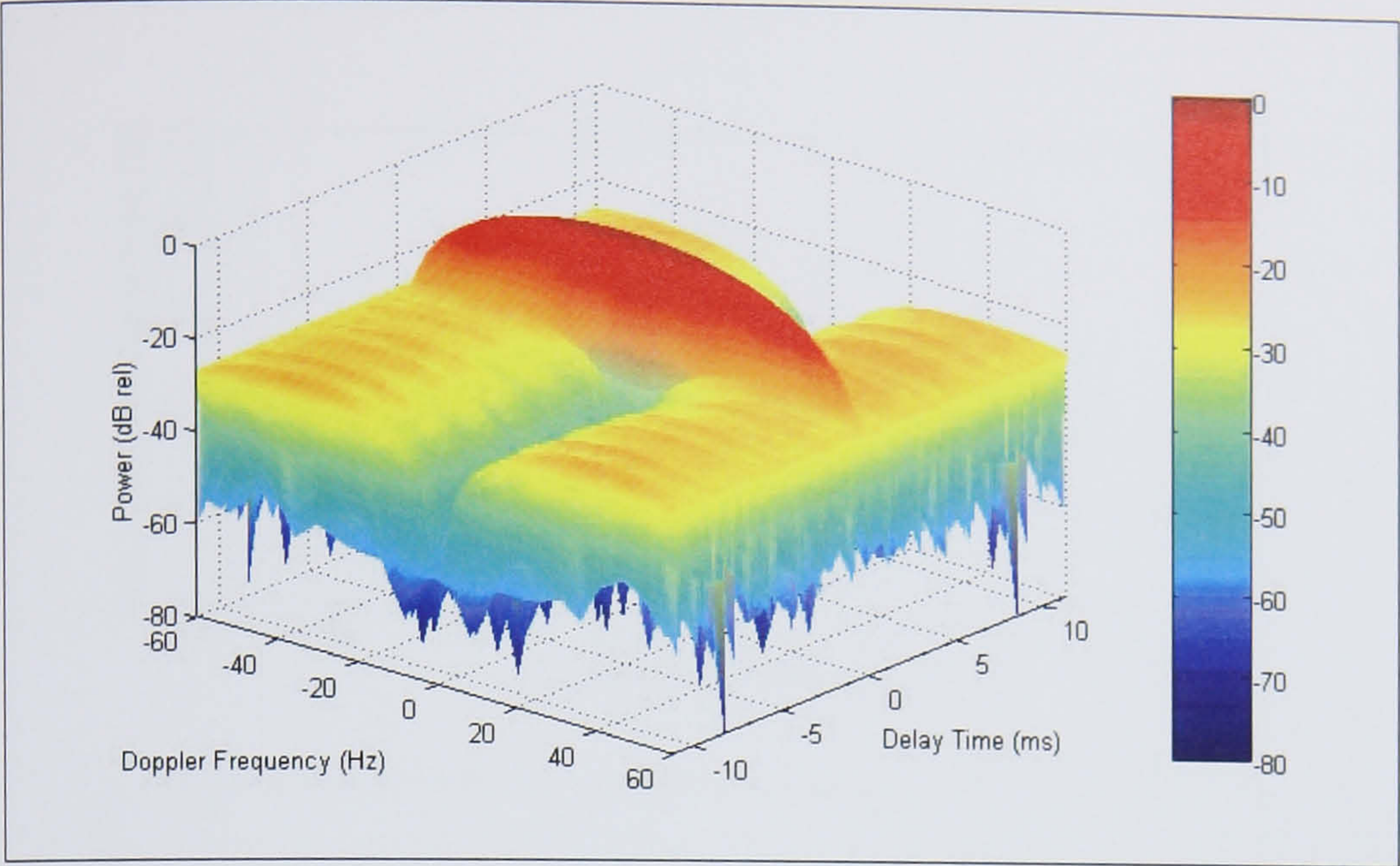


Figure 9-10 Band-limited 64 kchip/s PN1023 Waveform CIR versus Doppler Offset

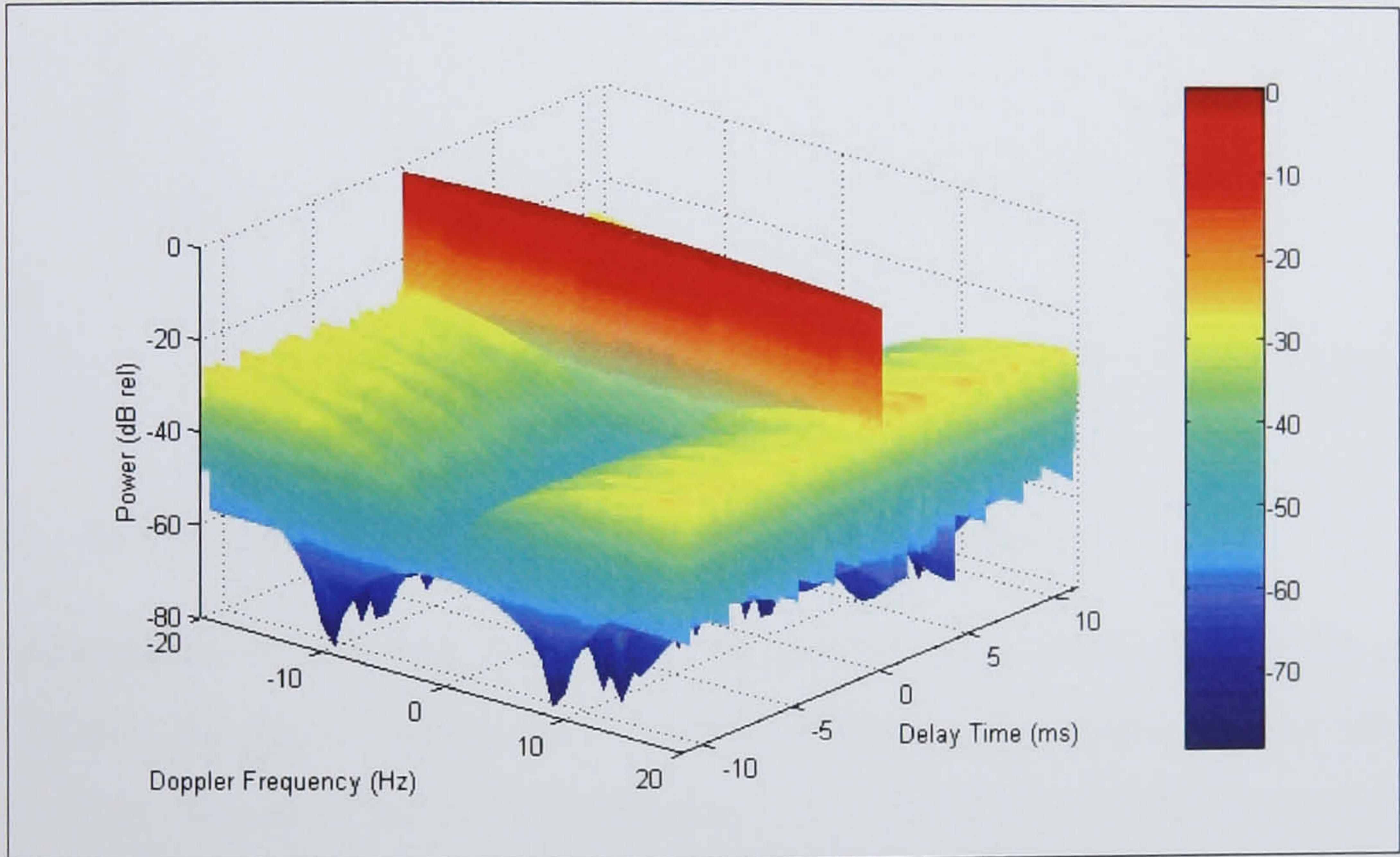


Figure 9-11 Band-limited 64 kchip/s PN1023 Waveform CIR versus Doppler Offset (close in)

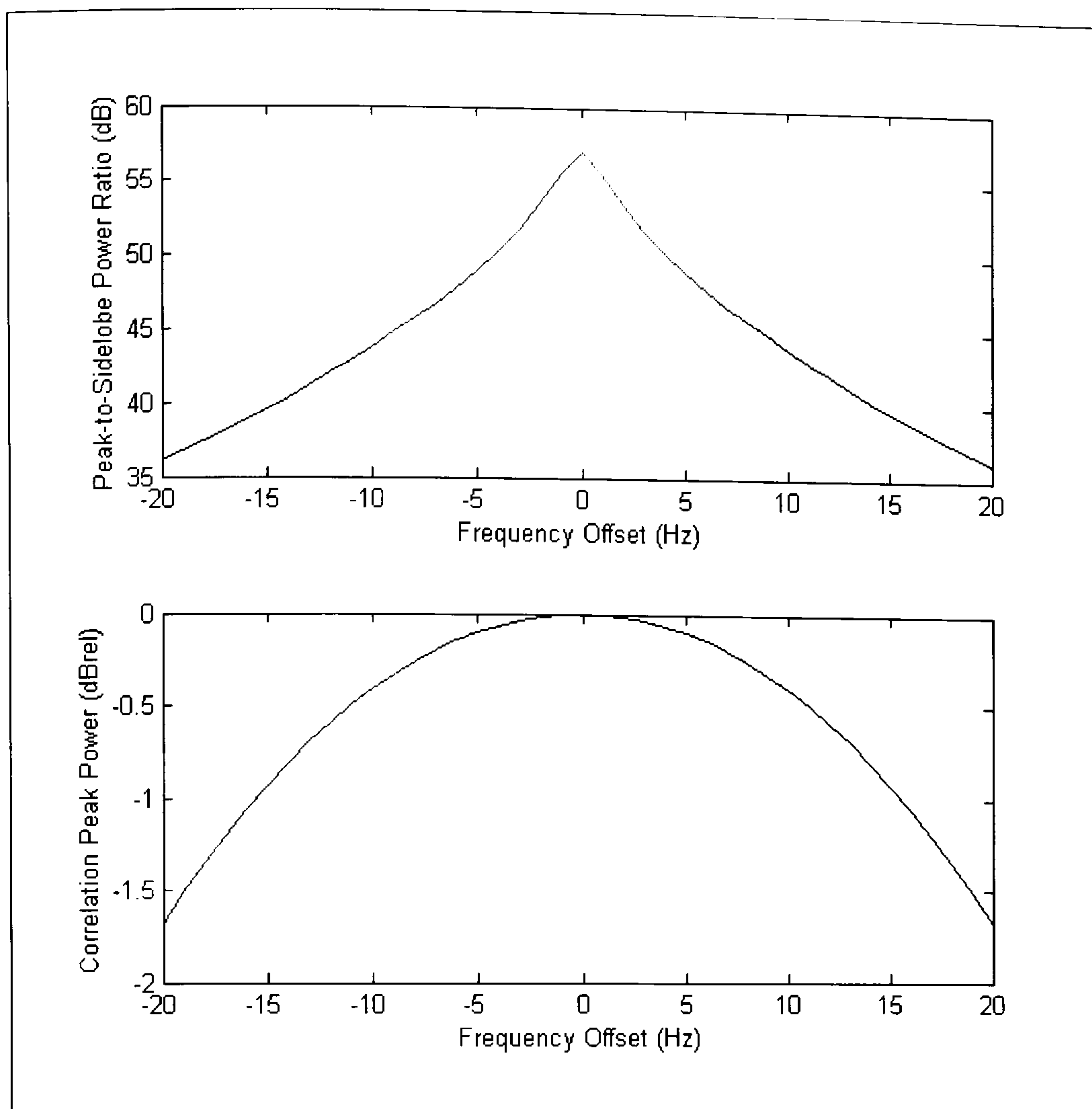


Figure 9-12 Performance of as a Function of Frequency Offset

9.4.4 Practical Waveform Implementation Issues

The sounding waveforms are designed to be implemented on the WHISPER sounder which utilises the digital transceiver platform. To generate a waveform description file the following additional steps are undertaken. A series of waveform transmit samples are obtained by generating three repeated waveforms (including all pulse shaping etc) and the centre section captured. This ensures that the transmitted waveform samples can be repeated without discontinuity to provide the ideal periodic correlation properties that gives good peak-sidelobe performance. For practical implementation reasons the waveforms are also re-sampled at design time to give a waveform length that is an exact integer sub-multiple of the digital transceiver clock frequency (62.208 MHz). This ensures that an exact integer decimation rate can be chosen for the receiver DDC and that there are an exact number of CIR measurements in a second which allows data collection at the receiver to be started on any second boundary (accurately synchronised using GPS). Table 9-3 details the measurement WCFs that have been implemented.

Waveform Filename	Chip rate (kchip/s)	Sequence Length	Sample Rate	Re-Sampled Length
'tx1023-81r'	81	1023	129,600	1620
'tx1023-64r'	64	1023	77,760	1296
'tx511-32r'	32	511	48,000	600
'barker-13'	2.4	13	2.4	13

Table 9-3 Implementation of WHISPER Sounding Waveforms

9.5 Receive Digital Signal Processing

Received signals are down-converted to complex baseband by the wideband digital receiver. To maximise flexibility the data is saved to disk as complex sample pairs at this stage. CIR measurements are calculated off-line by cross correlating the received signal against a template of the transmitted waveform. Initially a scattering function is generated from the first few seconds of data (256 CIRs) to allow the overall multipath and Doppler range of interest to be determined. Subsequently the entire measurement is processed to determine the sampled time, sampled delay CIRs, $\phi_c(\Delta\tau,\Delta t)$, over the delay range of interest (reducing the size of the data set by typically a factor of 2). This is windowed and FFT'ed to obtain the scattering function, $S(\Delta\tau,\Delta t)$, before Doppler filtering (removing all frequencies beyond that of the received signals) to improve the signal to noise ratio and further decrease the size of the data set. The decimated data may then be inverse FFT'ed to return to the time domain representation, $\phi_c(\Delta\tau,\Delta t)$.

9.5.1 Use of Windows in Calculating the Scattering Function

The scattering function is estimated by calculating the Fourier transform of a time series of CIR measurements at a specific delay time, τ . The Fourier transform is a periodic process over the series of samples transformed. If the series analysed is not periodic over this period unwanted sidelobes will be generated that may mask features of interest. Window functions can be used to force periodicity (by multiplying the series to be transformed by a function that tapers to zero at either end). The result of using a number of windows, with different characteristics [Harris, 175], in calculating the scattering function have been examined. The window utilised is a trade-off (principally) between the depth of the sideband suppression and broadening of the main lobe. Figure 9-13 shows the losses imparted by a number of different windows on a

periodic back-to-back measurement. Where data is presented in this thesis a Hanning window is utilised unless otherwise stated.

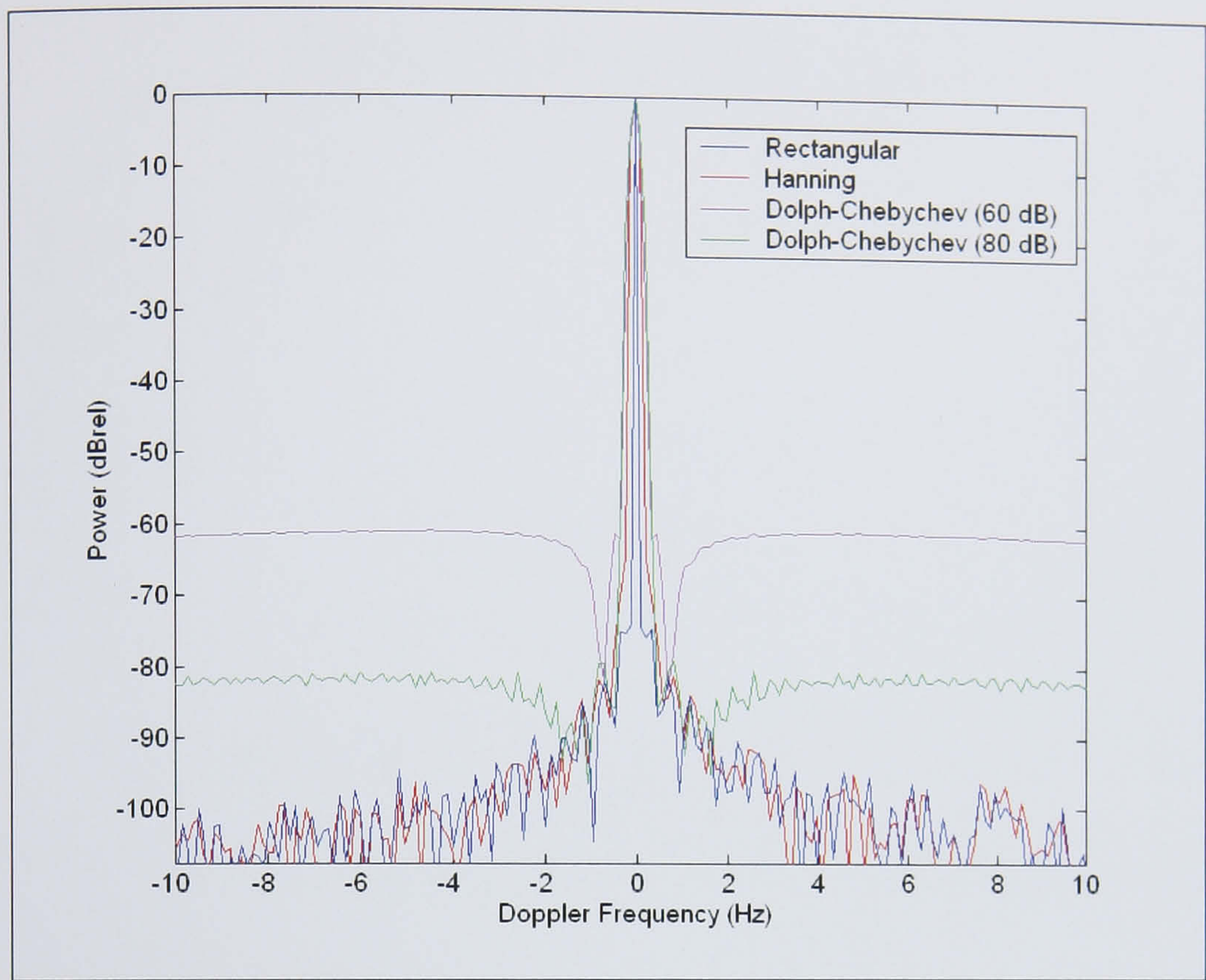


Figure 9-13 Use of Windows in Calculating the Scattering Function

9.6 Laboratory Measurements to Verify Sounder Performance

The WHISPER sounder transmitter and receiver system were connected in a back-to-back configuration via a variable attenuator in order to make some control measurements to verify the sounder’s performance. The results presented here are from measurements made using the *tx1023-64r* waveform (64 kchip/s PN-1023 sequence): Figure 9-14 shows the spectrum of the sounding waveform. Figure 9-15 is a plot of the back-to-back scattering function (effectively the ambiguity function). The sounding waveform time side-lobes can clearly be seen at -55 dBc as expected. The excellent dynamic range of the digital receiver can be witnessed across the rest of the surface where the instantaneous dynamic range is >90 dB (actually limited by the chosen plot floor rather than the instrument performance). Figure 9-16 shows the achieved time resolution of the sounder compared with the autocorrelation of the sounding sequence. It shows the time resolution that can be obtained from the sounder is better than 15 μs at -3 dB and ~30 us at -30 dB for this 64 kchip/s waveform in an 80 kHz bandwidth.

Figure 9-17 demonstrates the achieved Doppler performance of the sounder for 512 CIR measurements using a Hanning window.

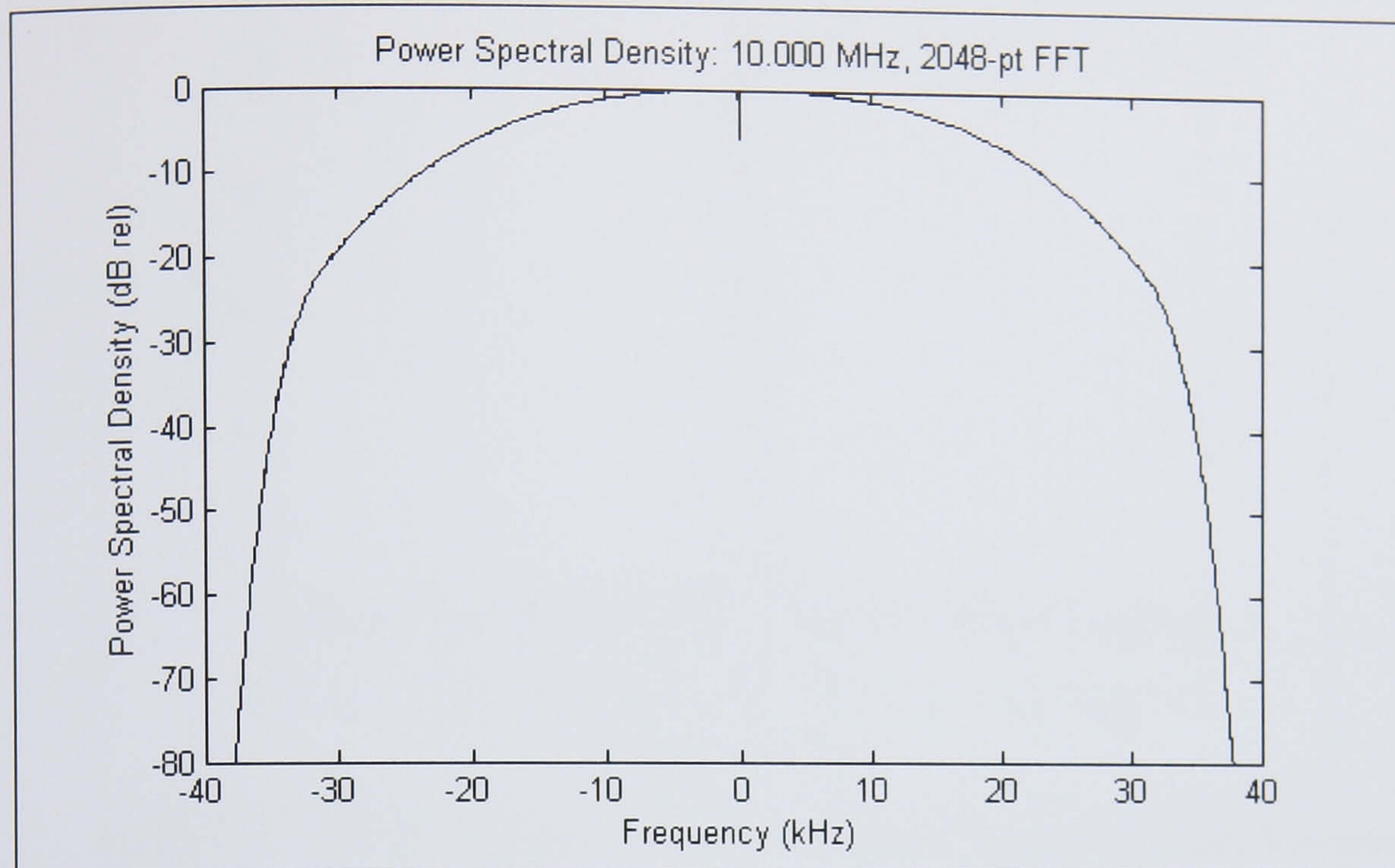


Figure 9-14 WHISPER Occupied Bandwidth (Waveform: tx1023-64r)

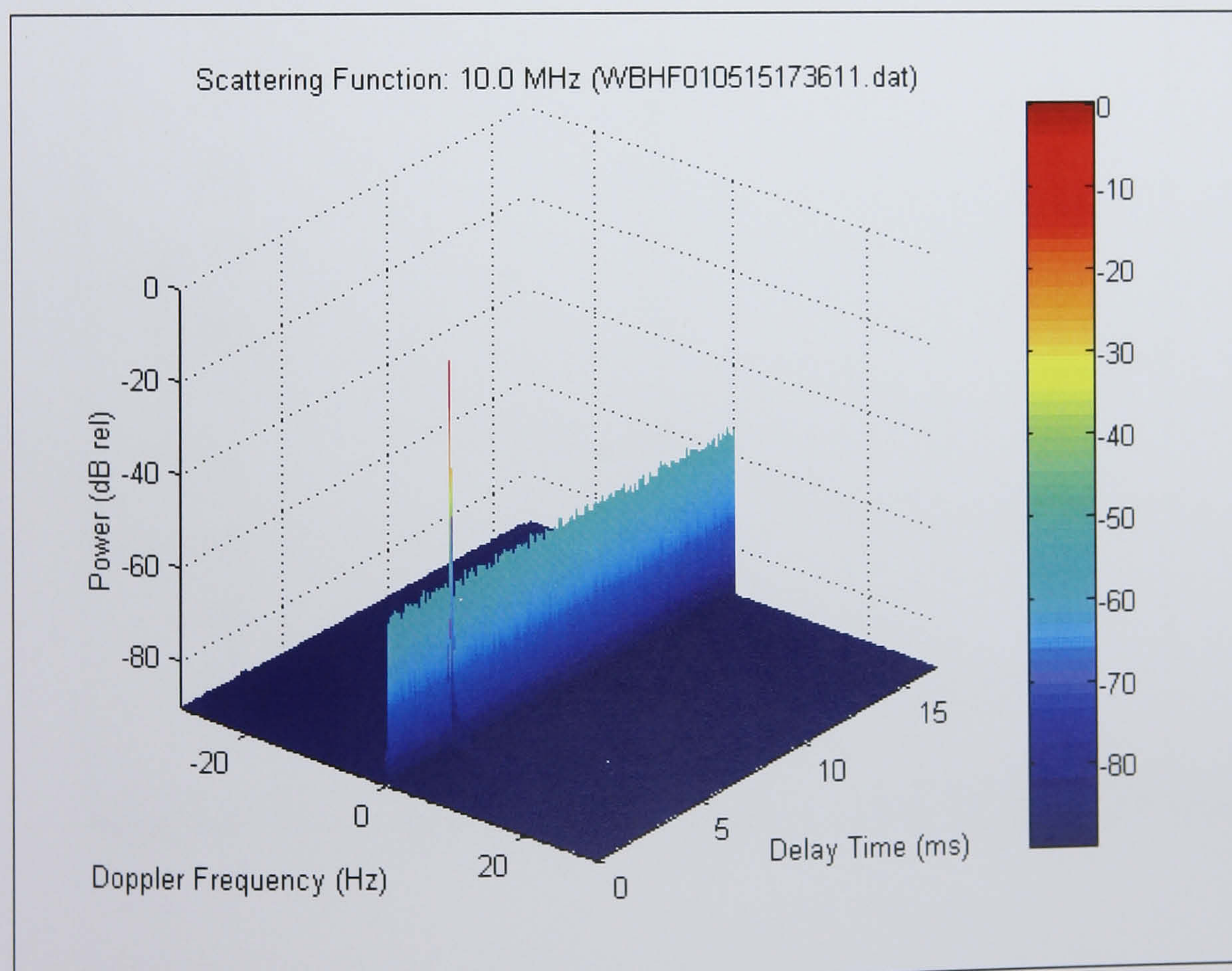


Figure 9-15 WHISPER Back-to-back Test: Measured Ambiguity Response

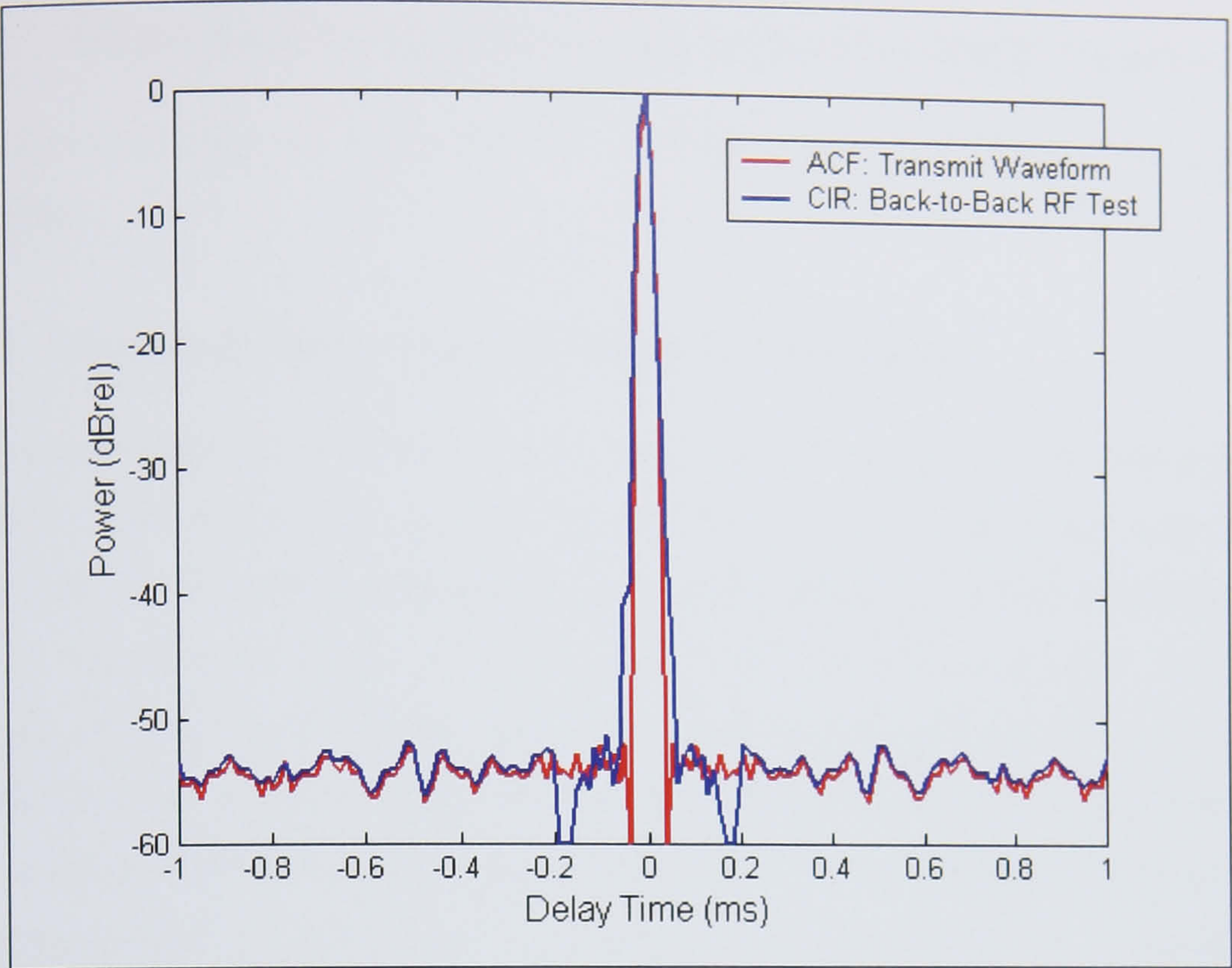


Figure 9-16 WHISPER Back-to-Back Test: Complex Impulse Response Resolution

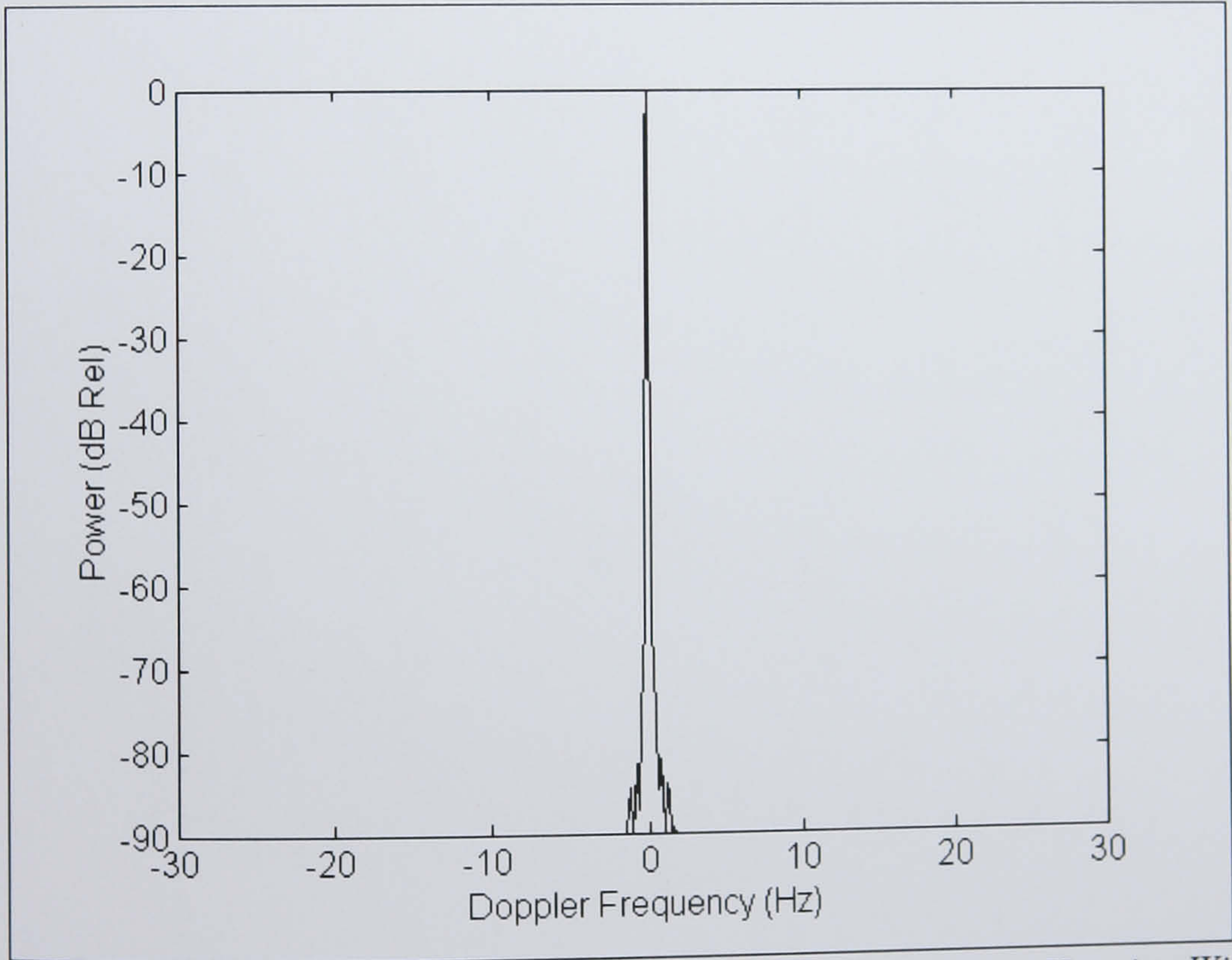


Figure 9-17 Back-to-Back Test: Doppler Resolution (512 CIRs, Hanning Window)

9.7 Suggestions for Improvements to the WHISPER Sounder

The following suggestions are made as to enhancements to WHISPER that would be beneficial.

9.7.1 Reduced Power Spectral Density Waveforms

The current sounding waveforms are cyclically repeated PN-sequences. However, this periodicity means that the power spectrum will be a comb with peaks spaced at the PRF (Figure 9-18). The wideband nature of this sounder means that it often has to operate as what is termed a secondary user (on a non-interference basis to other users). By applying a known pseudo random modulating code (to apply a 0° or 180° phase change to each sounding waveform repeat) it would be possible to spread the energy and reduce the waveforms power spectral density (PSD) further. Given good synchronisation and knowledge of the code, this is a process that is reversible at the receiver. A randomising code that repeated every 8192 PRIs could provide up to an additional 40 dB reduction in PSD.

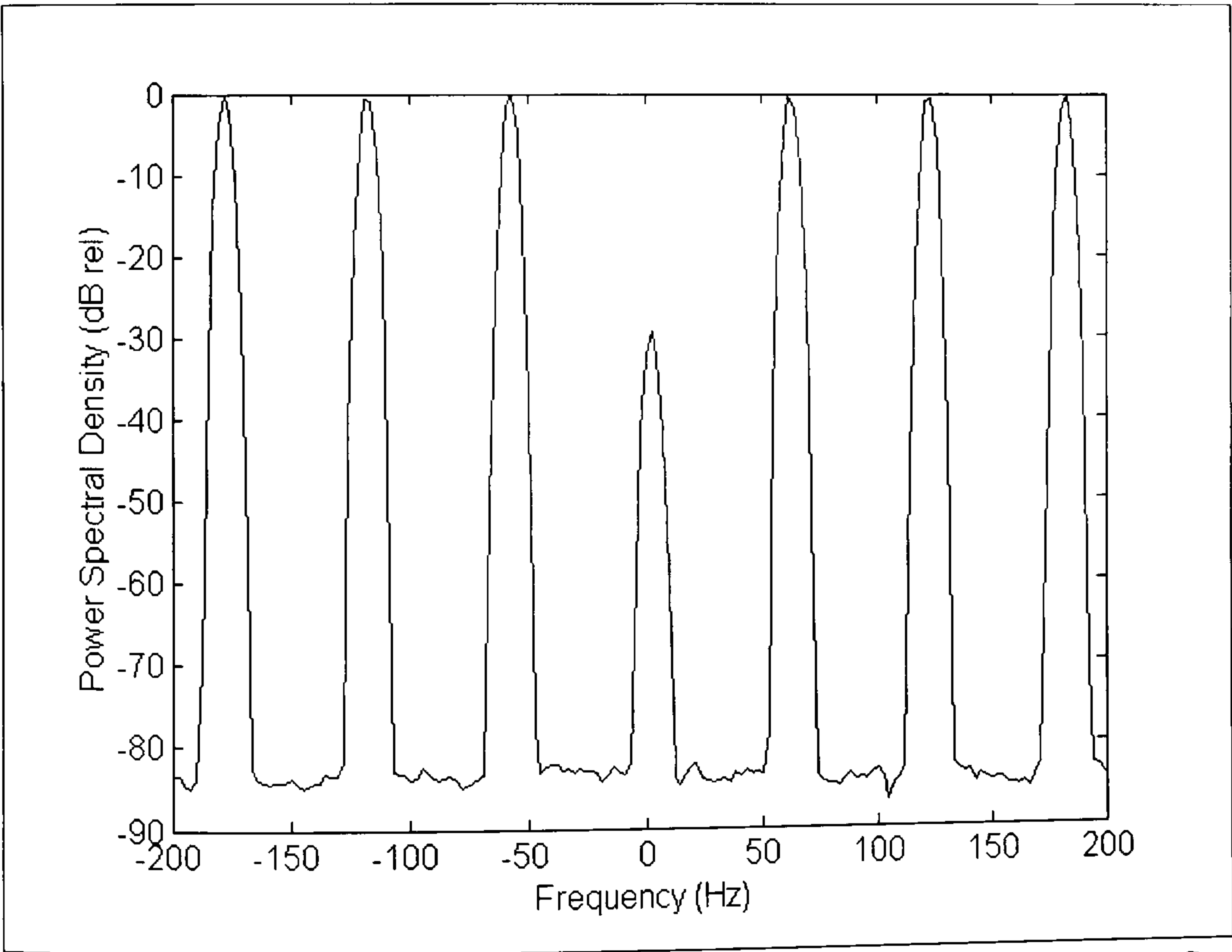


Figure 9-18 Centre of Measured 'tx1023-64r' Waveform Power Spectrum (PRF- 62.5 Hz)

9.7.2 Implementation of a Chirp Sounder Capability

When making HF channel measurements it is very useful to have access to real-time ionograms to allow interesting propagation conditions to be identified and investigated.

To increase the utility of the WHISPER sounder it would be possible to exploit the multi-channel nature of the digital transceiver platform to implement a second sounder that could operate in parallel with the primary pulse compression mode. In particular it would be particularly useful to implement a Chirp sounding function. The principal challenge would be implementing a sweeping LO. This could be done by implementing logic in the digital transceiver processing FPGA code in one of two ways. The DDC NCO could be programmed at a rate sufficiently high to cause it to appear to sweep coherently. Alternatively it would be possible for the FPGA to re-program the DDC NCO to step in frequency every N samples and then for a final stage complex frequency translation to be implemented in software after the DDC.

9.8 Chapter Summary

This chapter has documented the development of WHISPER, a new oblique HF ionospheric sounder capable of undertaking wideband measurements of the channel time varying complex impulse response. This is a low power pulse-compression sounder based on software radio techniques. It has been implemented as an application on the wideband HF digital transceiver described in Chapter 7. The design of sounding waveforms suitable for an investigation of wideband (~ 80 kHz) channel characteristics over mid-latitude Skywave propagation channels has been presented. Results of RF back-to-back measurements in the laboratory have confirmed the veracity of the sounder implementation and quantified its achieved performance. The next chapter presents results and analysis of wideband measurements made on a 170 km path in the UK during spring 2001.

Chapter 10.

Measurement of the Wideband HF Channel using WHISPER

Considerable effort has been expended in recent years to greatly increase HF data rates for beyond line of sight (BLOS) communications as the demand for improved throughput to support user applications grows. For the most part work has concentrated on increasing throughput in conventional narrow-band HF channels (e.g. [Jorgenson, 176]), but some researchers (e.g. [Elvy, 177]) have also investigated using much larger bandwidths. Further, whilst wideband HF propagation has been investigated previously (e.g. [Wagner, 178], [Vogler, 43]), there is still no accepted channel model that is able to describe both the large scale features (such as multiple modes, Doppler shift, Doppler spread, etc) and, significantly for modem designers, the detailed time varying properties of these channels such as inter- and intra- mode fading statistics [Sudworth, 179].

A new wideband HF sounder, known as WHISPER, developed specifically to investigate the fine structure of wideband HF channels was introduced in the previous chapter. This chapter details a series of wideband measurements made on a 170 km mid-latitude path using this sounder to verify its performance. A particular aim was to be able to investigate whether the Watterson [Watterson, 12] uncorrelated Raleigh fading model often used to represent narrowband (≤ 12 kHz) HF channels is applicable to wider bandwidth HF channels. Results from the analysis of the time varying channel CIR are given to demonstrate the ability of the sounder to make applicable measurements. This is done as three case studies.

10.1 Experiment Deployment

Initial channel sounding experiments were conducted over a 150 km, predominantly East-West, path from DERA Malvern to Cobbett Hill radio station in the UK during March and April 2001. At the Malvern transmit site the sounder utilised a linear RF power amplifier to provide ~ 100 W sounding transmissions which were fed into a 'droopy' loaded dipole antenna for transmission. The WHISPER receiver, located at the electrically quiet Cobbett Hill receive station, was fed from a wideband 2-8 MHz

dipole antenna. The initial sounding experiments collected continuous wideband data records of ~ 140 s duration (8192 complex impulse responses measured using a 61.4 kchip/s PN-1023 sequence) every five minutes during the day, dusk, night and dawn periods. Magnetic activity was low during the entire duration of the trial with the corrected sunspot number being ~ 200 (April campaign).

In order to provide collateral information and assist with frequency selection, a chirp sounder (2-16 MHz linear FM sweep) transmitter was also installed at Malvern. This shared the same power amplifier and antenna as the WHISPER transmitter. The chirp sounder was set to sweep once every five minutes with a transmit power of ~ 10 W. At Cobbett Hill an IRIS chirp receiver [Arthur, 180] processed the received signal to generate ionograms that were collected and displayed throughout the trials. The chirp transmitter and receiver were both synchronised to GPS time to allow absolute signal time-of-flight measurements to be made.

10.2 Results

10.2.1 Study Case 1: 10 April 2001 07:38 3.9 MHz

Figure 10-1 shows a scattering function measured on 10 April at 07:38 UT where three modes of decreasing amplitude are evident calculated from the first few seconds of data. Figure 10-2 is the scattering function measured over a 140 s following Doppler filtering to reduce noise and interference in the measurement (explained in section 9.5). A different representation of these data is given in Figure 10-4 (bottom left panel) where the original three modes are clear. Careful examination reveals an additional mode prior to these. This earlier weak mode is more evident in the delay power profile of Figure 10-4, which is a projection [Angling, 181] of the scattering function onto the delay-time axis. By reference to the corresponding IRIS chirp ionogram, the first three modes can be interpreted as 1E, 1F2 and 2F2 – the last mode is likely to be 3F2 but due to the lower processing gain of the IRIS ionosonde it is not visible on the ionogram. The operating frequency of 3.9 MHz lies slightly above the E region junction frequency and this probably accounts for the low signal amplitude of the 1E mode. The E region junction frequency estimate is based upon a measurement of f_oE at the Chilton vertical ionosonde, which is near the midpoint of the link, with due allowance for the path obliquity.

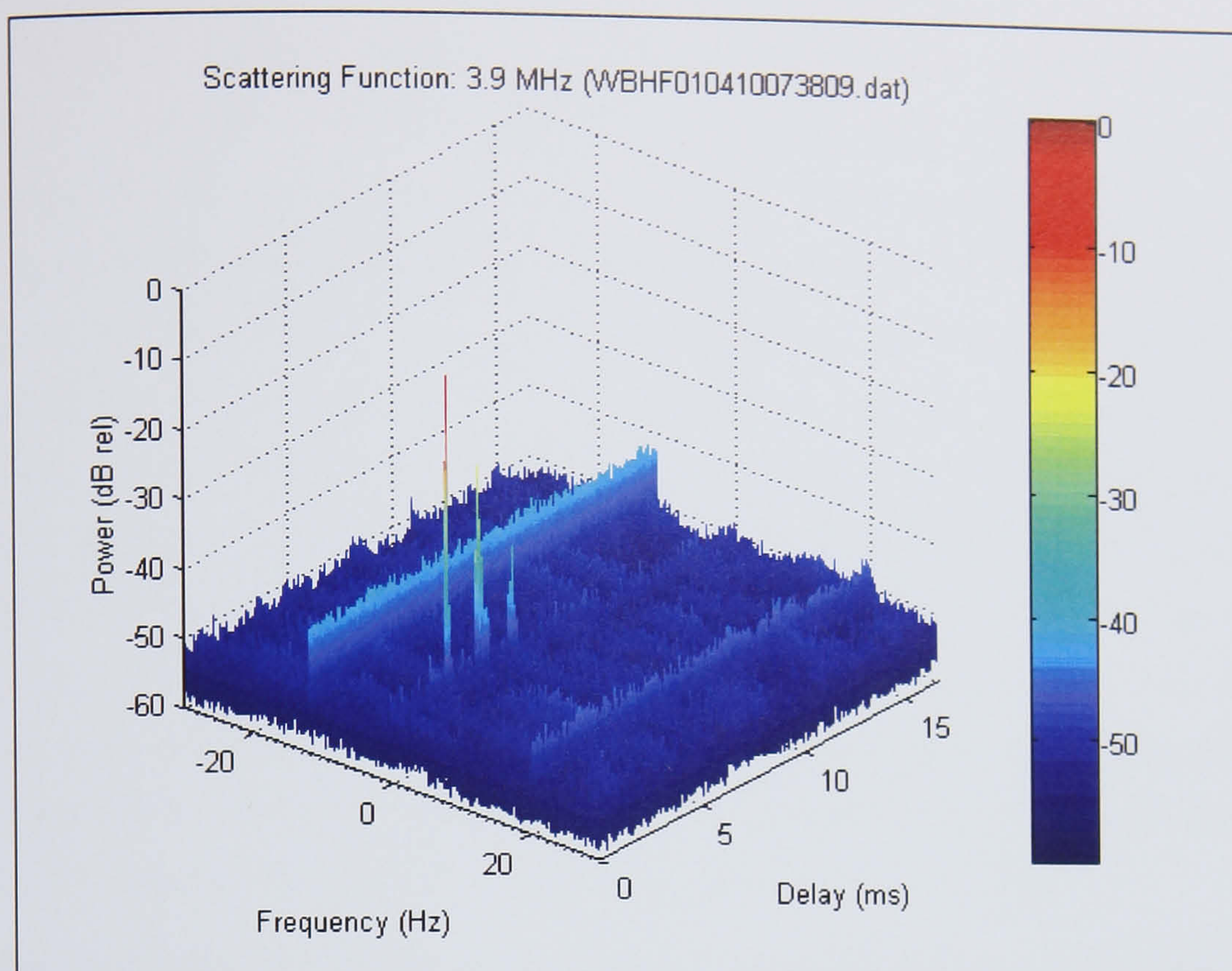


Figure 10-1 Measured Channel Scattering Function (3.9 MHz, 10 Apr 2001 07:38)

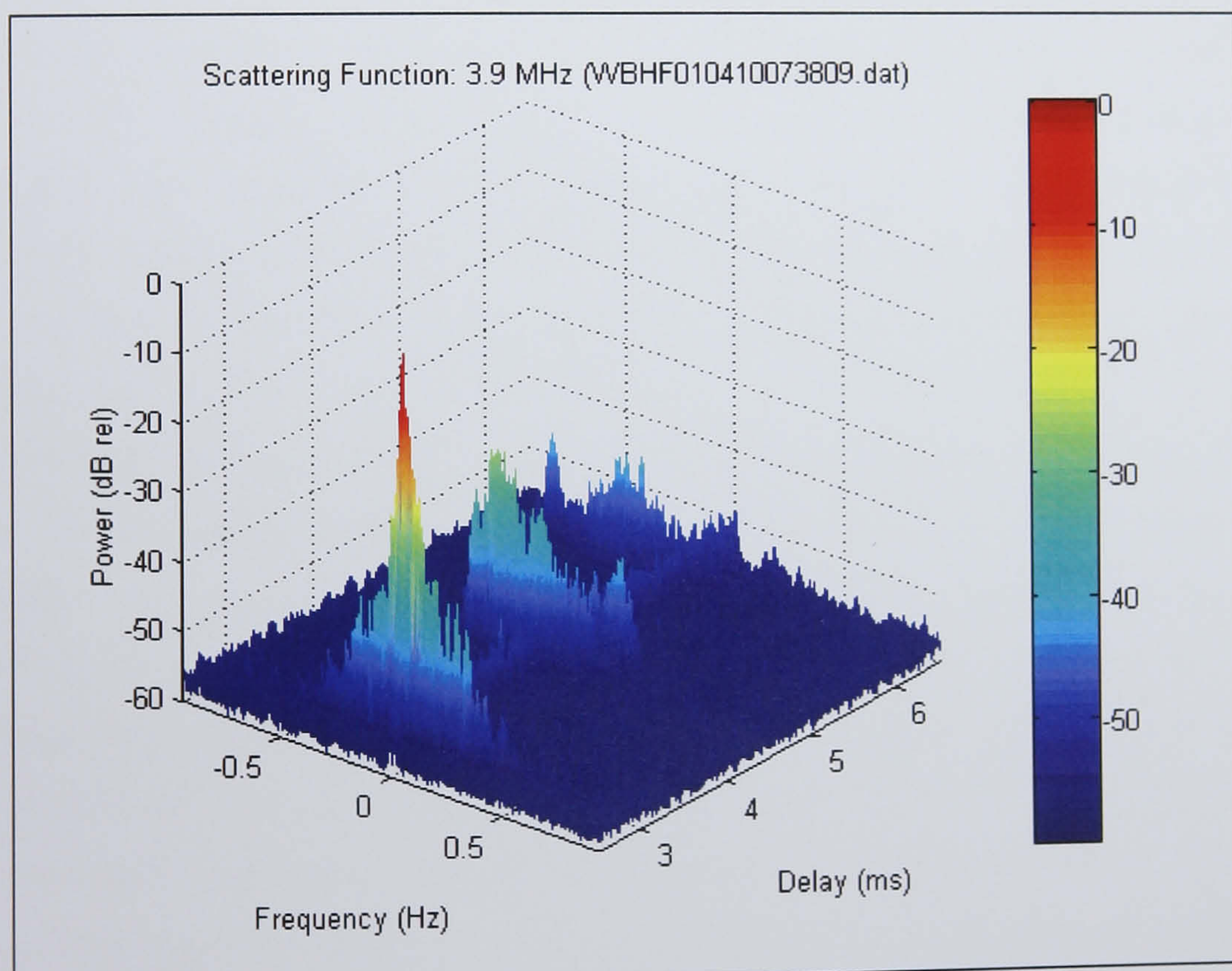


Figure 10-2 Measured Channel Scattering Function after Doppler Filtering (3.9 MHz 10 Apr 2001 07:38)

The scattering function of Figure 10-4 shows the 1F2 mode to be characterised by a fairly strong central component with almost no Doppler spread, surrounded by signals of much higher spread but also at a very low power. This signal would be expected to be highly coherent and other analyses bear this out. The 2F2 and 3F2 modes are much more diffuse both in time and frequency. Furthermore, the frequency shift increases between the 1F2, 2F2 and 3F2 modes. It should be noted that as yet it has not been possible to fully demonstrate that there is no frequency offset between the transmitter and the receiver. The frequency shift variation which is observed might be explained by a filling of the ionosphere as the solar zenith angle increases, or by an increase in reflection height. The 2F2 and 3F2 modes would be more sensitive to this than the 1F2 mode, since propagation would be more nearly vertical. Analysis of data from the evening shows an opposite Doppler trend which would support this hypothesis. This explanation should, however, be treated with some care at the moment.

Figure 10-5 to Figure 10-7 shows the channel power (left hand panel) and phase (right hand panel) for the 1F2, 2F2 and 3F2 modes over the 140 s measurement period as a function of delay time. The power plots are all plotted relative to the peak observed power in the channel (i.e. all the plots share the same scaling). The 1F2 mode shows a very slow, non-systematic variation in phase angle with time. This is consistent with the ~ 0 Hz Doppler seen in Figure 10-4. The first part of the signal return is essentially specular with no discernible time dispersion or fading due to the channel – the phase coherency over delay times from 2.65 ms to 2.72 ms (corresponding to around 5 measurement bins) being due to pulse shaping in the sounding waveform. This is followed by a much weaker decaying return which does exhibit much more phase volatility which appears to be Raleigh distributed. The 2F2 mode is, however, spread over a much wider time delay window. It shows a much faster (though reasonably regular) phase variation at both the leading and trailing edges of the mode, but the phasor is much noisier in the centre. It is possible that the trailing edge corresponds to the extraordinary (X) mode. Analysis of the 2F2 mode amplitude statistics suggests that it is all Rayleigh distributed, but given the limited signal to noise ratio it is difficult to make any conclusive statements. The phase plot also suggests that there is some structure giving a degree of delay time correlation across the mode but this requires further investigation in order to confirm it.

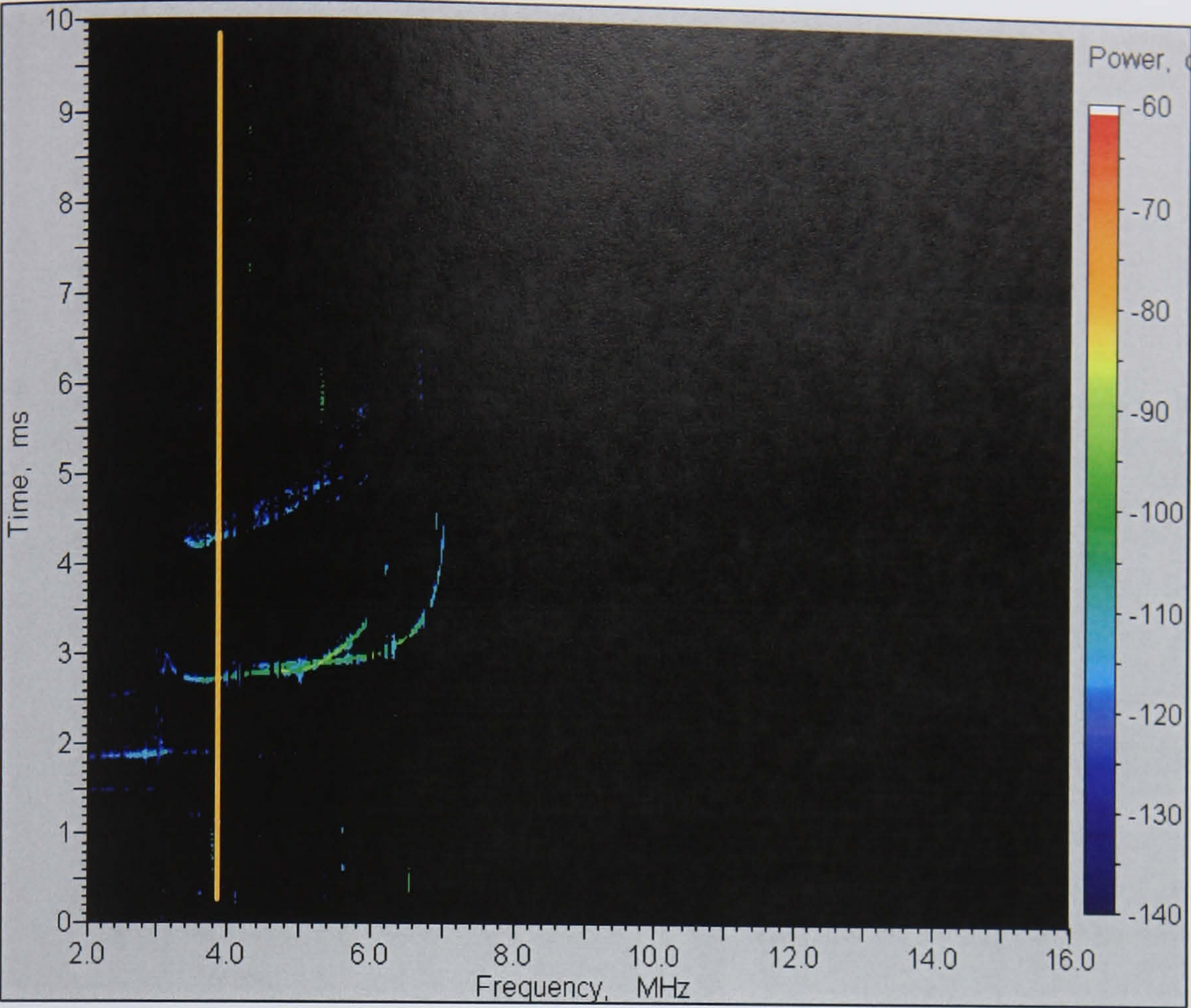


Figure 10-3 Oblique Ionogram (10 Apr 2001 07:38)

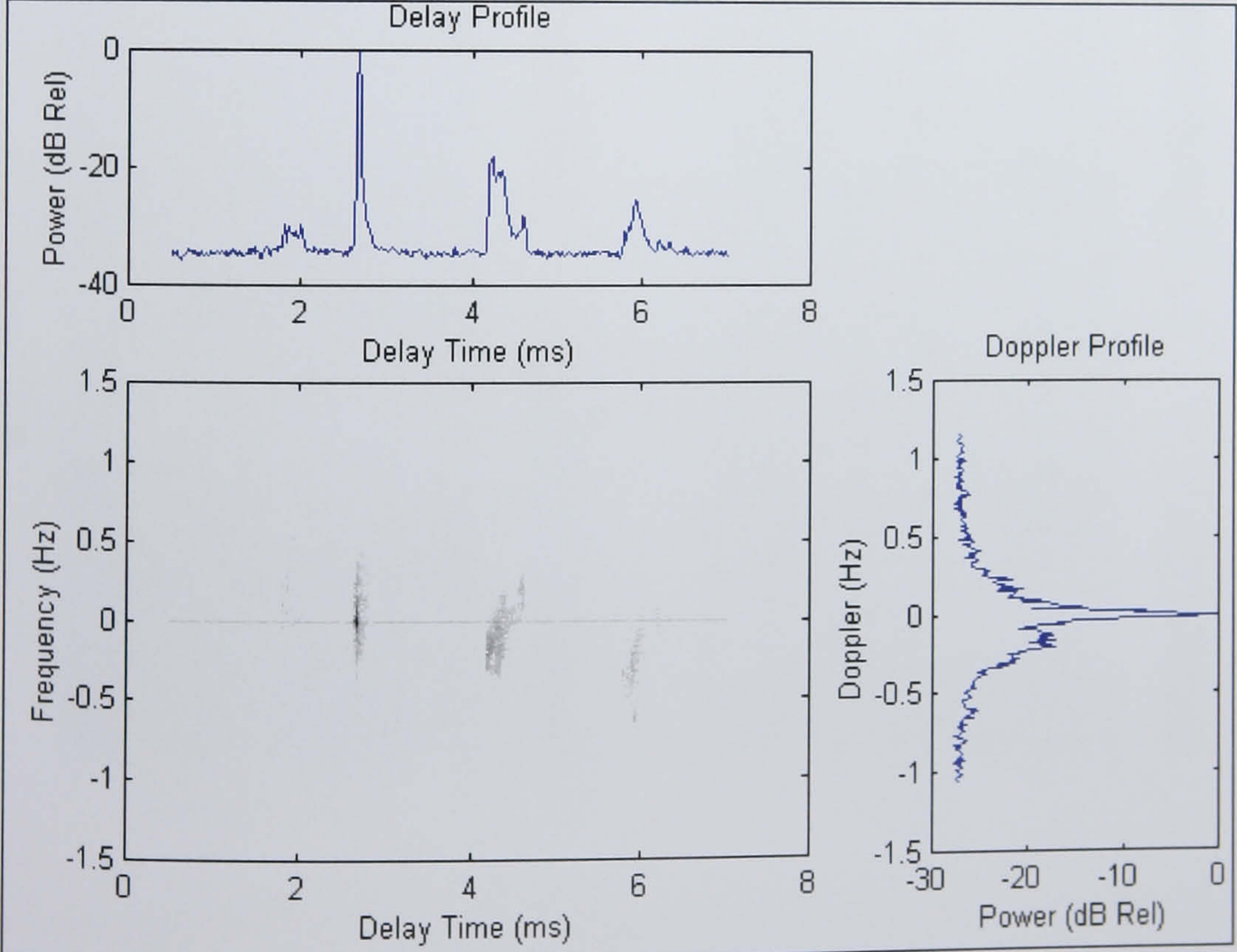


Figure 10-4 Magnified View of Channel Scattering Function (3.9 MHz 10 Apr 2001 07:38)

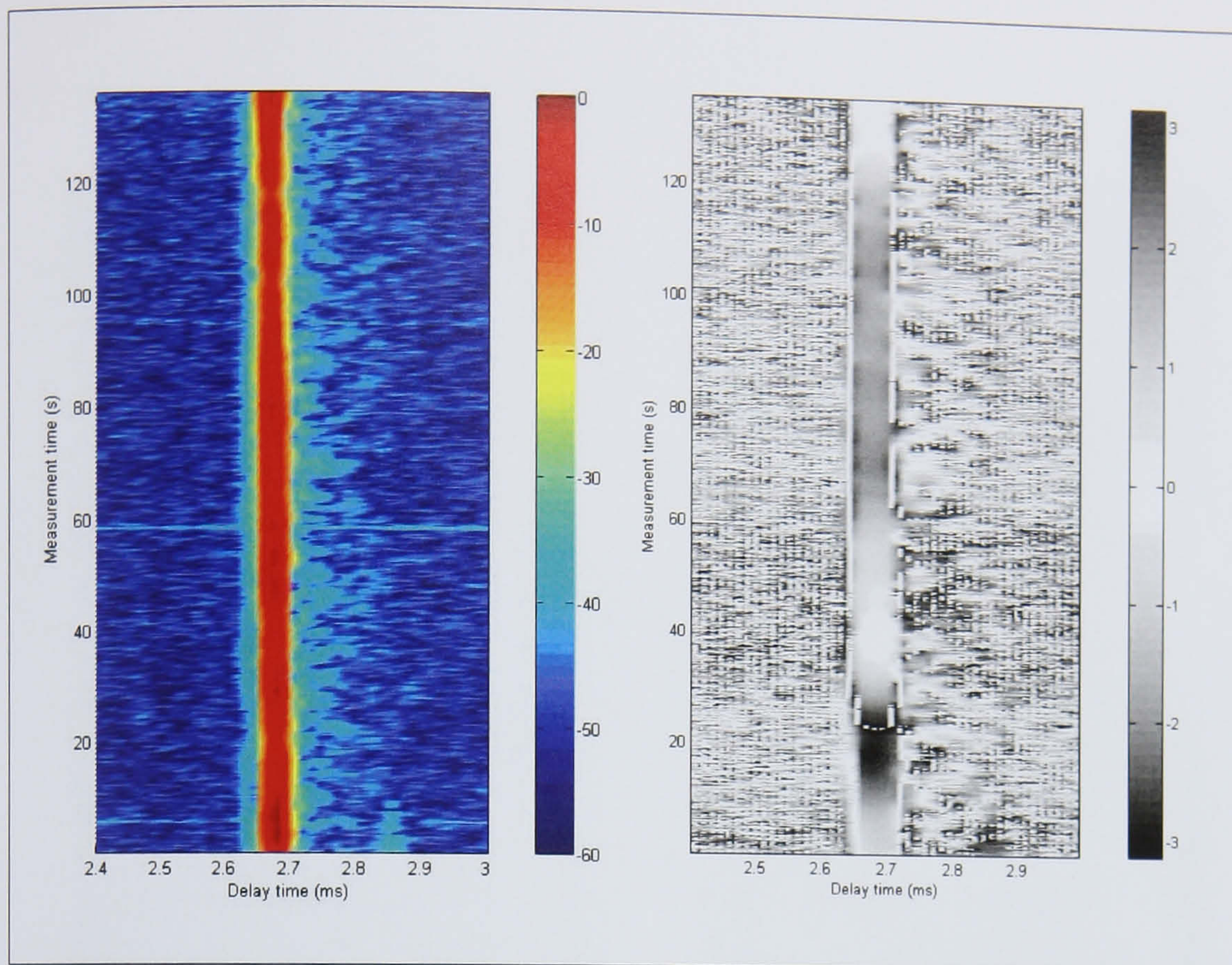


Figure 10-5 Channel Power and Phase (Radians) plotted for 2.7 ms Mode versus Measurement Time (3.9 MHz, 10 April 2001 07:38)

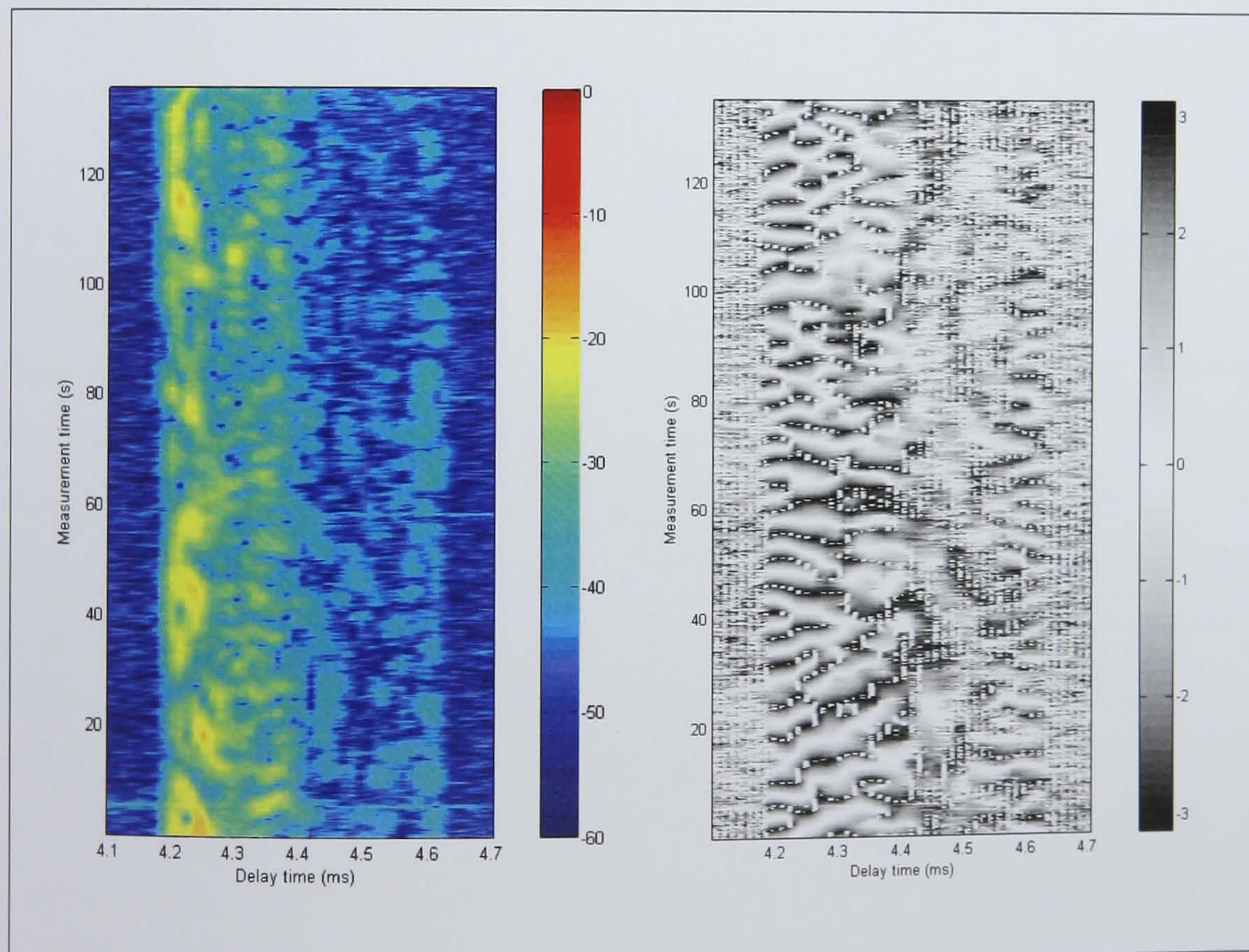


Figure 10-6 Channel Power and Phase (Radians) plotted for ~4.3 ms Mode versus Measurement Time (3.9 MHz, 10 April 2001 07:38)

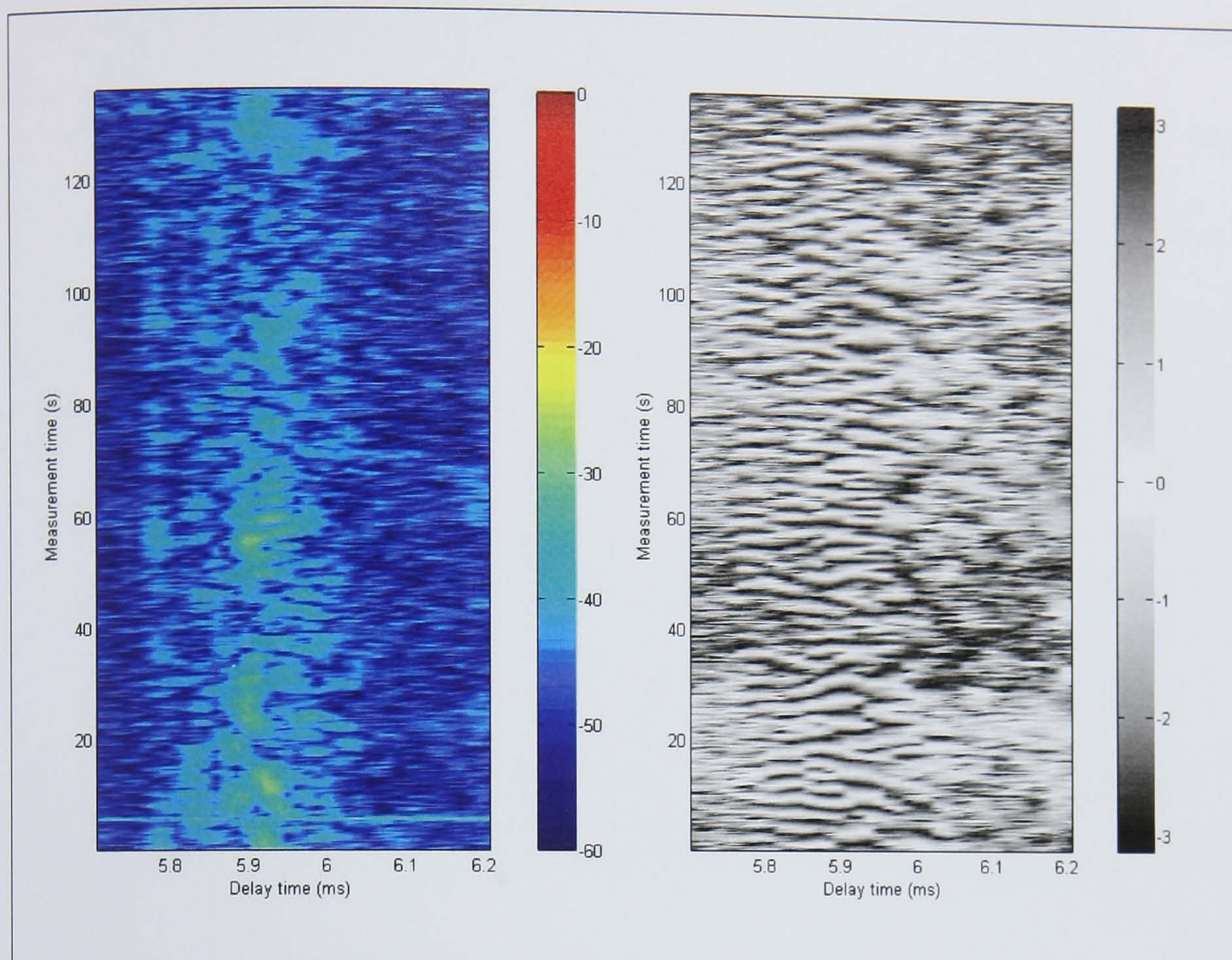


Figure 10-7 Channel Power and Phase (Radians) plotted for ~6 ms Mode versus Measurement Time (3.9 MHz, 10 April 2001 07:38)

10.2.2 Study Case Two: 9th April 2001 20:31, 6.7 MHz

This study case shows an example of where the channel is changing rapidly within the measurement timescale. It also illustrates how the Doppler filtering technique (incorporated in the data analysis tool which has been written in MATLAB) is able to remove interferers which have periodicity that alias into the Doppler spectrum away from the wanted signal. Such signals would be hard to remove in either the time domain or the frequency domain of the received signal. The oblique ionogram of Figure 10-8 illustrates the prevalent channel condition with multiple F-layer returns evident. Figure 10-9 and Figure 10-10 show the measured scattering function before and after Doppler filtering. A series of five multipath modes are discernable. The power and phase stability plot for the first mode is given in Figure 10-11. This shows the delay increasing some 0.75 ms over the 140 s measurement period.

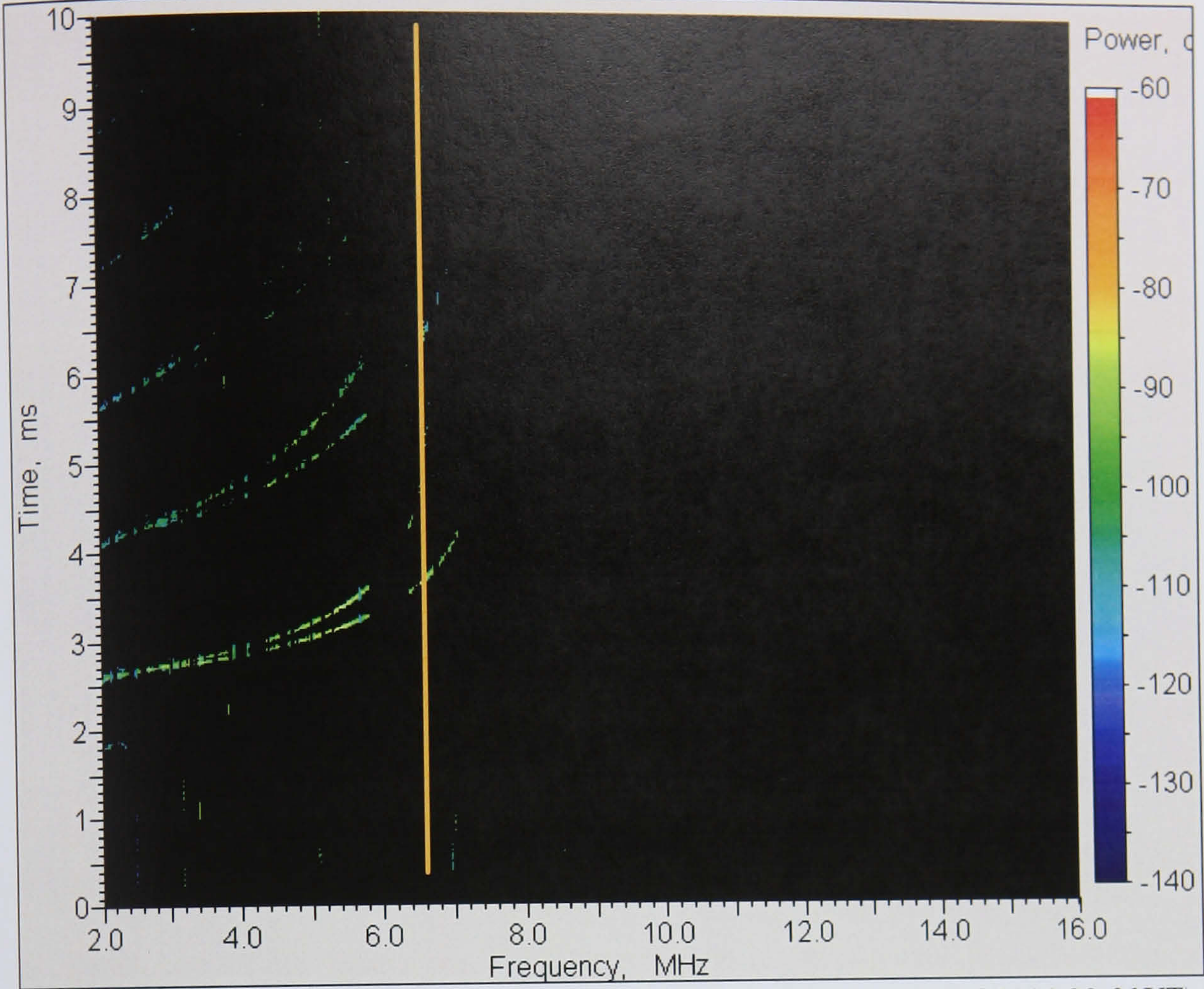


Figure 10-8 Ionogram (9 April 2001 20:31UT)

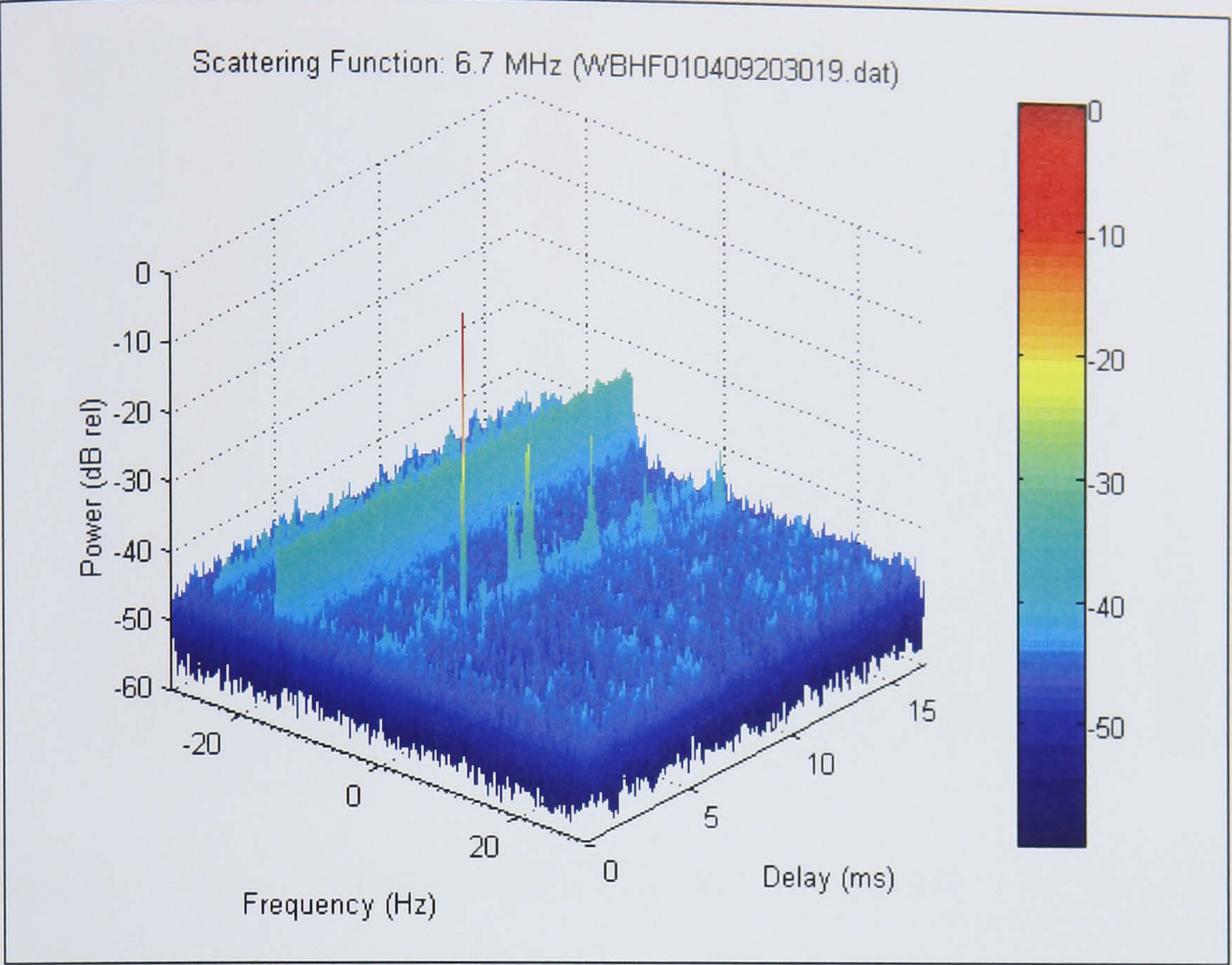


Figure 10-9 Measured Scattering Function (6.7 MHz, 9 April 2001 20:30)

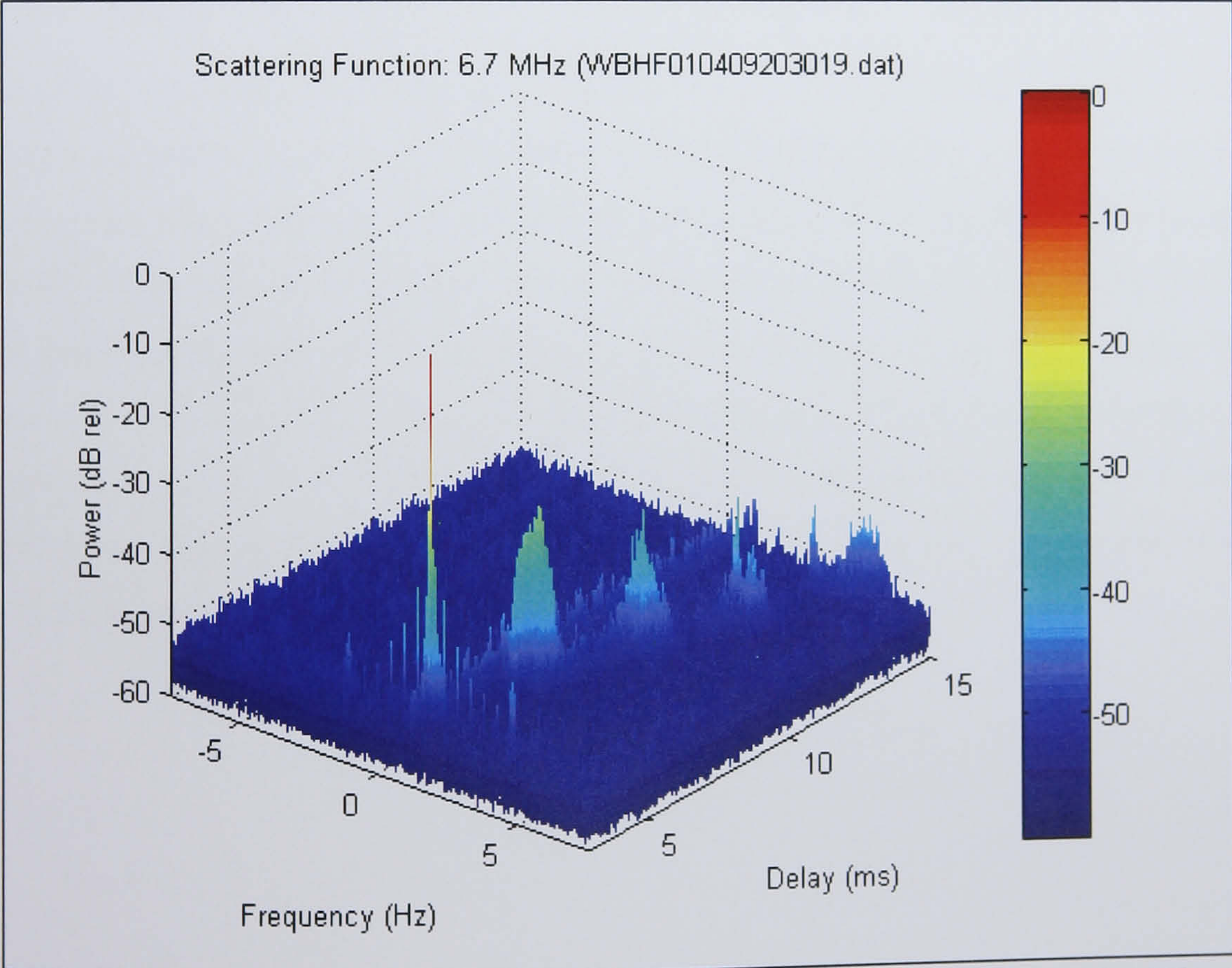


Figure 10-10 Measured Scattering Function after Doppler Filtering (6.7 MHz, 9 April 2001 20:30)

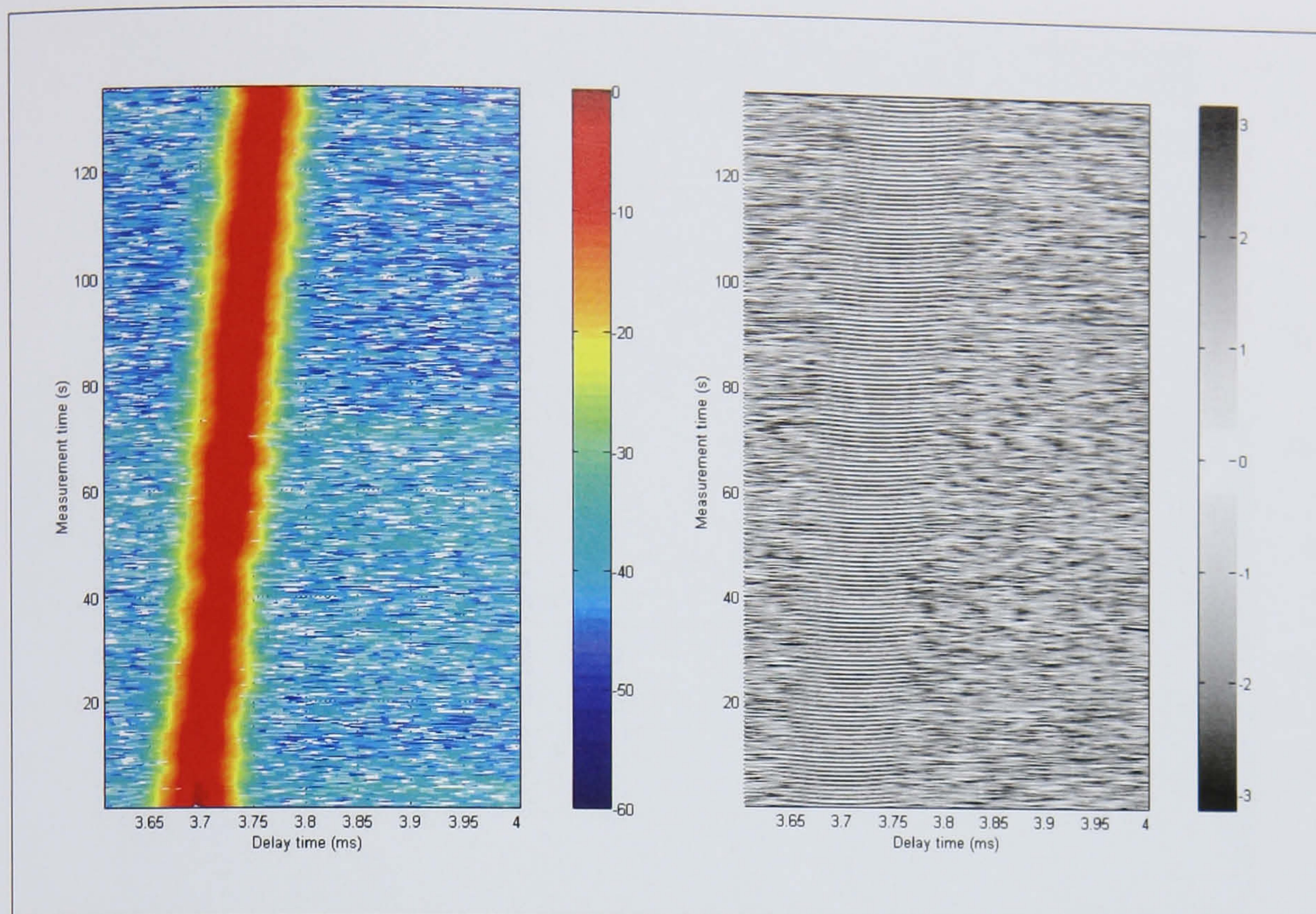


Figure 10-11 Power and Phase Plot of 3.7 ms Mode Showing Rapid Movement of Layer (6.7 MHz, 9 April 2001 20:30)

10.2.3 Study Case Three: 10th April 2001 08:10, 5.7 MHz

This final case study presented is for another case with interference present. Figure 10-12 is an oblique ionogram which indicates the basic propagation conditions present. In this case the nature of the interferer is such that it is spread across the Doppler domain of the scattering function (Figure 10-13). The benefit of the filtering process and, more particularly, the much longer integration time (~140 s) of the second plot, Figure 10-14, are evident. Whilst the first two modes have Doppler shift, they appear to be principally specular in nature (minimal power variation with time and a regular phase profile) whereas the delayed 5.4 ms mode is time dispersed and has much less structure in its phase plot.

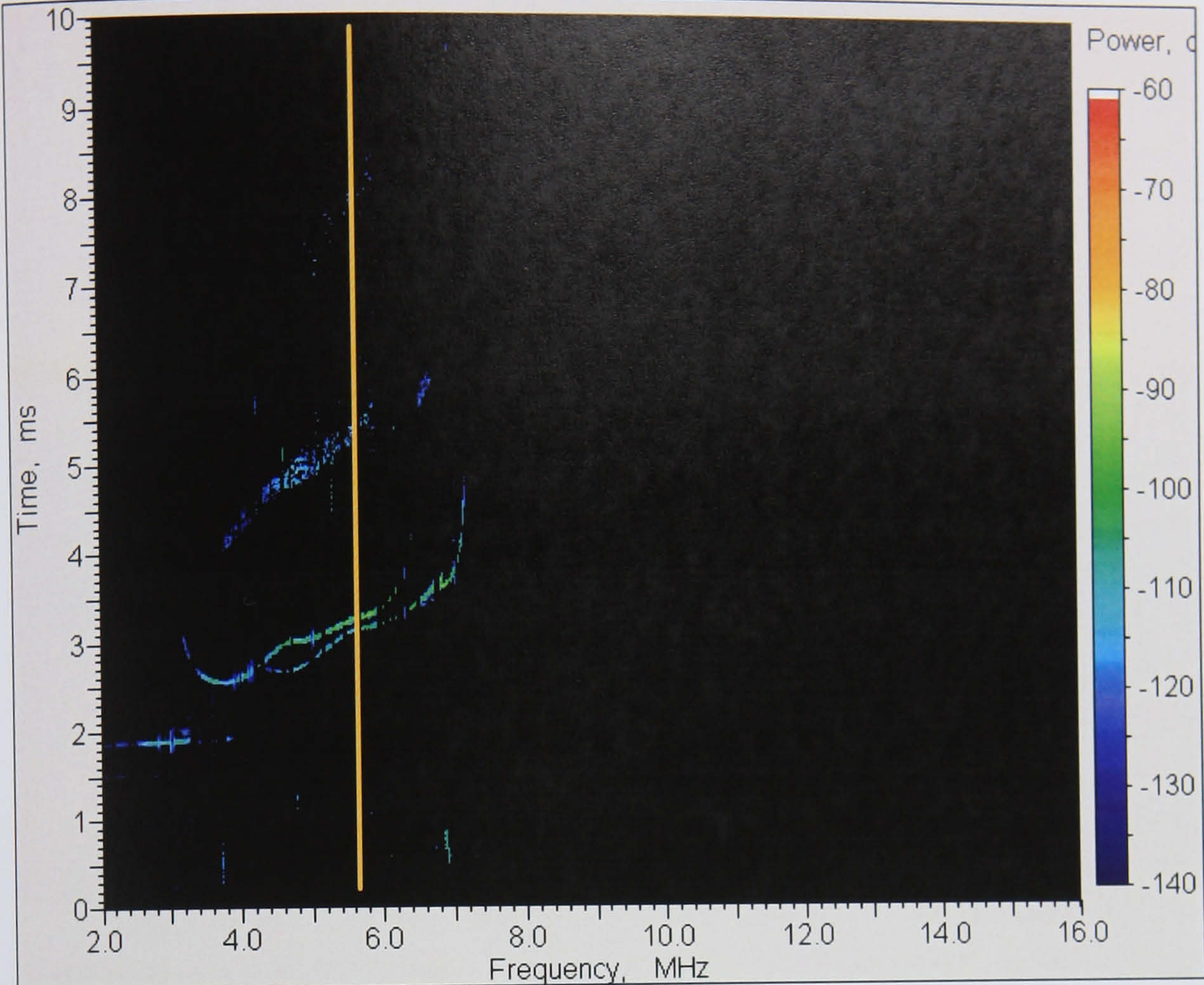


Figure 10-12 Oblique Ionogram (10 April 2001 08:10UT)

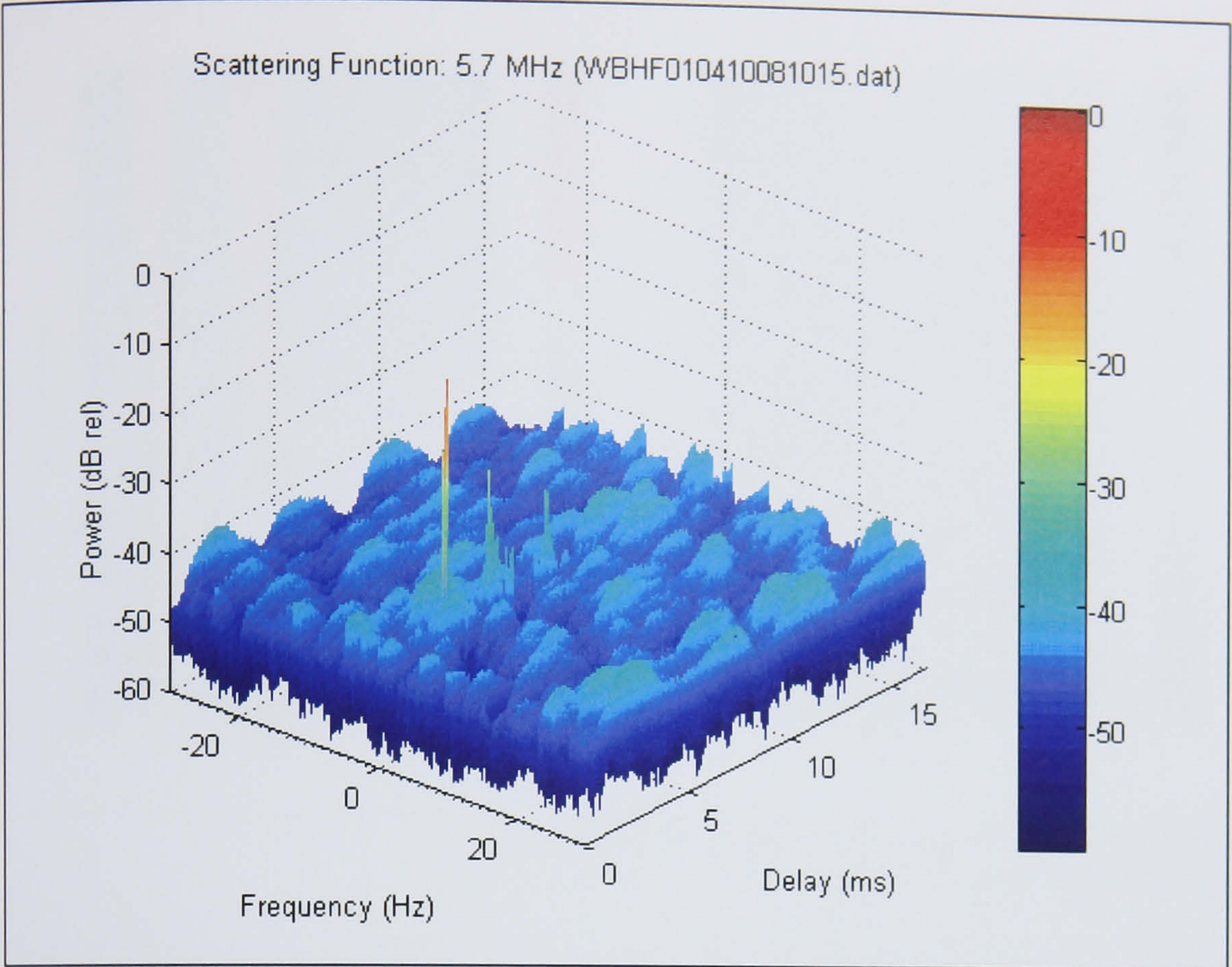


Figure 10-13 Measured Scattering Function (5.7 MHz, 10th April 2001 08:10UT)

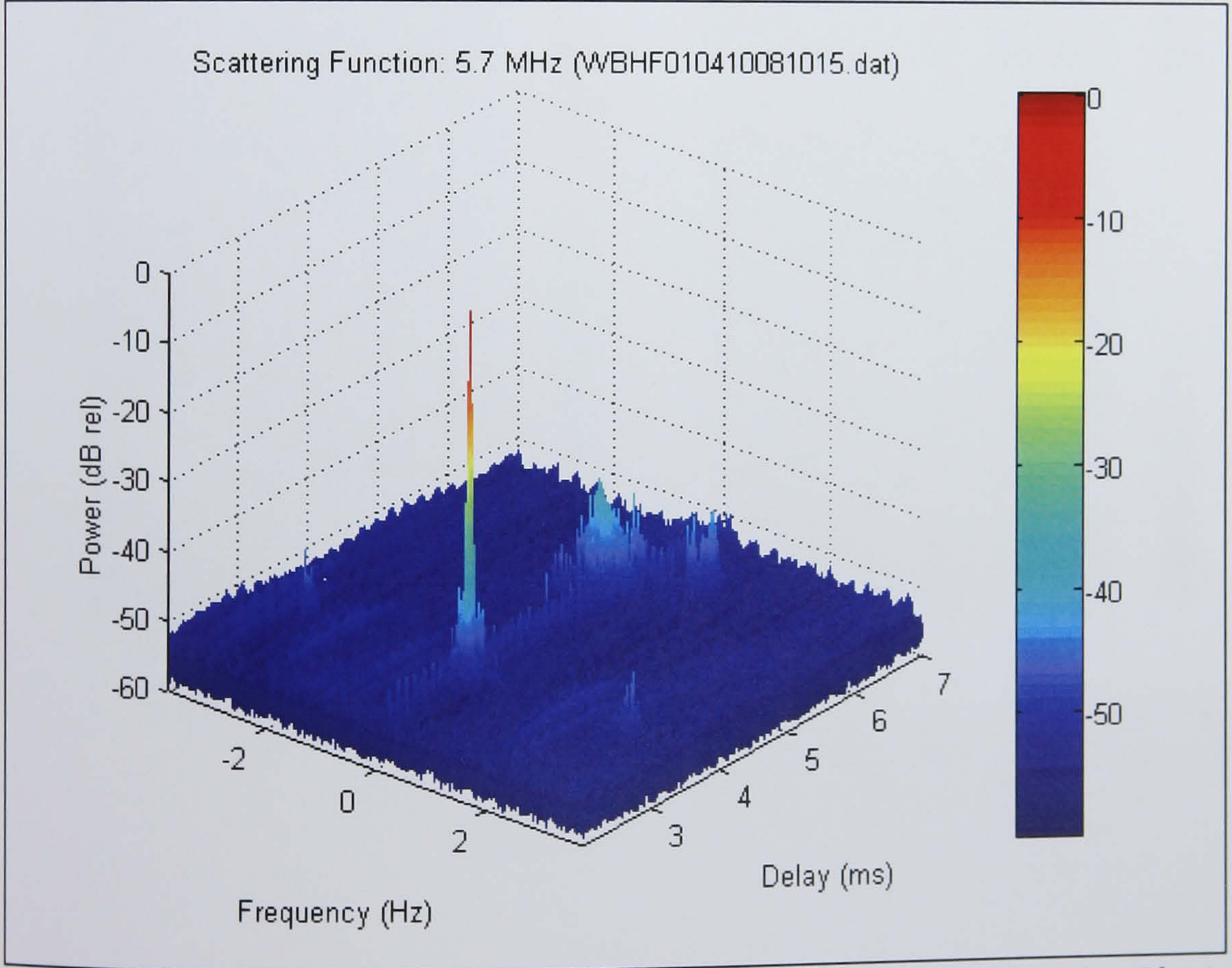


Figure 10-14 Measured Scattering Function After Doppler Filtering (5.7 MHz, 10th April 2001 08:10UT)

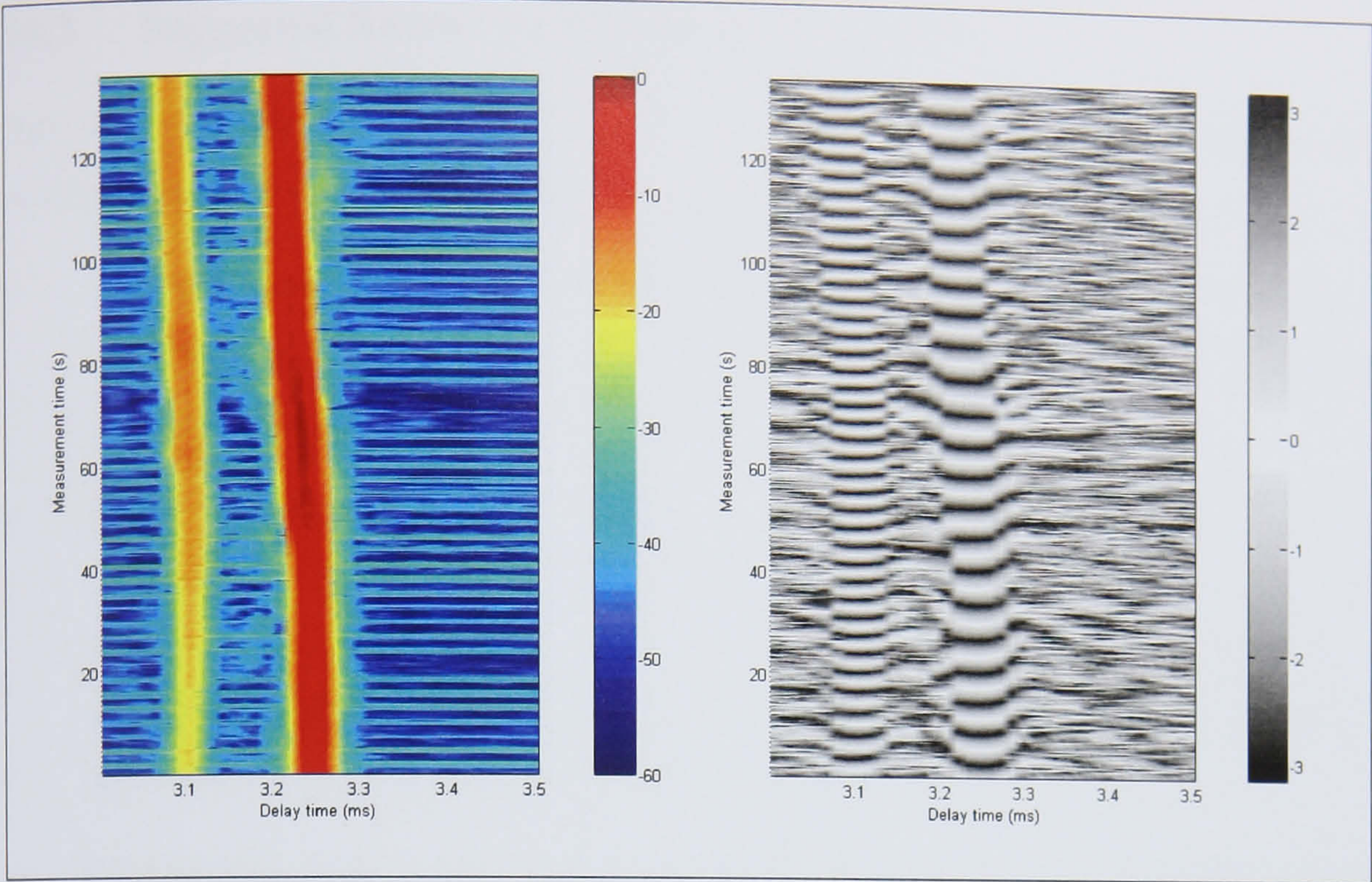


Figure 10-15 Power and Phase Plot of ~3 ms Modes
(5.7 MHz, 10th April 2001 08:10UT)

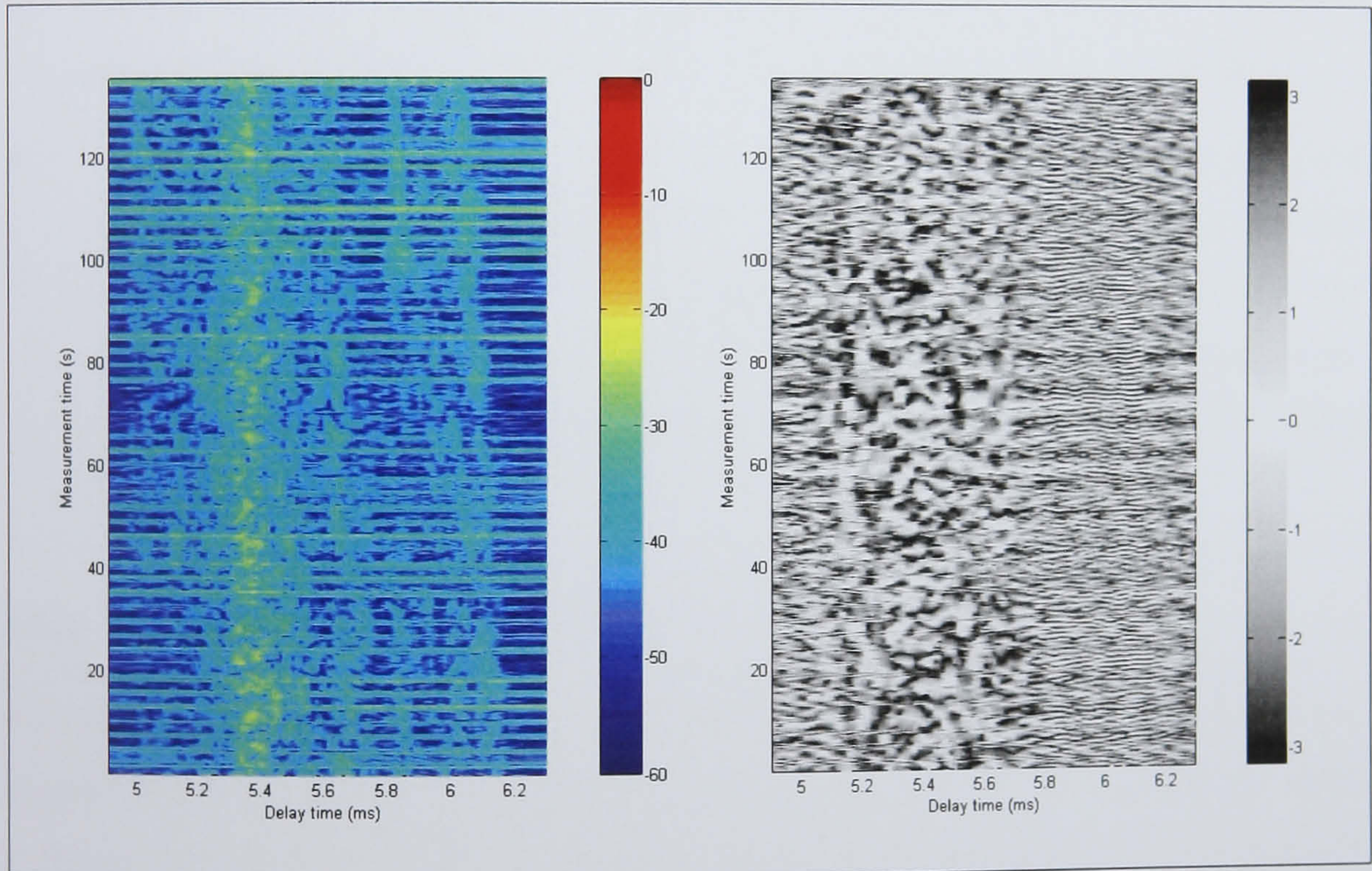


Figure 10-16 Power and Phase Plot of ~5.4 ms Spread Mode
(5.7 MHz, 10th April 2001 08:10UT)

10.3 Suggested Routes for Further Data Analysis

Only initial results from wideband measurements have been presented. A number of possible routes for detailed analysis of the data are suggested:

- **Fading Characteristics** – It is suggested that fading spectra are measured at each distinct delay times within a mode to assess the extent to which the wideband channel can be considered to be a Gaussian fading channel.
- **Fading Independence within Modes** – It is suggested that the data is analysed to determine the complex cross correlation of channel phase as a function of delay time within modes. The results presented (plots of the channel phase for non-specular modes) indicate that this would probably have to be done over relatively short periods rather than over the whole measurement.
- **Comparison with Narrowband Measurements** – It would be of value to assess the extent to which the additional structure that the wideband sounder is able to resolve makes a channel's characteristics different to those that would be measured in a narrowband channel (e.g. a Gaussian Rayleigh fading channel).
- **Interference Excision** – Whilst, even with the low transmit powers employed, the majority of the data collected appeared to be suitable for analysis, further interference excision may still be of value. A number of excision techniques that could be applicable to removing narrowband interferers from spread-spectrum signals such as this have been reported (e.g. [DiPietro, 174], also [Burley, 84] may be relevant).

10.4 Chapter Summary

This chapter has detailed a series of initial measurements of the wideband time varying channel complex impulse response on a 170 km path in the UK during Spring 2001 using the WHISPER sounder. The results presented are corroborated by an oblique FM CW channel sounder that was used to collect data simultaneously on the same link (it shared antennas and the transmitter PA). The results analysed confirm the ability of the WHISPER sounder to measure the channel scattering function and the amplitude and phase within individual modes. Even at this early stage the data considered so far suggests that (for the conditions observed) the principal modes are often largely

specular in nature. This may have important implications for the implementation (and simulation) of wideband communications. A number of possible directions for more detailed analysis have been identified.

Chapter 11.

Applications of Digital Radio in the HF Band

This chapter identifies a number of applications for digital radio in the HF band. Potential applications include the implementation of digital broadcast receivers, channel sounders, RF channel simulators and advanced automated HF communications systems. Finally, two examples of applicable non-HF applications are identified.

11.1 Digital Broadcast Receivers

A potential application of the new direct sampling digital receiver architecture presented in this thesis is as the basis for a digital broadcast receiver. Such a receiver may be particularly attractive for new services such as DRM [ETSI, 182]. DRM includes a technique called automatic frequency control to obviate listeners from having to tune to different frequencies across the band to determine which give satisfactory signals. Control data streams are multiplexed with the audio transmission and these provide information on when broadcasts will change frequency and which other frequencies are broadcasting the same programming. An intelligent receiver can use this information to optimise reception. As well as the initial acquisition of a signal, adaptive techniques can be used to provide fade mitigation and improved reception quality. The ability to have multiple digital receivers maximises this flexibility. One receiver can be used for reception of a selected broadcast whilst the other can continually scan alternate frequencies to compare the signal quality. Ultimately, with two (or more) parallel receivers it is possible to implement frequency diversity reception techniques [Stott, 183].

The work on direct-sampling receivers presented in this thesis was originally presented by the author in 2000 [Davies, 184] and has led to the development of at least two receivers of a similar type by other research groups: [Stott, 183] and [Bradley, 185].

11.2 Chirp Sounder

HF chirp sounders (FMCW sounders, see 9.1.2.3) are well established both for use in propagation research and to support the practical management of HF communications. However, they are generally large, expensive and complex to implement¹ (e.g. [Arthur, 180]). A particular challenge is the need for a high quality local oscillator capable of coherent sweeping. Implementing such a function within a programmable digital receiver (i.e. DDC) is an attractive solution – it adds minimal complexity to the NCO design. One of the design features of the wideband HF digital transceiver platform (presented in Chapter 7) is that the DDC is controlled via the processing FPGA. This would make it straightforward to implement an application to coherently sweep the receiver (by synchronously re-programming it). Other processing functions (principally an FFT) could be readily implemented in software residing either on the DSP subsystem or in the host computer. An additional benefit of a digital receiver implementation is the large instantaneous linear dynamic range available. This minimises the need for an AGC function which, if it were required, would have to be carefully characterised to allow absolute power measurements to be undertaken.

11.3 RF Channel Simulator

HF channel simulators are widely used in the development and performance assessment of HF systems, particularly baseband (audio frequency) testing of data modems. The principal benefit of testing using channel simulators as opposed to ‘over-the-air’ trials is that repeatable measurements can be made using known channel characteristics. Whilst on-air trials are valuable they are expensive to undertake and often require extended measurement periods in order to obtain results under all the propagation conditions of interest. Whereas traditionally HF radios and modems have been separate pieces of equipment, it is now not uncommon to find that a HF radio is a complex, integrated HF terminal including automatic channel selection (ACS), automatic link establishment (ALE), data modems and link layer functions (e.g. STANAG 4538 ARCS [NATO, 187], STANAG 5066 [NATO, 81]). Further, modern high throughput waveforms using higher order modulation schemes are increasingly sensitive to the implementation of the

¹ A low cost receiving system for chirp transmissions has been implemented by Gallagher [Gallagher, 186]. Whilst it is a useful tool, its technique of stepping matched filter reception in a fixed bandwidth gives low processing gain and reception compared with the FMCW approach.

radio itself (e.g. filtering, receiver AGC, transmitter ALC). Hence, in order to be able to effectively assess the performance of such modern systems in a controlled manner an RF simulator would be of great utility.

Figure 11-1 is a block diagram outlining a suitable architecture for a frequency agile HF channel simulator [Birch, 188], [Davies, 189]. By employing whole-band digitisation and subsequent digital processing it would be possible to use techniques such as the FFT to track a frequency agile input signal and modify the channel simulator's parameters based on the simulated conditions at that frequency.

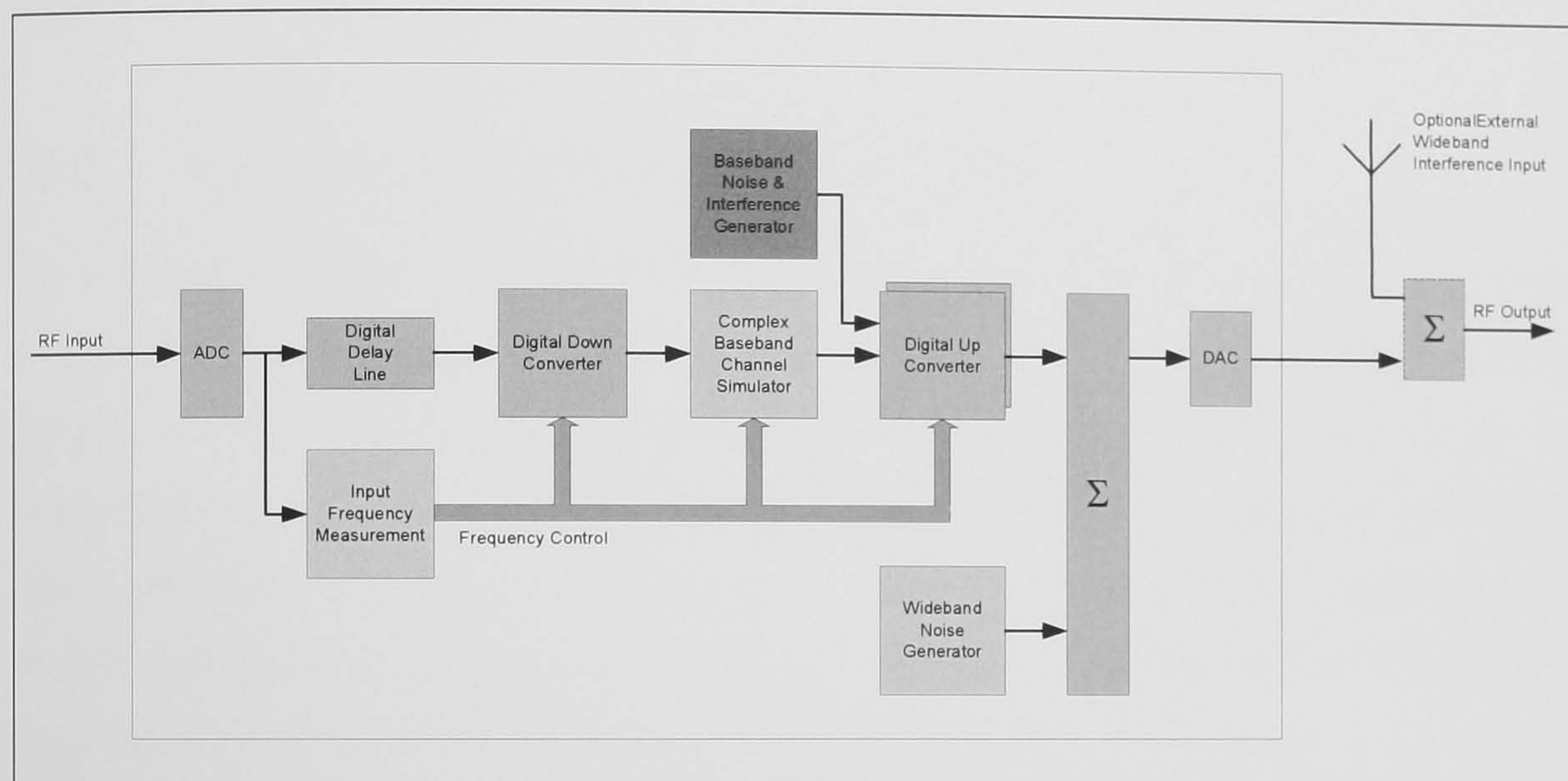


Figure 11-1 Frequency Agile Simulator Architecture

11.4 High Performance ALE Systems

Establishing reliable links over HF circuits has traditionally required skilled operators who have the experience (and patience) to determine the best channels (frequencies) to use at a particular time of day for a given circuit and then to establish communications on them. Automatic link establishment (ALE) systems automate this process using a process called automatic channel selection (ACS) to determine the best frequency to use. The most widely used ALE system is MIL-STD-188-141A Appendix A [DOD, 191]. A receiver waiting for a call scans a list of allocated frequencies (a scan list), pausing to listen for a short time on each. The time spent on each frequency is called the dwell time and is typically 0.5 s. Thus it would take 5 s for a receiver to listen to all the frequencies in a ten channel scan list. A transmitter in the same network trying to establish a call must transmit the call message (perhaps ~1 s) plus an additional 5 s to ensure that the called receiver(s) will have time to scan round to the calling frequency

and hear the call. If the frequency tried didn't work this has to be repeated. If all ten channels have to be tried this would take 50 s. In more complicated networks there may be more than ten frequencies in use. In some applications the call time can be excessively long.

A digital radio platform, based on ideas incorporated in the digital transceiver presented in this thesis, would allow the implementation of a high performance ALE system. With a direct sampling, wideband digital receiver it would be possible to allocate several DDCs to the task of scanning for calls and so significantly reduce the call setup time.

11.5 Applications in Other Frequency Bands

As was demonstrated in Chapter 6 the prototype direct sampling receiver implemented can be successfully used to bandpass sample (sub-harmonically sample) frequencies in excess of 200 MHz. This would allow the application of the technology to implementing an IF/baseband sub-system for higher frequency applications (using a single or dual conversion RF front-end). As the digital transceiver platform was implemented with two RF channels it would be possible to utilise one for HF and one for a higher frequency receiver thus making a multi-band software radio.

11.6 Applications to Weather Radar

Digital radio has application in the implementation of high performance 'software radars'. The digital transceiver platform presented in Chapter 7 has recently been applied to a University of Bath EPSRC research programme entitled "Development and Application of an Advanced Digital Receiver System for Atmospheric Radar" [Watson, 192]. By replacing conventional analogue radar waveform generators and receivers with high dynamic range digital receivers and DSP performance and functionality can be significantly increased. Examples of improvements, which are of interest to the radar metrology community, include (from [Watson, 192]):

- Zero in-phase and quadrature phase error, gain imbalance and offset (DC bias) errors of digital receivers. These errors manifest themselves as image spectra or clutter echoes in the Doppler spectra.
- Wider dynamic range with a truly linear response;

- Any number of channels can be constructed with a high degree of repeatability – cross covariance parameters in polarimetric radars are then more a function of the target and less a function of the receiver;
- Greatly reduced temperature sensitivity; and
- Reconfigurable in real-time – for example, the final IF filtering characteristics can be changed on a pulse-to-pulse basis if required.

Chapter 12.

Conclusions and Recommendations for Further Work

This thesis has presented new work on digital radios and their application in the HF band.

New waveforms have been proposed for the transmission of higher data rates in an extended HF channel bandwidth (6 kHz). The results of laboratory tests and analysis of data collected during on-air trials of implementations of these 16 kbps waveforms have been presented. The analysis undertaken indicated that these new waveforms would be capable of reliable operation over surface wave and benign HF Skywave channels providing a sufficient received SNR can be maintained. The work presented has contributed to the international standardisation of higher throughput waveforms (specifically US MIL-STD-188-110B). It has also demonstrated the value in exploiting wider bandwidths for HF radio applications.

Architectures for the implementation of wideband and multi-channel digital HF radios (software radios) have been investigated. The requirements for high performance receivers as a consequence of the HF propagation, noise and interference environment have been established. A new direct-sampling architecture for a digital HF receiver has been proposed. In such a receiver the entire HF band is digitised and then all subsequent processing is undertaken digitally, conceptually allowing an arbitrary number of channels to be simultaneously received. A practical design for a direct sampling receiver is analysed showing that it is now possible, for the first time, to construct a high performance receiver using this architecture. The work indicates that, with careful design, such a receiver should attain performance comparable with (or even exceeding) that of many high quality conventional super-heterodyne single channel receivers. A prototype wideband direct sampling receiver (part of a digital HF transceiver platform) has been implemented and its performance characterised confirming the potential for such a design.

A new high performance wideband, multi-channel HF transceiver using the direct sampling architecture has been designed and constructed. It has been implemented as a

highly re-configurable software defined radio platform intended to support diverse applications including use as a wideband or multi-channel radio/modem and for channel sounding.

An event based processing architecture for use across an array of heterogeneous processors has been conceived, developed and implemented on the wideband digital HF transceiver platform. It uses an active messaging concept in which messages arriving in a queue cause pre-defined processing activities to take place.

A new, high resolution wideband oblique HF channel sounder, which has become known as WHISPER, has been developed and implemented as an application on the wideband digital HF transceiver platform. The system is very flexible with sounding waveforms and their characteristics (sounding waveform, bandwidth, repetition interval etc) being determined by a configuration file. The sounder makes use of an external GPS receiver to provide accurate synchronisation of transmitter and receiver in order to allow time-of-flight measurements to be made. Pulse-compression sounding waveforms with carefully controlled time sidelobes have been designed to allow high fidelity measurement of the time varying characteristics of wideband (~80 kHz) HF channels. The high performance of the complete sounding system has been verified through back-to-back RF tests in the laboratory.

The WHISPER wideband sounder has been used to make high resolution measurements of the time varying complex impulse response on a 170 km path in the southern UK. The results of these measurements have been analysed and confirm the ability of the sounding instrument to measure the channel scattering function and the amplitude and phase within individual modes. A number of possible directions for a more detailed analysis have been identified.

12.1 Recommendations for Further Investigation

This thesis closes with suggestions for a number of areas in which further work has been identified.

12.1.1 Extended Bandwidth Modems

A number of areas have been identified in which more work could be done on improving and assessing the extended bandwidth (6 kHz) high throughput prototype

modem presented in Chapter 4. The modem as implemented contained no interference excision and performance was observed to suffer in the presence of co-channel interference. Even relatively simple techniques such as tone excision (e.g. adaptive tone excision [Darbyshire, 83] or sophisticated techniques such as those based on cyclostationarity [Burley, 84]) would be expected to significantly improve performance.

The modem initial synchronisation and preamble was short (~ 0.1 s) and the modem's initial synchronisation performance consequently weak. This was clearly demonstrated when file transfers were attempted - often the first part of a file was missed while the remainder was received with few errors. It is considered likely that a longer initial synchronisation would readily cure this problem.

The short interleaving option included in the modem was optimised for low latency applications (such as digital voice applications). It has been shown to provide little benefit over the non-interleaved mode and would benefit from being replaced with an interleaver of at least one second duration to provide increased robustness for data communications.

The on-air trials of the modem were undertaken during a short period in Spring 1998 on a single short sky-wave path. It would have been valuable to deploy the modem on other paths and under other propagation conditions to assess its performance more fully.

12.1.2 Direct Sampling Digital Radios

In the time since the practical work presented has been completed the speed and capacity of FPGA devices has increased significantly (from $\sim 100,000$ gates to over two million). It would be valuable to consider an implementation using a high performance FPGA to replace the DDC and DUC ASICs of the digital transceiver as this would further increase flexibility. This would allow high dynamic range DDCs/DUCs to be implemented. With the availability of ADCs with faster sampling rates it would be possible to provide whole-band coverage and make the front-end pre-selector design easier. To achieve the full promise of the architecture a more linear RF amplifier is required. It would be valuable to incorporate this latter change and then to assess the performance of the receiver in a number of general use environments (perhaps alongside other high performance radios).

It would be interesting to implement a wideband interference characterisation application for the digital transceiver to act as a passive monitor collecting absolute signal strength information from across the HF band. In addition to examining the basic statistics of the environment, this could be extended to recognise and classify signal types present at different frequencies in order to gain a better understanding of the nature of the interference. For example, the information could be used to assess which classes of interference modem designers should test their modems with (or possibly even excise).

12.1.3 Event Based Processing Architecture

Whilst the event based processing architecture was shown to be successful a number of areas in which further work would be beneficial have been identified.

The local bus processor code is currently written in C because a SHARC C++ compiler only became available after the implementation was complete. It would be interesting to translate the existing code to C++ (which would then better mirror the host side software) and to determine if this activity suggests any improvements in the processing architecture. At the very least an object oriented implementation would be more robust because more extensive encapsulation (virtualisation) could be employed. Having multiple dynamically instantiated objects on the local bus processors would likely require a more complex (and more uniform) approach to addressing.

The local bus processor code was written for a cluster of SHARC processors without the benefit of a multi-threaded RTOS. The provision of a multi-threaded environment would be expected to simplify the messaging software infrastructure (but not its efficiency) and may suggest further extensions in capability.

An improved (i.e. bug-free) Windows driver for the PLX9054 PCI bus interface device to allow DMA transactions to be employed in both directions between host and local bus processors would realise the throughput inherent to the architecture.

It would be relatively straightforward to extend the capability of the message pumps that process pending message queues to allow messaging with different priorities. This would allow processing of higher priority messages to be expedited.

Whilst processing functions are manually allocated to a particular processor it might be possible to develop light-weight techniques to allow messages to be routed to the

processor that is most lightly loaded at any given time based on metrics for historic processing load and (automatic) benchmarking of the time taken to process particular messages.

The work presented here concentrates on the deployment of application software across multiple heterogeneous processors. It would be interesting to extend the work to look at more flexible ways of configuring both the DSP processors and the PLDs and developing techniques applicable to further abstraction from the hardware. In the time since the original practical work was completed it is understood that this has become a major research topic for software radios.

12.1.4 Wideband HF Sounders

The current sounding waveforms are cyclically repeated PN-sequences. However, this periodicity means that the power spectrum will be a comb with peaks spaced at the PRF. The wideband nature of this sounder means that it often has to operate on a shared, non-interference basis with other (primary) users. By applying a known pseudo random modulating code (to apply a 0° or 180° phase change to each sounding waveform repeat) it would be possible to spread the energy and reduce the waveforms power spectral density (PSD) further than it is currently. Given good synchronisation and knowledge of the code, this is a process that is reversible at the receiver. A randomising code that repeated every 8192 PRIs could provide up to an additional 40 dB reduction in PSD.

When making HF channel measurements it is very useful to have access to real-time ionograms to allow interesting propagation conditions to be identified and investigated. To increase the utility of the WHISPER sounder it would be possible to exploit the multi-channel nature of the digital transceiver platform to implement a second sounder that could operate in parallel with the primary pulse compression mode. In particular it would be particularly useful to implement a Chirp sounding function. The principal challenge would be implementing a sweeping LO. This could be done by implementing logic in the digital transceiver processing FPGA code in one of two ways. The DDC NCO could be programmed at a rate sufficiently high to cause it to appear to sweep coherently. Alternatively, it would be possible for the FPGA to re-program the DDC NCO to step in frequency every N samples and then for a final stage of complex frequency translation to be implemented in software after the DDC.

12.1.5 Analysis of Wideband Channel Data

In section 10.3 a number of specific routes have been suggested for the analysis of wideband channel measurement data with the aim of investigating fading correlation within modes and the extent to which the wideband channel may still be considered a Gaussian fading channel. The degree of correlation of fading within time dispersed modes may have significant implications for modem designers and influence the implementation of wideband channel simulators (where the degree of correlation may be another parameter that must be specified).

It is suggested that future wideband channel measurements be compared with interspersed narrowband measurements to assess the benefits of having a more detailed description of the channel (i.e. are the present models, such as the Watterson model [Watterson, 12], adequate? If they are acceptable what should the simulation parameters be).

The data presented in this thesis was collected in a single 24-hour period on one 170 km path in the southern UK. It would be valuable to collect and analyse data from across a much broader range of conditions.

It would be useful to compare the results of measured data with some of the new HF channel models that have recently been proposed (e.g. [Strangeways, 47], [Vogler, 43]) in order to both verify their veracity and to better understand the relationship between the detail included in the ionospheric specification and the accuracy of the results.

Another interesting avenue of investigation would be to deploy a multi-channel sounder (which may readily be implemented using a number of digital transceivers with their diversity capability) with multiple antennas. This would allow the investigation of spatial decorrelation in the HF channel and consequent possible gains from multiple-input, multiple-output (MIMO, [Foschini, 193]) transmit and receive diversity (space-time processing of received signals).

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Appendix A.
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Appendix B.

A Wideband HF Channel Model

B.1 Introduction

Chapter 2 introduced a number of classes of HF channel models that may be used to implement simulators that can be used to evaluate the performance of HF systems (e.g. data modems). In particular the Watterson model, as documented by [ITU, 13], is a widely used (although imperfect) *defacto* standard applicable to narrowband channels (less than around 12 kHz). Work has been done to develop complementary wideband channel models. Of particular note is the improved ionospheric channel model that has been proposed by the Institute of Telecommunication Sciences (ITS) [Vogler, 43]. The model includes delay spread and non-Gaussian fading, but simplifies to the standard Watterson model for zero delay spread and Gaussian fading. Although developed as a wide-band model, the ITS model can also be applied to narrow band channels. Channel simulation using this model requires the re-construction of the time-varying channel impulse response; $h(t, \tau)$. The methodology for this reconstruction, outlined in the following sections, follows that of [Mastrangelo, 44] and [Behm, 45].

B.2 ITS Channel Model - Impulse Response Reconstruction

The overall channel impulse response is defined as a sum of the impulse responses of each propagation mode, and is a function of time t and delay τ . The ITS model represents the impulse response of each mode as the product of three terms - a stochastic modulating function ($\psi_n(t, \tau)$), that is defined by the Doppler spread and spectral shape; a deterministic phase function ($D_n(t, \tau)$) defined by the Doppler shift and rate of change of Doppler shift with respect to delay; and the square root of a delay power profile ($P_n(t, \tau)$), defined by the propagation mode's time of flight, its delay spread and its maximum power.

$$h(t, \tau) = \sum_n h_n(t, \tau) \quad (B-1)$$

$$h(t, \tau) = \sum_n \sqrt{P_n(\tau)} D_n(t, \tau) \psi_n(t, \tau) \quad (B-2)$$

Each of these terms will be examined in the following sections, and a simplified diagram of the process is depicted in Figure B-1.

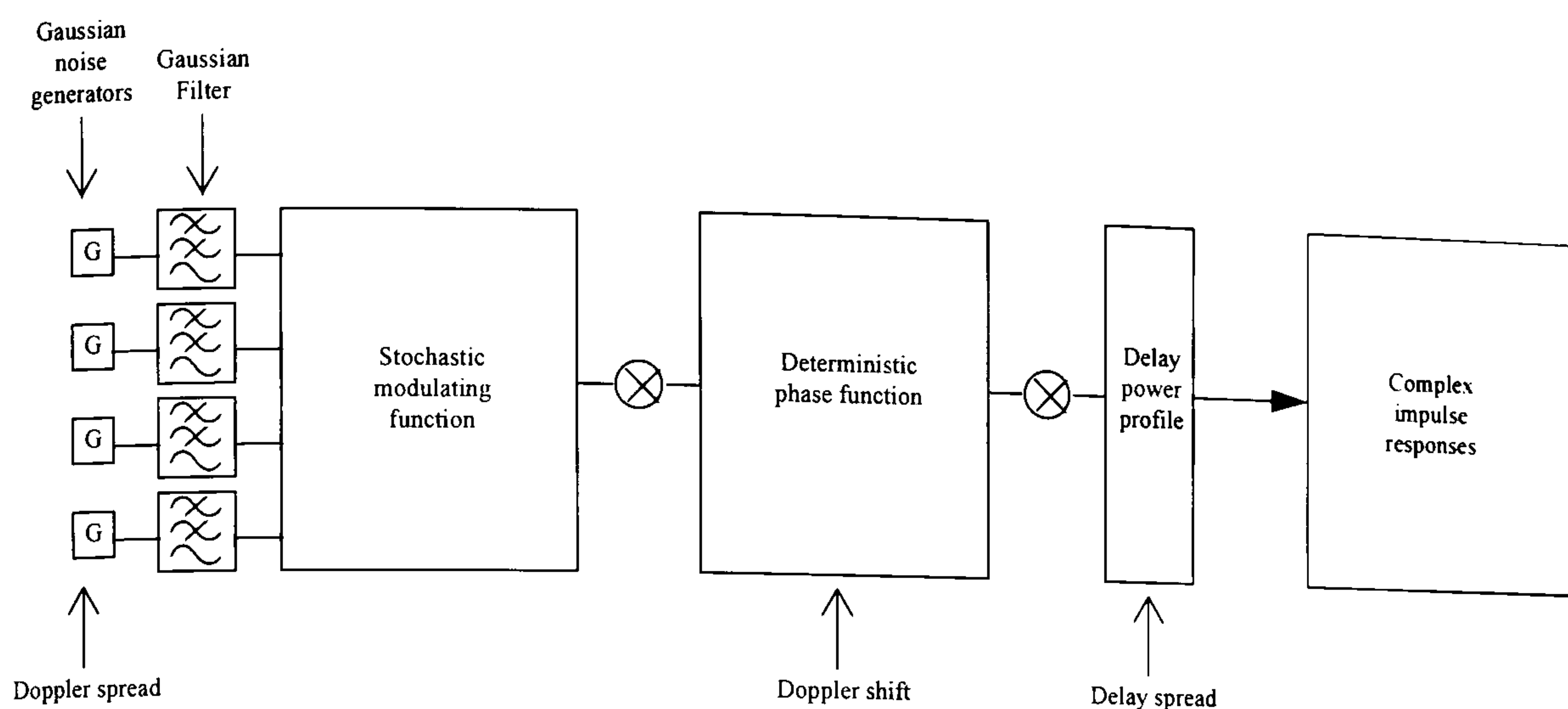


Figure B-1 Block diagram of impulse response reconstruction [Angling, 46]

B.2.1 Stochastic Modulating Function

In order to model the fading of the impulse responses, the stochastic modulating function (SMF), $\psi(t, \tau)$ is constructed from an ensemble of time series of random complex numbers. At each delay offset a random number sequence is constructed, whose real and imaginary parts are independent, white and Gaussian. This is convolved with a Gaussian filter, to produce a random number sequence that exhibits Raleigh fading and whose power spectrum's width corresponds to the required Doppler spread of the mode.

B.2.2 Deterministic Phase Function

The Doppler shift of the mode is implemented by multiplying the SMF by a deterministic phase function:

$$D(t, \tau) = e^{j2\pi[f_s + m(\tau - \tau_c)]t} \quad (B-3)$$

where t is the time variable, τ is the delay variable, τ_c is the delay of the mode peak, m is the rate of change of Doppler shift with respect to τ , and f_s is the Doppler shift at $\tau = \tau_c$. This function allows for the inclusion of slant modes - i.e. modes whose Doppler shift varies with delay.

B.2.3 Delay Power Profile (DPP)

The Delay Power Profile (DPP) determines the shape of the mode in the delay dimension and is defined by the position (in delay) of its peak, τ_c , and the positions of two points of intersection with a threshold, τ_L and τ_U , (Figure B-2).

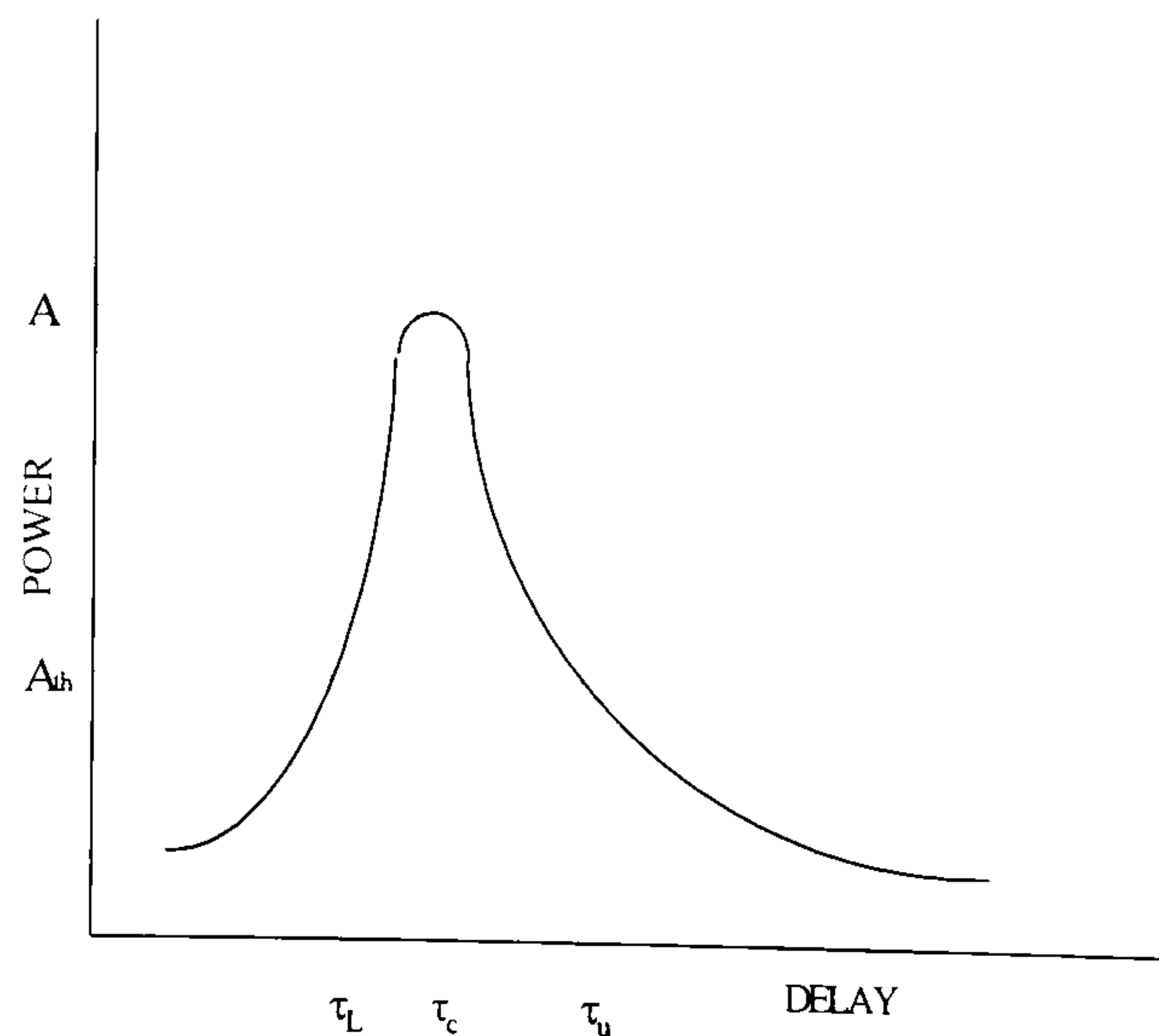


Figure B-2 Delay Power Profile [after Vogler, 43]

Mathematically, the profile is defined by:

$$P(\tau) = Ae^{\alpha[\ln z + 1 - z]} \quad (B-4)$$

where

$$z = (\tau - \tau_l) / (\tau_c - \tau_l) > 0 \quad (B-5)$$

and A is the peak power of the mode. The parameters α and τ_l control the width and symmetry of the profile. They depend upon the delay spread and the threshold level and are calculated by an iterative method, [Vogler, 43].

This function, proposed by Vogler and Hoffmeyer, will only allow the DPP to be skewed so as to have a fast attack and a slow decay. However, propagation measurements from instruments such as DAMSON [Davies, 49] also contain frequent examples of modes with a slow attack and fast decay. Consequently, in these cases the model has been extended [Angling, 46] such that the values of τ_L and τ_U are swapped, the DPP is generated and then rotated about the delay of the profile peak. This allows the DPP to vary from symmetric to highly skewed in either direction.

B.2.4 Channel Impulse Response

Each time offset of the SMF is multiplied by the square root of the DPP. The resulting function is the time varying impulse response for one mode. The process outlined above is repeated for each mode and the impulse responses summed to give the channel impulse response, $h(t, \tau)$ (Figure B-3). In this example, modes can be seen at delays of ~ 2 and ~ 9 ms. The channel response is displayed for a time period of 2 s, and shown on an arbitrary amplitude scale. The more rapid amplitude variation (i.e. faster fading) of the ~ 9 ms mode indicates that it has had a larger Doppler spread imposed upon it.

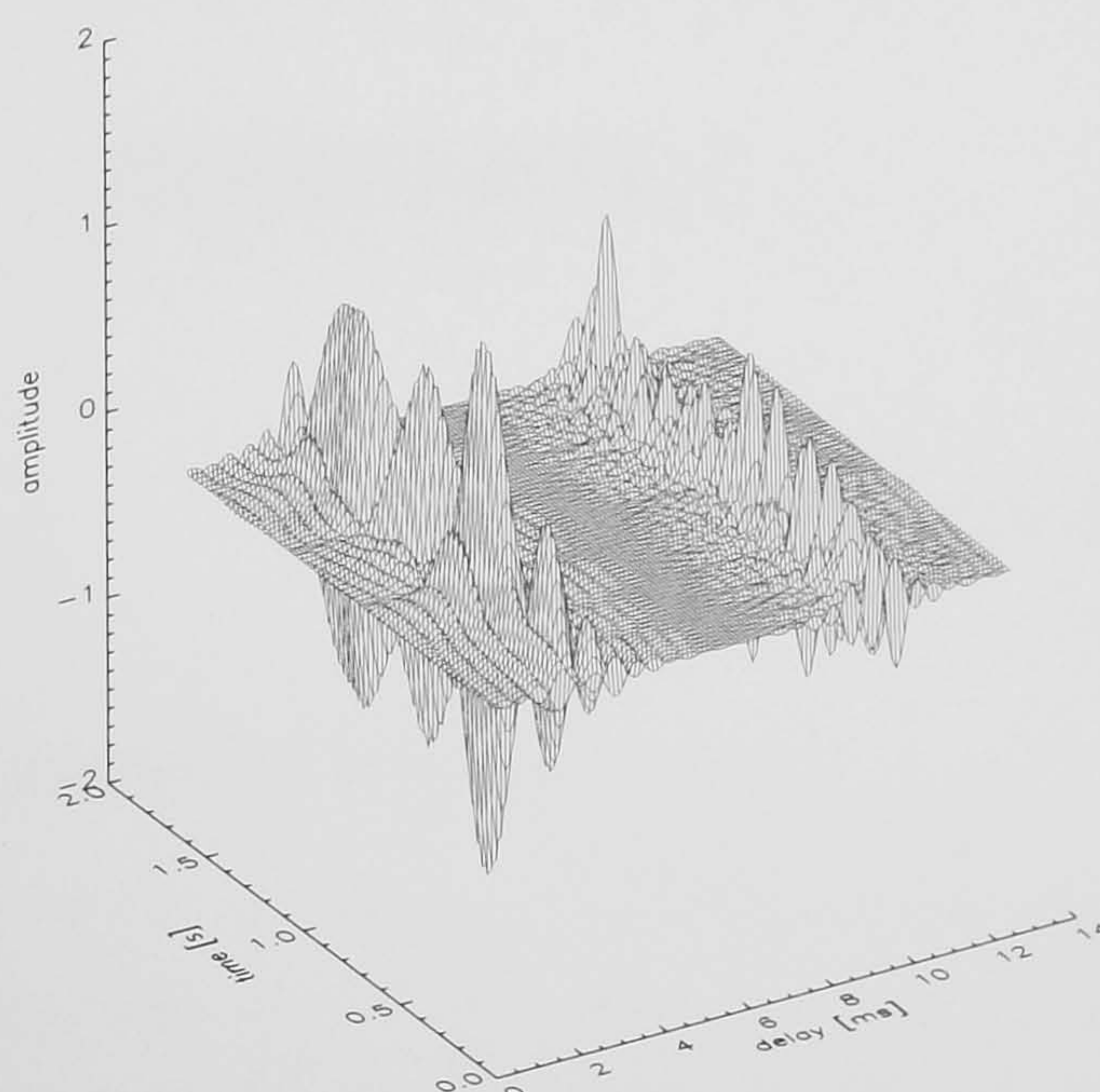


Figure B-3 Impulse response for two modes

B.3 Scattering Function

In order to more easily visualise the propagation conditions on the channel, it is possible to produce the channel scattering function ($S(f, \tau)$) from the impulse responses. The scattering function describes the way in which the signal power is distributed in the Doppler and delay domains. It is defined as the Fourier transform (over the time domain) of the autocorrelation of the impulse response; i.e. to produce the scattering function the power spectrum of the impulse response must be found at each delay offset.

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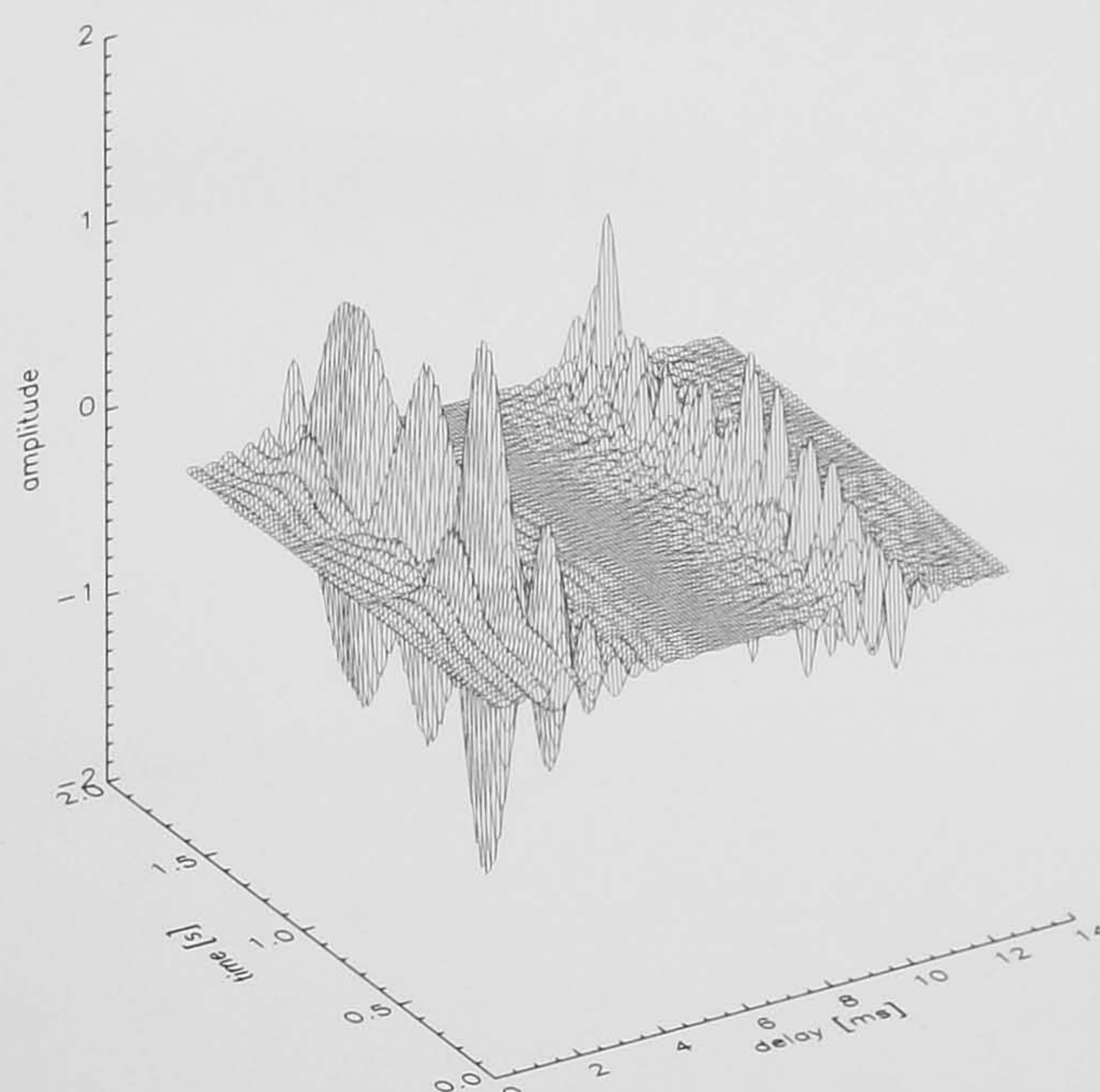


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$$S(f, \tau) = \left| \int_{-\infty}^{\infty} h(t, \tau) e^{-i2\pi f t} dt \right|^2 \quad (B-6)$$

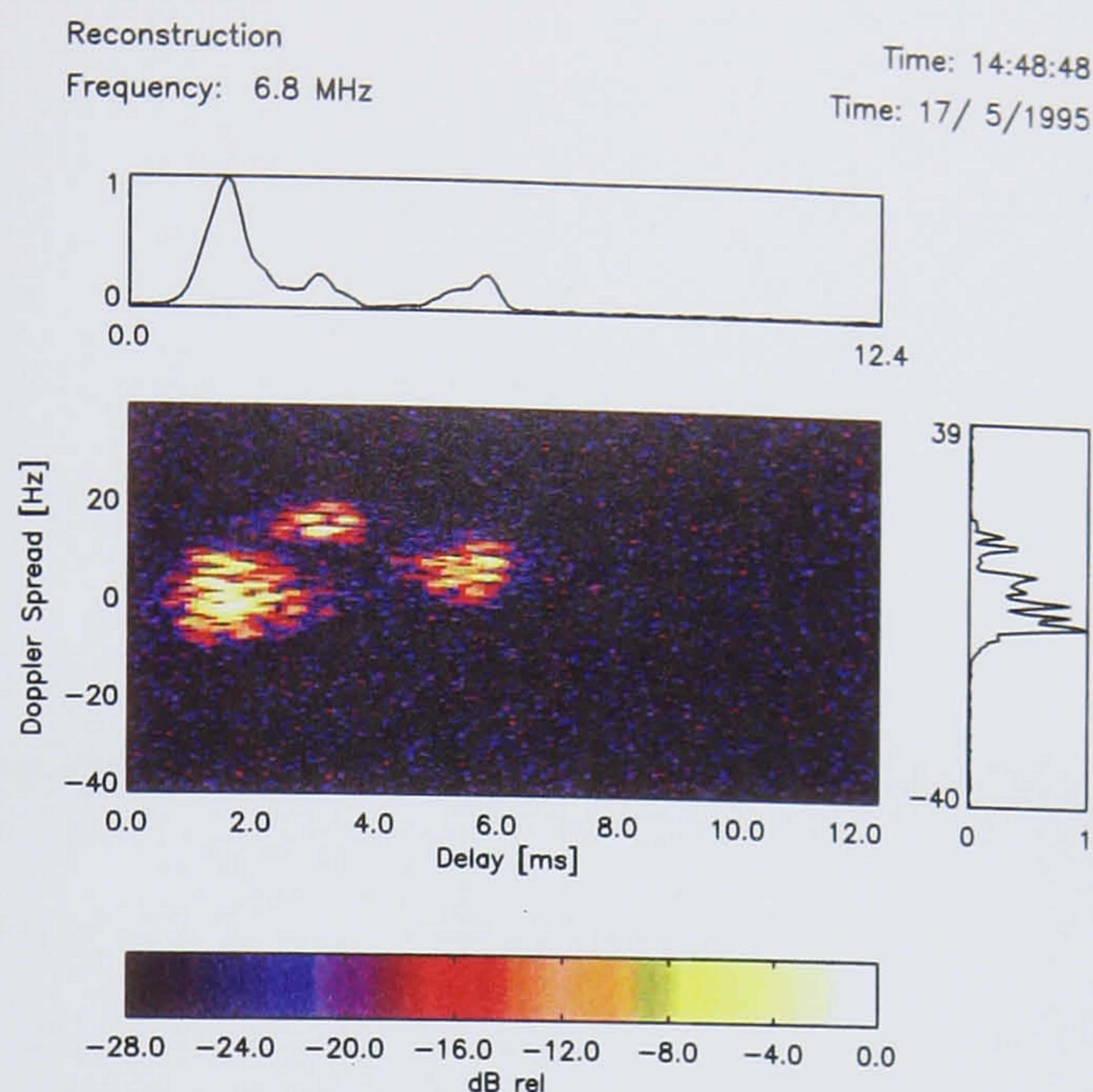


Figure B-4 Reconstructed scattering function

B.4 Veracity of the ITS Wideband Model

The ITS wideband model is capable of reproducing good approximations of the macroscopic features that have been observed on a variety of HF channel measurements. However, the choice of DPPs and SMF for wideband HF system evaluations is unclear as few real measurements have previously been made and so only a limited data base exists. Of more significance, it remains unclear how the fading within a single propagation mode should actually be related as a function of delay time - the ITS model assumes that fading is uncorrelated with delay time but it is not clear that this is truly the case. As it stands, the ITS model also does not include the ability to reproduce features which vary as a function of carrier frequency (e.g. mode group delay slope, group delay slope variation) but which may readily be observed in measured ionograms (and indeed HF propagation models).

Appendix C.

Characterisation of a High Performance Conventional HF

Receiver

C.1 Introduction

Measurements have been made on a high performance commercial HF receiver in order to characterise it and to establish the ‘state-of-the-art’ for traditional narrowband super-heterodyne designs. The receiver measured was a Racal Communications type RA3701 [Racal, 104] which is anecdotally regarded (by professional HF communicators) to be one of the best performing receivers available. This receiver is a classical two conversion design with IFs at 41.4 MHz and 1.4 MHz. The receiver in its standard configuration (and as measured) does not have sub-octave filters. It has a front-end RF amplifier to improve sensitivity which may be used or bypassed from the user interface. All measurements were made at the 1.4 MHz second IF as interest was focused on the receiver’s front end performance rather than any degradation in subsequent processing. The following characteristics were measured:

- **Sensitivity** – Receiver’s ability to receive weak signals;
- **IP_{3IN}** - 3rd Order Intermodulation Intercept Point
- **IP_{2IN}** – 2nd Order Intermodulation Intercept Point
- **Blocking Dynamic Range (BDR)** - the ability to receive weak signals in the presence of strong signals removed in frequency by several Megahertz.
- **Instantaneous Dynamic Range (IDR)** – the instantaneous linear dynamic range of the receiver.
- **Image Rejection** - ability to reject strong out-of-band signals which is a measure of the rejection provided by the front end filter.

C.2 Sensitivity (Noise Figure)

The RA3701 sensitivity was measured using the test set up illustrated in Figure C-1. An HP8645A RF signal generator was used to introduce a signal into the receiver tuned to the same frequency. FFT analysis of the 1.4 MHz IF output was used to measure the resulting power spectral density.

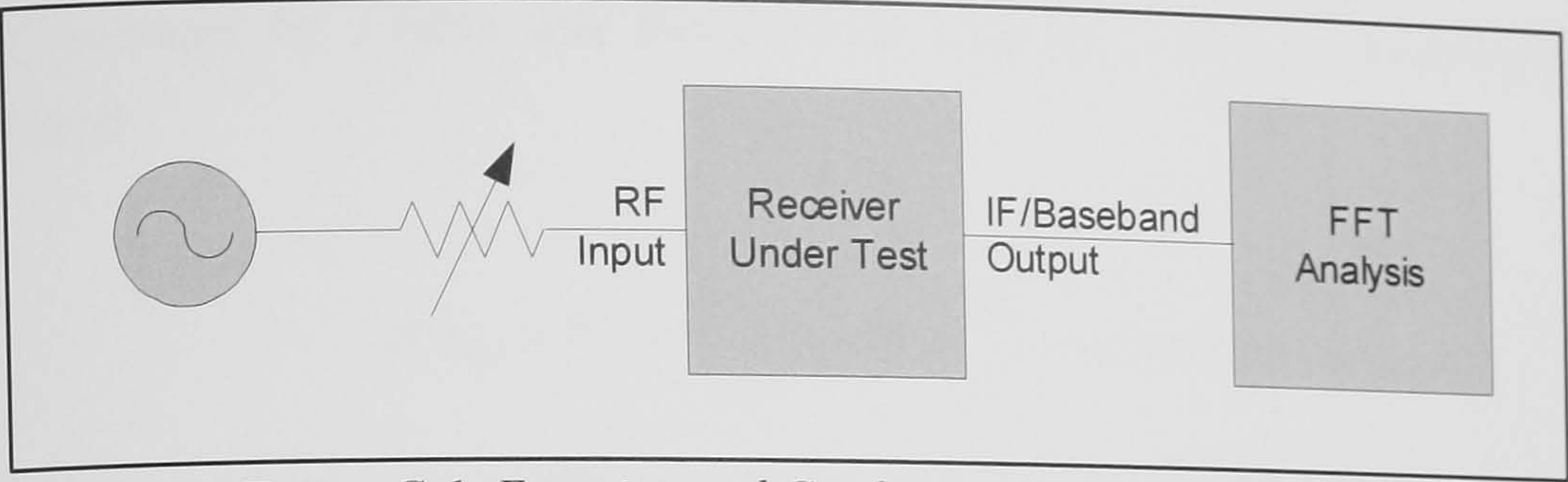


Figure C-1 Experimental Configuration to Measure Receiver Sensitivity

The receiver IF output level for a -110 dBm input signal, was found to produce a 50 dB SINAD in 1 Hz (Figure C-2) with the receiver's RF pre-amplifier off. This is equivalent to a 14 dB noise figure (or a sensitivity of -115 dBm for 10 dB SINAD in 3 kHz bandwidth). With the RF pre-amplifier switched on the noise figure improved by 6 dB.

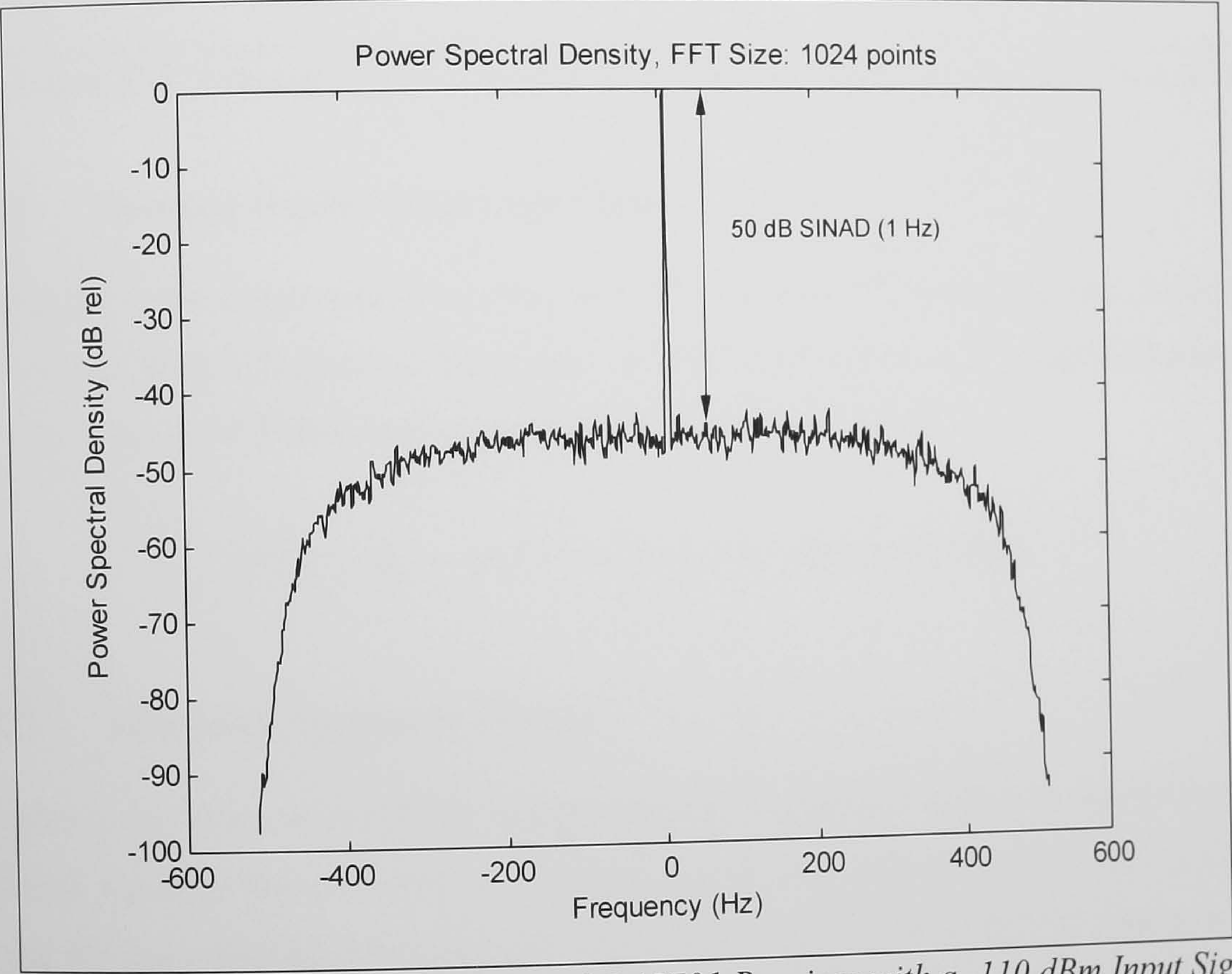


Figure C-2 Sensitivity of Racal RA3701 Receiver with a -110 dBm Input Signal

C.3 Third Order Intercept Point

The RA3701's $IP3_{IN}$ was measured using the experimental configuration shown in Figure C-3 using two HP8645A signal generators. The RA3701 was set to manual IF gain to disable its AGC in order to obtain an accurate measurement. The level of the 3rd order IMD product generated in the receiver IF pass band produced by two -15 dBm

tones separated by 1 MHz was found to be -90 dBc. $IP3_{IN}$ is therefore easily calculated:

$$IP3_{IN} = P_{IN} + \frac{IMD}{2} = -15 + \frac{90}{2} = +30 \text{ dBm}$$

With the receiver RF pre-amplifier switched on $IP3_{IN}$ falls to +25 dBm.

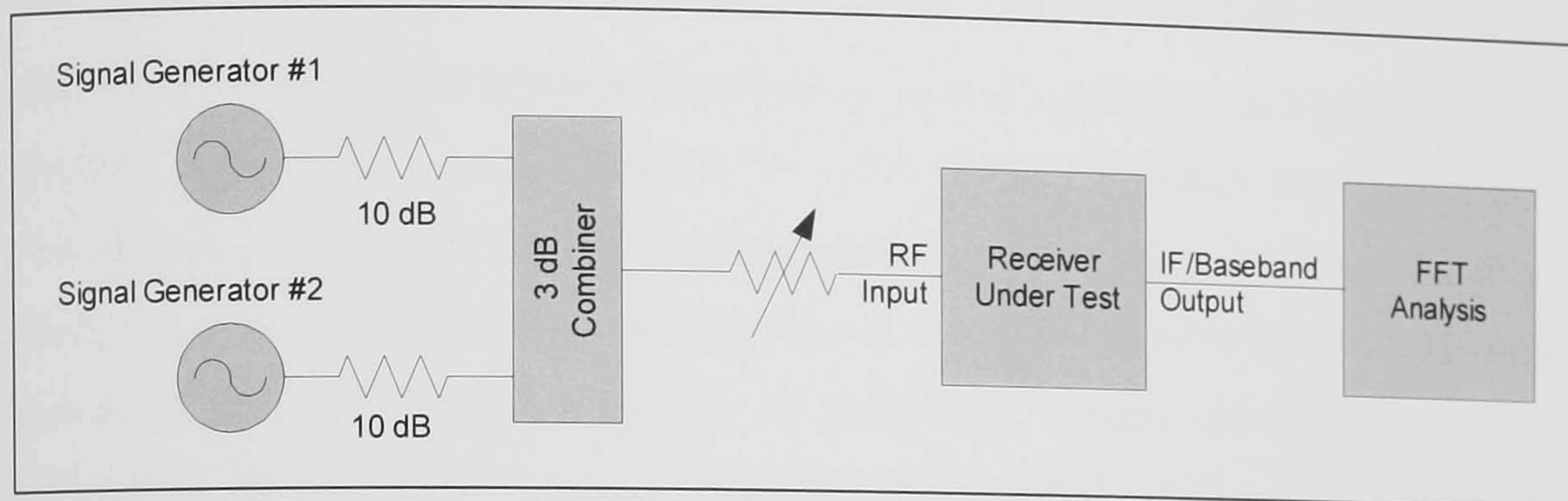


Figure C-3 Experimental Configuration to Measure Receiver Intercept Point ($IP3_{IN}$)

C.4 Second Order Intercept Point

Using the same experimental configuration the receiver 2nd order intercept point was measured. With -15 dBm 6.3 MHz and 7.2 MHz input signals a 2nd order IMD product of -102 dBm at 14.5 MHz was measured. $IP2_{IN}$ was calculated:

$$IP2_{IN} = P_{IN} + IMD_2 = -15 + (-15 - -87) = +57 \text{ dBm}$$

C.5 Blocking Dynamic Range

Blocking dynamic range (BDR) is a measure of a receiver's ability to receive a weak wanted signal in the presence of a strong signal. The RA3701 BDR was measured using the experimental configuration illustrated in Figure C-4 using two HP8645A RF signal generators. The measurement was made by applying a -110 dBm wanted signal at 10 MHz (receiver tuned to this frequency) and applying an interferer at 25 MHz whose power was varied. The resulting receiver response was measured by FFT analysis of the receiver's 1.4 MHz output. Receiver AGC was switched on.

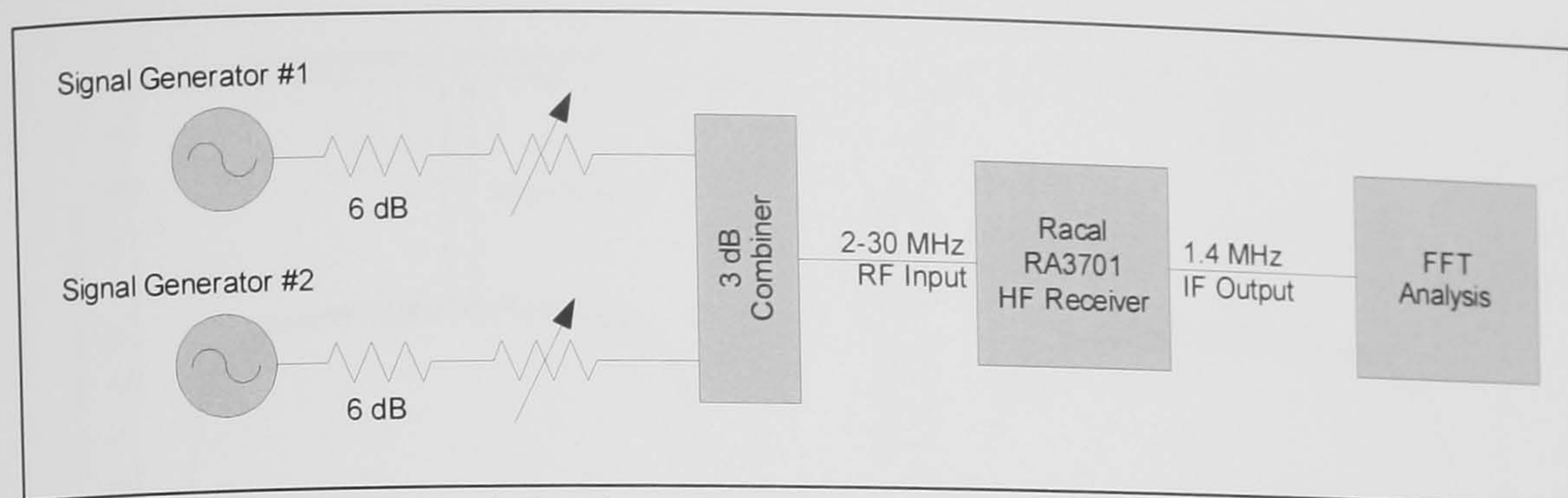


Figure C-4 Experimental Configuration to Measure Receiver Blocking Dynamic Range

The result of the test for different interferer powers is reproduced in Figure C-5. The RA3701 noise figure was measured to be 14 dB (see above) which is a noise floor of -160 dBm/Hz. As can be seen the receiver starts to be de-sensitised when the interferer reaches a power of -12 dBm and any increase in unwanted signal level above this value results in a commensurate reduction in sensitivity. Hence the receiver BDR is 148 dB/Hz (the difference between -160 dBm and -12 dBm) which is a BDR of 113 dB in a standard 3 kHz bandwidth. It is therefore concluded that a digital receiver with good sensitivity (noise floor < -155 dBm) and a zero attenuation clipping level of around -10 dBm will have an acceptable (i.e. comparable) blocking performance.

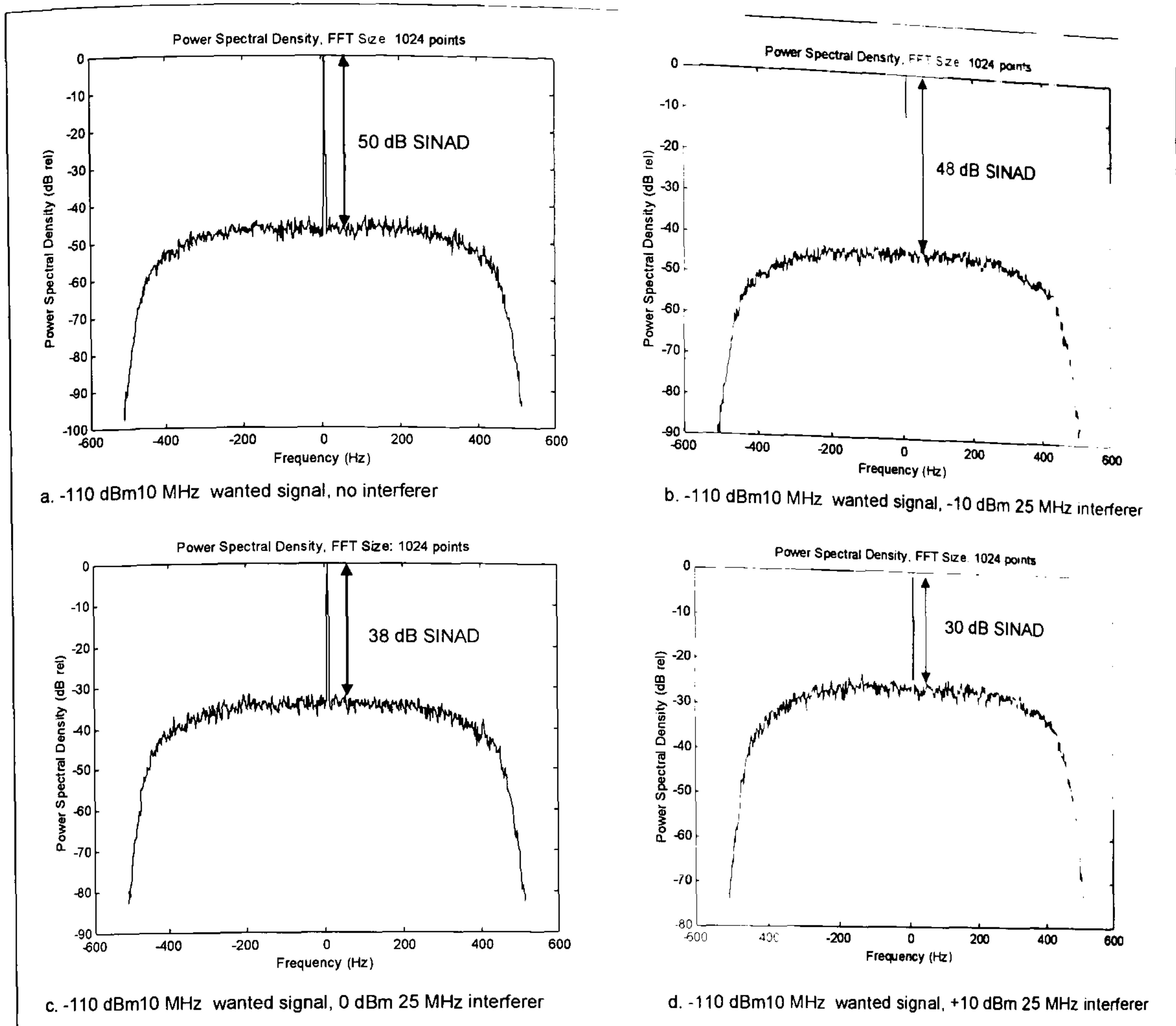


Figure C-5 Blocking Performance Measured at 1.4 MHz IF Output of RA3701 Receiver

C.6 Instantaneous Dynamic Range

The receiver's instantaneous dynamic range (IDR) was characterised by measuring the output power from the receiver as the input signal power of a single on-channel tone was varied between -120 dBm and 0 dBm. The measurements were made with the receiver in a manually controlled IF gain mode and repeated for IF gain settings between 25 and 250 (no units). The results (Figure C-6) indicate a maximum IDR of ~75 dB (depending on the gain setting).

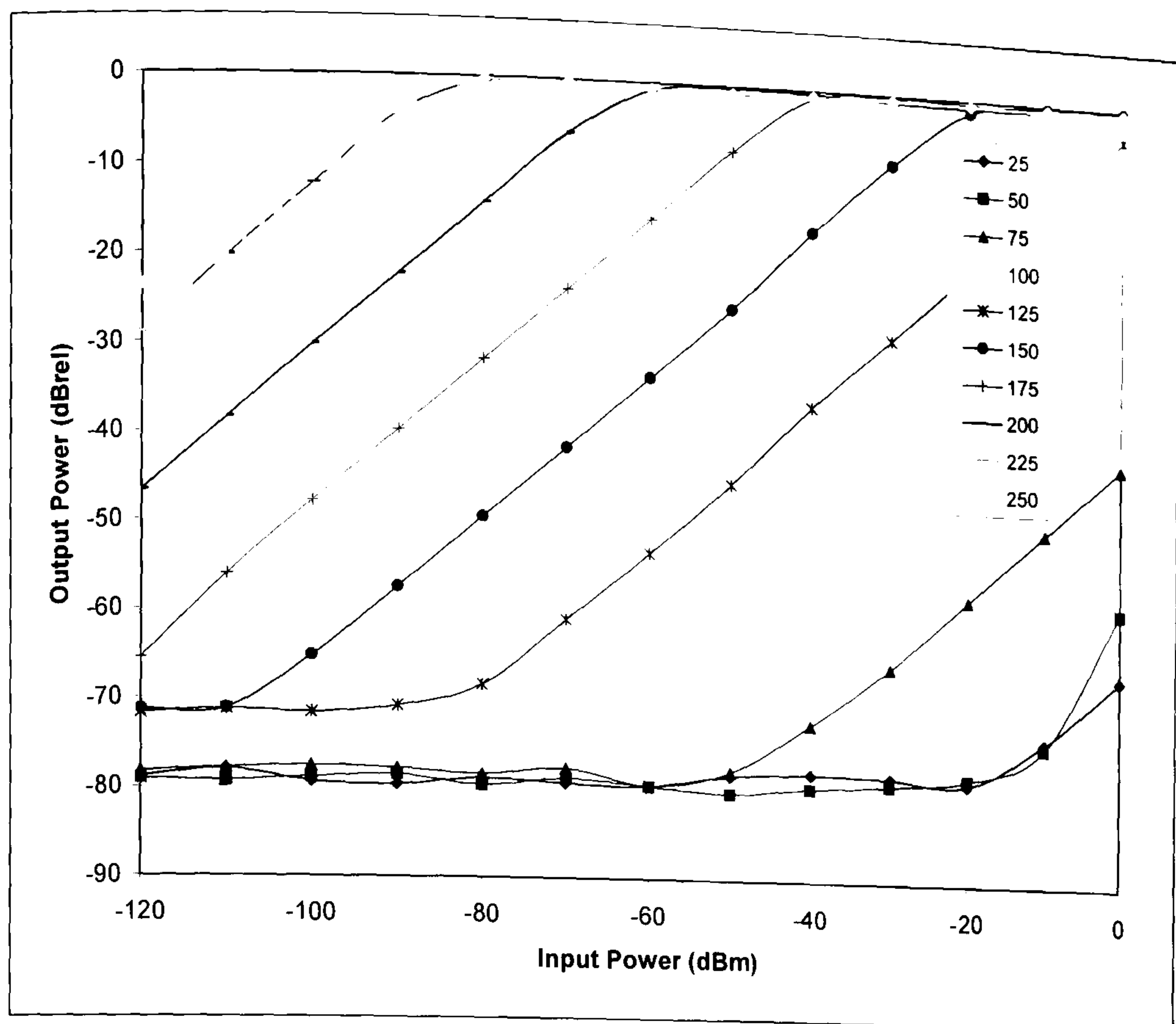


Figure C-6 Measured Instantaneous Dynamic Range (IDR) of RA3701 Receiver for a Range of IF Gain Settings

C.7 Image Rejection

The RA3701's ability to reject a strong out-of-band signal at the first mixer image frequency was measured. In this receiver the 1st mixer image rejection is all due to the receiver's front end filtering ahead of the mixer. The measurement was made using the experimental configuration in Figure C-4. It was found that with the receiver tuned to 10 MHz, a -8 dBm interferer applied at 92.7995 MHz produces an image signal in the receiver IF pass band having an equivalent signal strength to a wanted -118 dBm signal at 10.001 MHz. This is illustrated in Figure C-7. Note that, due to the receiver's frequency plan the 1.4 MHz IF is inverted in frequency). So, the receiver front end filter provides an effective 110 dB of rejection (the difference between the signal powers).

It is concluded that a digital receiver with an anti-aliasing filter that provides 110 dB of rejection in the second Nyquist zone will provide performance at least as good as the high quality commercial receiver tested. Additional attenuation of image frequencies will, in many cases, be provided by the HF antenna installation's frequency response. It is concluded that the performance required of the low pass anti-aliasing filter design

required to achieve equivalent performance to a good conventional receiver is somewhat less challenging than may have initially been anticipated.

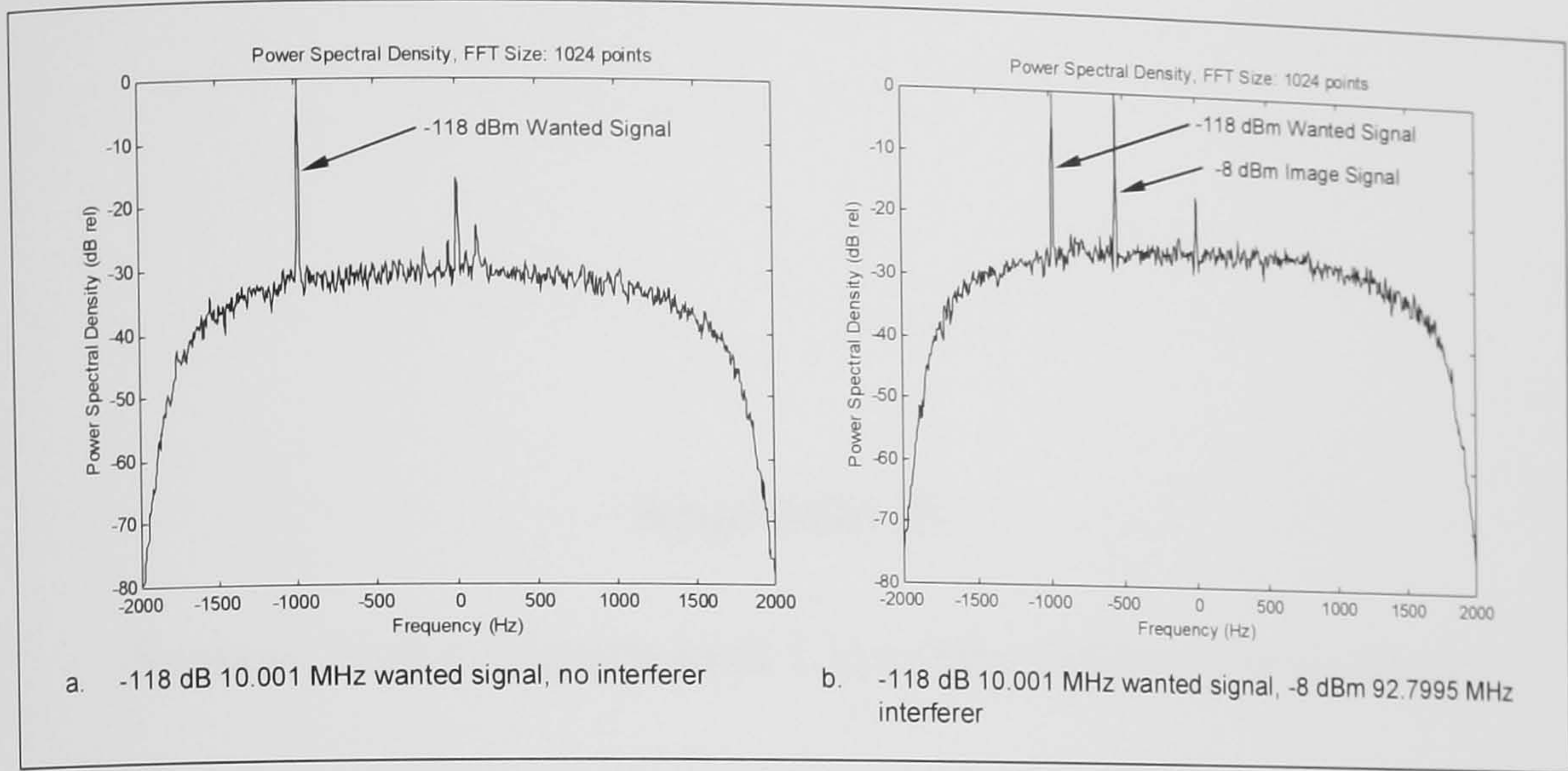


Figure C-7 Measured Image Rejection of RA3701 Receiver 1st Mixer

C.8 Summary of Super-heterodyne Performance

The performance of the RA3701 receiver RF front end is summarised in Table C-1. The measured results are compared with the published specification [Racal, 104].

Parameter	Specification (RF Pre-amp off)	Specification (RF Pre-amp on)	Measured (RF Pre-amp off)
Noise figure	14 dB	10 dB	14 dB
IP3 _{IN}	+32 dBm	+25 dBm	+30 dBm
IP2 _{IN}	Not specified	Not specified	+57 dBm
Blocking Dynamic Range	Not specified	Not specified	113 dB (3 kHz) 148 dB (1 Hz)
Instantaneous Dynamic Range	Not specified	Not specified	75 dB
Image Rejection	>90 dB	>90 dB	110 dB
Reciprocal Mixing (1 st LO Phase noise)	-96 dBc @ 20 kHz offset -106 dBc @ 80 kHz offset	-96 dBc @ 20 kHz offset -106 dBc @ 80 kHz offset	Not measured

Table C-1 Racal RA3701 High Performance HF Receiver Performance

Appendix D.

System Noise Figure and Linearity (Intermodulation)

D.1 Introduction

This appendix provides a summary of a number of key concepts and equations relied upon in the body of the thesis relating to the sensitivity (noise floor) and linearity of devices and systems.

D.2 Thermal Noise Power and Noise Figure

Thermal noise is generated as a result of the thermally excited random motion of free electrons in a conducting medium. It can be shown [e.g. Stremmer, 61 p199] that any practical device will have a noise floor which cannot be less than that due to the equivalent thermal noise power generated in a matched voltage source. This thermal noise power density, is given by:

$$\text{Thermal Noise Power Density} = 10 \log_{10}(kT_0) \quad \text{dBW / Hz} \quad (D-1)$$

where

k is Boltzmann's constant (1.38×10^{-23} J/K); and

T_0 is the system temperature in degrees Kelvin.

Any practical device will generate a higher level of noise than this. For convenience this additional noise is related to the thermal noise power at the device input by the noise figure, NF:

$$NF = 1 + \frac{T_e}{T_0} \quad (D-2)$$

where

T_e is the effective noise temperature of the device.

NF is unit-less and commonly expressed in decibels.

D.3 System Noise Figure – Noise Figure of Cascaded Devices

It is useful to be able to calculate the composite noise figure of a system as a whole from the parameters of the devices making it up (Figure D-1). The cascaded noise figure is given by:

$$NF_{TOT} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_2 G_1} + \frac{NF_4 - 1}{G_3 G_2 G_1} + \dots \quad (D-3)$$

where

NF_n is the noise figure of the n 'th cascaded device; and

G_n is the gain of the n 'th cascaded device.

Note that this calculation must use the linear noise figure and gain values. A general observation is that in most practical systems the impact of the earliest stages on overall noise figure is the greatest.

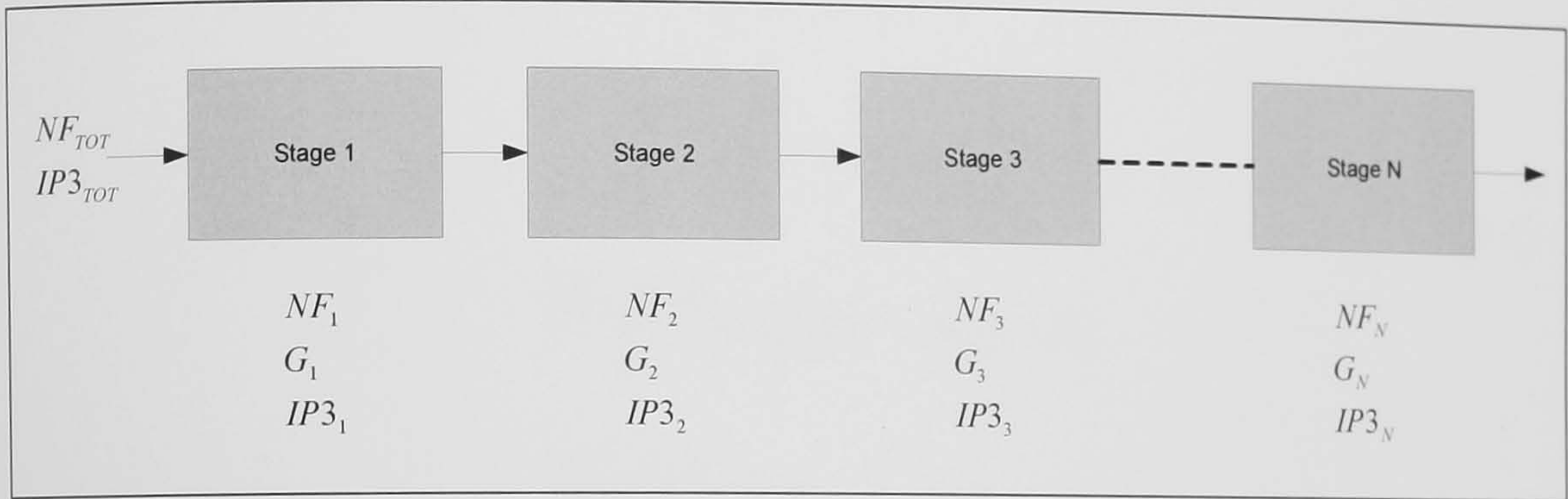


Figure D-1 Noise Figure and Intercept Point of a System of Cascaded Devices

D.4 Harmonic and Intermodulation Characteristics of non-Linear Devices

Signal processing devices, such as amplifiers and mixers, are non-linear to at least some degree and may in many cases be characterised as having a transfer function of the form:

$$y(t) = K_1 x(t) + K_2 x^2(t) + K_3 x^3(t) + \dots K_n x^n(t) \quad (D-4)$$

If such a device is excited by two signals simultaneously of the form:

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t + \phi) \quad (D-5)$$

then an output will be generated including all possible products. The most significant of these are (obtained by expansion using trigonometric identities):

$$K_1 [A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t + \phi)] \quad (D-6)$$

which represent the first order terms,

$$NF_{TOT} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_2 G_1} + \frac{NF_4 - 1}{G_3 G_2 G_1} + \dots \quad (D-3)$$

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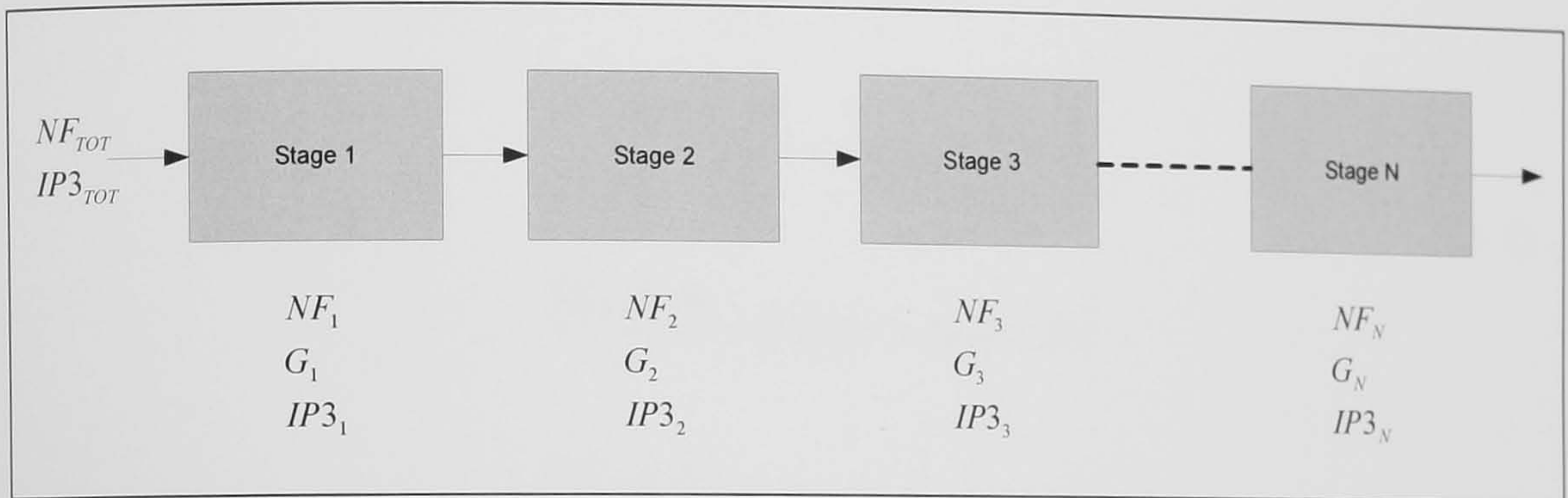


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$$K_1 [A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t + \phi)] \quad (D-6)$$

which represent the first order terms,

$$\begin{aligned}
 & \frac{K_2 A_1^2}{2} \cos(2\omega_1 t) \\
 & \frac{K_2 A_2^2}{2} \cos(2\omega_2 t + 2\phi) \\
 & K_2 A_1 A_2 \cos[\omega_1 t - \omega_2(t + \phi)] \\
 & K_2 A_1 A_2 \cos[\omega_1 t + \omega_2(t + \phi)]
 \end{aligned}
 \tag{D-7}$$

which represent the second order terms, and

$$\begin{aligned}
 & \frac{3K_3 A_1^3}{4} \cos(3\omega_1 t) \\
 & \frac{3K_3 A_2^3}{4} \cos(3\omega_2 t) \\
 & \frac{3K_3 A_1^2 A_2}{4} \cos[2\omega_1 t \pm \omega_2(t + \phi)] \\
 & \frac{3K_3 A_1 A_2^2}{4} \cos[2\omega_2(t + \phi) \pm \omega_1 t]
 \end{aligned}
 \tag{D-8}$$

the most significant third order terms. In many cases the remaining 3rd and higher order terms are negligible and may be ignored.

It can immediately be seen from the above that as the power of the input signals is increased the resulting harmonics and intermodulation distortion (IMDs) products will have different slopes according to their order. Second order products follow a square law increasing in power by 2 dB per dB increase in the input power. Third order terms increase by 3 dB/dB. Hence the concept of an intercept point can be evolved to characterise the power level at which the intermodulation products will theoretically have the same power as the fundamental outputs (Figure D-2). The intercept point can be referenced to the devices input or output, the output intercept point merely being factored by the device power gain. This is a point that cannot usually be reached as a device will normally go into compression first (where the fundamental outputs no longer linearly increase with the input signal). Intercept point is commonly measured using a two tone test. In its simplest form two, same power tones, are applied to a system and the resulting IMD products are measured. Then, the n 'th order intercept point (referenced to the input) can readily be calculated [Kundert, 101]:

$$IPn_{IN} = P_{IN} + \frac{IMD_n}{n-1} \text{ dBm} \quad (D-9)$$

where

P_{IN} is the input power of each of the two tones (dBm); and

IMD_n is the power of an n 'th order IMD product relative to a fundamental (dBc).

The 1 dB compression point (P1) is defined as the point at which the output is 1 dB reduced to that expected for linear operation.

Despite not being directly measurable, intercept points provide a key measure of the performance of a device. Given the device noise figure, the spurious free dynamic range (SFDR) can readily be calculated. SFDR is defined as the spurious free signal range from the noise floor to the point at which the 3rd order intermodulation products exceed the noise floor.

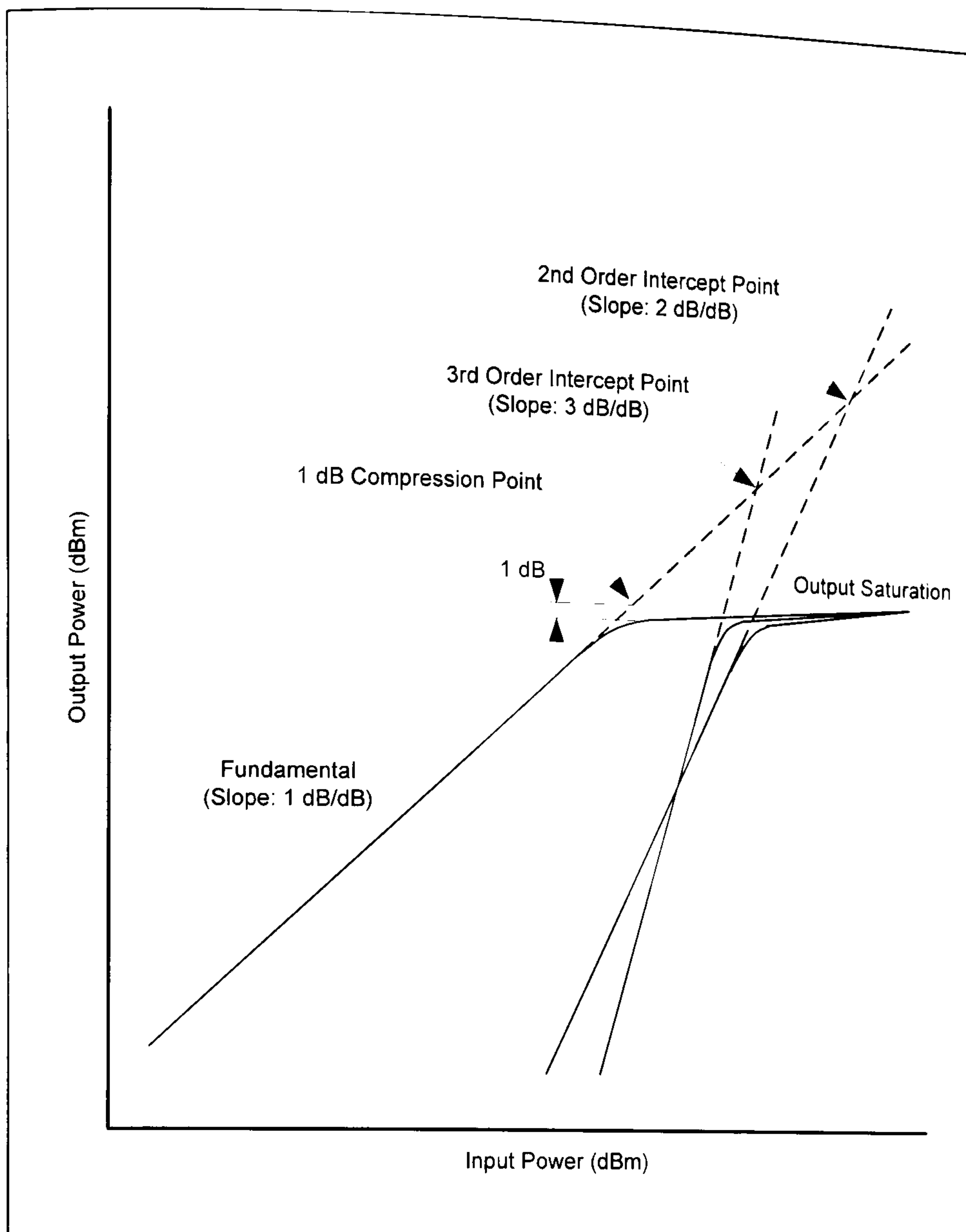


Figure D-2 Response of a non-Linear Device showing Compression and Extrapolated Intercept Points

D.5 System Intercept Point – Cascaded Non-Linear Devices

The intercept point of a system due to that of the cascaded devices making it up (Figure D-1) is given by:

$$\frac{1}{IP_{TOT}} = \frac{1}{IP_{IN1}} + \frac{G_1}{IP_{IN2}} + \frac{G_2 G_1}{IP_{IN3}} + \frac{G_3 G_2 G_1}{IP_{IN4}} + \dots \quad (D-10)$$

where

IP_{INn} is the input intercept point of the n 'th cascaded device; and

G_n is the power gain of the n 'th cascaded device.

Note that it is necessary to use the linear terms for gain and intercept point (rather than their decibel equivalent) in the above equation. A general observation is that in systems with gain the IMD performance of the later stages can have the biggest impact on the overall system intercept point.

Appendix E.

Calculation of Jitter Due to Oscillator Phase Noise

E.1 Introduction

It is typical for oscillator phase noise to be specified in terms of noise density relative to the fundamental at a number of frequency offsets (such as illustrated in Figure E-1) and taking the performance between these specification frequencies as being straight line segments when plotted on a log-log graph.

In order to determine the equivalent phase jitter requires the phase noise contributions to be integrated. The appendix provides a derivation of how this may be achieved and discusses the selection of appropriate limits for that integration.

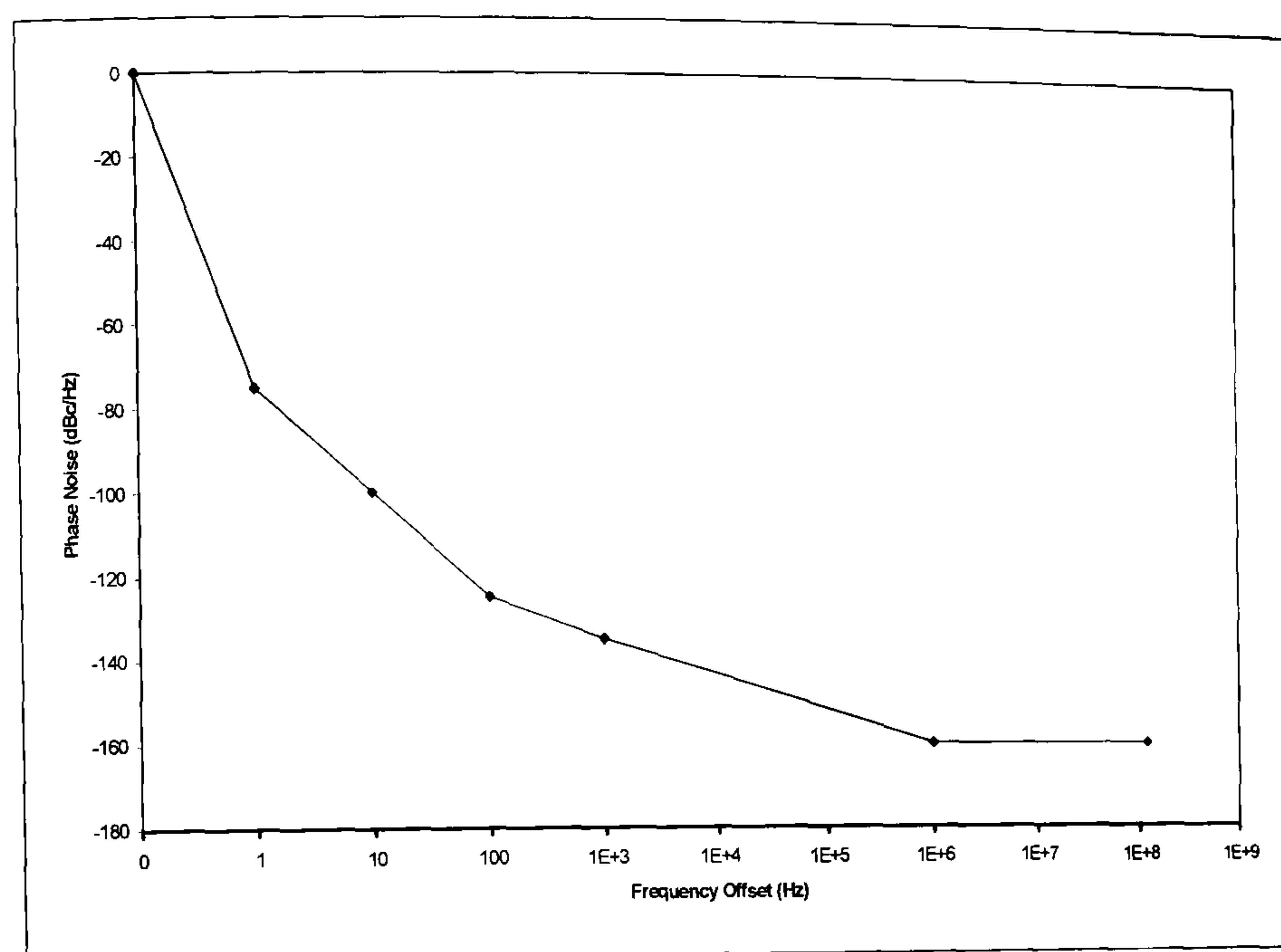


Figure E-1 Typical Oscillator SSB Phase Noise Specification

E.2 Derivation of Integrated Jitter Calculation

Integrated phase jitter variance due oscillator noise is given by [Robins, 109]:

$$\bar{\phi}^2 = \int_b^a \left(\frac{2N_{op}}{C} \right) df \quad \text{rads}^2 \quad (E-1)$$

where

$\left(\frac{N_{op}}{C} \right)_f$ is the SSB phase noise density at frequency, f , relative to the oscillator fundamental

If the noise is white over this frequency interval then:

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It is typical for oscillator phase noise to be specified in terms of noise density relative to the fundamental at a number of frequency offsets (such as illustrated in Figure E-1) and taking the performance between these specification frequencies as being straight line segments when plotted on a log-log graph.

In order to determine the equivalent phase jitter requires the phase noise contributions to be integrated. The appendix provides a derivation of how this may be achieved and discusses the selection of appropriate limits for that integration.

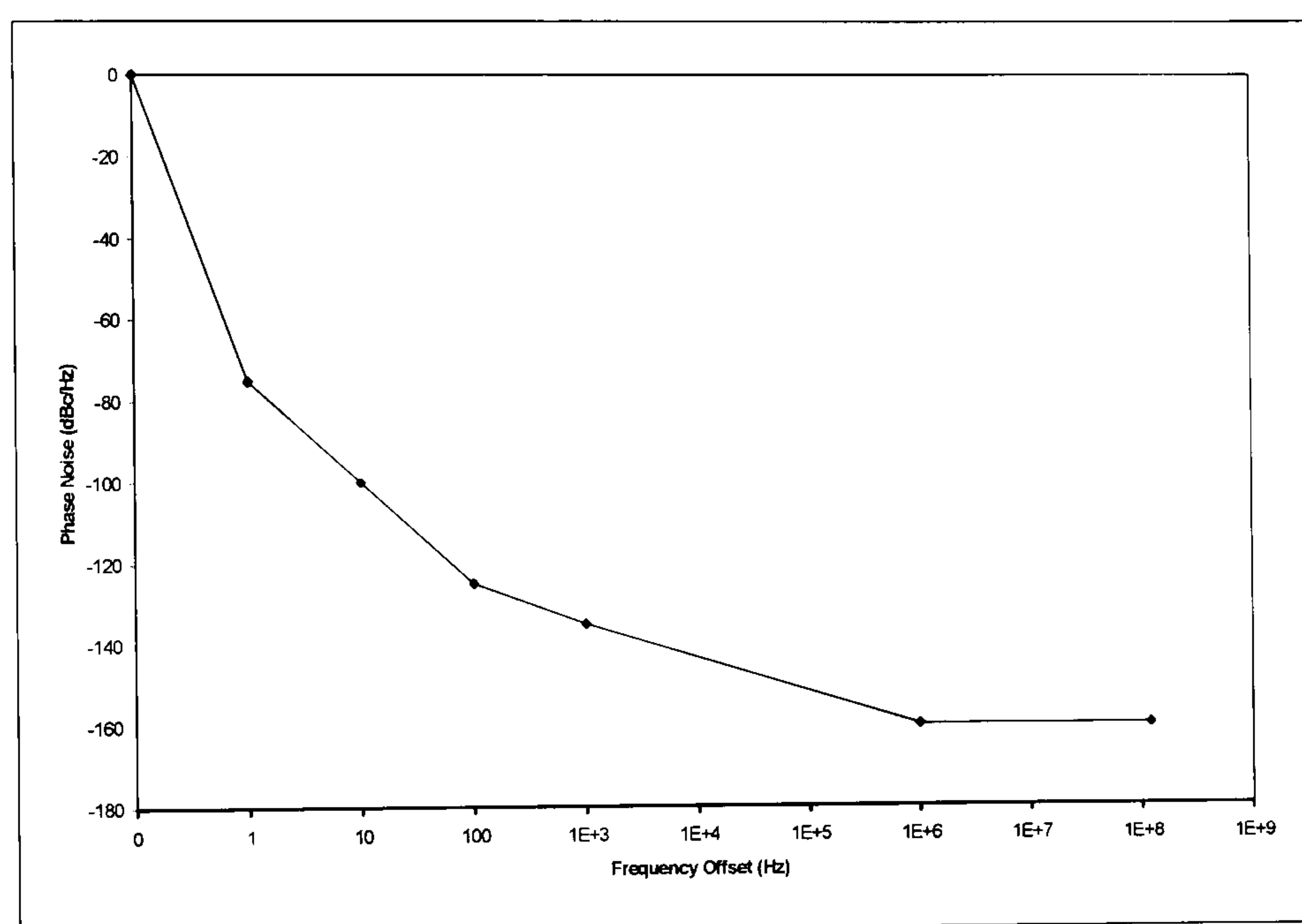


Figure E-1 Typical Oscillator SSB Phase Noise Specification

E.2 Derivation of Integrated Jitter Calculation

Integrated phase jitter variance due oscillator noise is given by [Robins, 109]:

$$\overline{\phi}^2 = \int_{-b}^{+b} \left(\frac{2N_{op}}{C} \right) df \quad \text{rads}^2 \quad (E-1)$$

where

$\left(\frac{N_{op}}{C} \right)_f$ is the SSB phase noise density at frequency, f , relative to the oscillator fundamental

If the noise is white over this frequency interval then:

$$\bar{\phi}^2 = \frac{2N_0}{C} b \quad \text{rads}^2 \quad (E-2)$$

In order to determine the integrated jitter contribution from a line segment of the phase noise specification between two frequencies, f_a and f_b , it is possible to define a gradient, n , such that:

$$n = \frac{\log\left(\frac{N_{op}}{C}\right)_a - \log\left(\frac{N_{op}}{C}\right)_b}{\log\left(\frac{f_b}{f_a}\right)} \quad (E-3)$$

Therefore the phase noise density at any frequency, f , can be written:

$$\therefore \left(\frac{N_{op}}{C}\right)_f = \left(\frac{N_{op}}{C}\right)_a \left(\frac{f_a}{f_f}\right)^n, \quad f_a \leq f \leq f_b \quad (E-4)$$

Writing an expression for the integrated jitter variance over an interval:

$$\bar{\phi}^2(f_a \rightarrow f_b) = \int_a^b \left(\frac{2N_{op}}{C}\right)_f df \quad (E-5)$$

And given eq.(E-4):

$$\bar{\phi}^2(f_a \rightarrow f_b) = \int_a^b \left(\frac{2N_{op}}{C}\right)_{f_a} \left(\frac{f_a}{f}\right)^n df \quad (E-6)$$

$$\therefore \bar{\phi}^2(f_a \rightarrow f_b) = \left(\frac{2N_{op}}{C}\right)_{f_a} \left(\frac{f_a}{f}\right)^n \frac{1}{1-n} \left[f^{1-n}\right]_a^b, \quad n \neq 1 \quad (E-7)$$

In this problem, the singularity which occurs when $n=1$ is not a physical limitation and can be practically avoided by setting $n=0.95$. A sensitivity analysis in a practical case has shown an impact of $\ll 1$ dB on the final results.

The total integrated phase jitter for an oscillator can be written in terms of a number of these line segments:

$$\therefore \bar{\phi}^2(f_{\Delta\min} \rightarrow f_{\Delta\max}) = \phi^2(f_a \rightarrow f_b) + \phi^2(f_b \rightarrow f_c) + \phi^2(f_c \rightarrow f_d) + \dots \quad (E-8)$$

Thus the RMS phase jitter due to phase noise between $f_{\Delta\min}$ and $f_{\Delta\max}$ offset from the fundamental can be written:

$$\therefore \bar{\phi}_{RMS}(f_{\Delta \min} \rightarrow f_{\Delta \max}) = \sqrt{\phi^2(f_{\Delta \min} \rightarrow f_{\Delta \max})} \quad rads \quad (E-9)$$

E.3 Selection of the Minimum and Maximum Frequency Offsets in Phase Noise Analysis

Carefully selecting the frequency bounds to consider analysing the impact of phase noise is important. In particular a judgement is required when considering energy close to the fundamental. It is useful to consider the problem in terms of short term stability (phase noise beyond a certain frequency offset from the fundamental) and long term stability (contributions between the fundamental and this frequency). In terms of a modem or a PRBS channel sounder the boundary is of the order of the time taken to pass a block of symbols or to make a single measurement respectively. Long term stability may be considered in terms of frequency drift for a modem or the timing accuracy to make a series of well timed measurements in a sounder. In practice, for the work described in this thesis, 1 Hz was selected as a suitable bound.

Equally, an outer bound must be selected. This is most easily selected based on the maximum bandwidth present in the system. For a wideband system (many Megahertz), given an oscillator with a good wideband phase noise specification (e.g. Figure E-1) the selection of this bound has a minimal impact on the overall integrated phase noise (jitter). For the calculations presented in this thesis for the wideband digital transceiver the bound was selected as the ADC sampling frequency (~62 MHz).

Appendix F.

Equalisation of Amplitude and Phase Distortion in a Channel

Sounder

F.1 Introduction

This appendix describes how a simple transversal linear equaliser can be formulated to correct amplitude or phase perturbations caused within the transmitter or receiver equipment used within the sounder. This includes such processes as analogue filtering and amplification.

F.2 Correction Using a Transversal Equaliser

If, for the transmission of a band-limited sampled signal, s_m , the associated received signal is x_n , then, for a time invariant distortion (such as caused by the presence of non-linear components in the sounder), a linear (FIR) equaliser can be defined in terms of its coefficients, a_k , such that:

$$\begin{bmatrix} x_0 & x_{-1} & x_{-2} & \dots & x_{-2N} \\ x_1 & x_0 & x_{-1} & \dots & x_{-2N+1} \\ \vdots & \vdots & \vdots & & \vdots \\ x_{2N-1} & x_{2N-2} & \vdots & & x_{-1} \\ x_{2N} & x_{2N-1} & x_{2N-2} & \dots & x_0 \end{bmatrix} \begin{bmatrix} a_{-N} \\ \vdots \\ a_0 \\ \vdots \\ a_N \end{bmatrix} = \begin{bmatrix} s_{-N} \\ \vdots \\ s_0 \\ \vdots \\ s_N \end{bmatrix} \quad (F-1)$$

This may be re-written in matrix form, viz:

$$XA = S \quad (F-2)$$

and may be readily solved:

$$A = X^{-1}S \quad (F-3)$$

Such an equaliser is usefully implemented following the pulse compression matched filtering in a sounder receiver. The processing overhead can be minimised by convolving the matched filter coefficients and the equalisation coefficients leaving only the initial task of determining the equaliser coefficients in the first place.

Appendix G.

Key HF Communications Standards

G.1 Introduction

This appendix includes a non-exhaustive list of many of the key HF communication standards in widespread use or in-development. The majority of these are military standards but many are suitable for wider application.

G.2 Existing HF Standards

STANAG 4203 - 'Technical Standard for Single Channel HF Radio Equipment'. This is a Tri-Service standard. The standard specifies radio system parameters for voice and radio teletype (RATT) operation.

STANAG 4285 - 'Characteristics of 1200/2400/3600 Bits Per Second Single Tone Modulators/Demodulators for HF Radio Links'. This is a tri-service military standard for serial tone modem waveforms.

STANAG 4197 - 'Modulation and Coding Characteristics that must be Common to Assure Interoperability of 2400 bps Linear Predictive Encoded Digital Speech Transmitted over HF Radio Facilities'. This is the 39-tone modem used with the LPC-10 vocoder of STANAG 4198.

STANAG 4198 - 'Parameters and Coding Characteristics that must be Common to Assure Interoperability of 2400 bps Linear Predictive Encoded Digital Speech'. This specifies an LPC-10 vocoder.

STANAG 4415 - 'Characteristics of a Robust Non-Hopping Serial Tone Modulator/Demodulator for Severely Degraded HF Radio Links'. This is a tri-Service standard. This standard describes a very robust 75 bps in-band spread spectrum serial tone modem waveform.

STANAG 4444 - 'Technical Standards for a Slow-Hop HF EPM Communications System'. This Tri-Service standard contains many waveforms for operations under a considerable range of conditions. User data rates range from 75bps to 2400bps.

STANAG 5066 - 'Profile for High Frequency (HF) Radio Data Communications'. This is a standard detailing sub-network interface matters and containing an ARQ protocol.

STANAG 4538 - 'Technical Standards for an Automatic Radio Control System for HF Communications Links'. This Tri-Service standard is a major advance on currently

available automated systems for frequency selection, link establishment and link maintenance.

STANAG 4539 - 'Technical Standards for Non-hopping HF Communications Waveforms'. This Tri-Service Standard contains fixed-frequency waveforms for operation under a considerable range of conditions. User data rates will range from 75bps to (currently) 9600bps (with optional uncoded operation at 12800bps).

MIL-STD-188-110A - US Military Standard for 'Interoperability and Performance Standards for Data Modems'. This comprises a range of data-rates from 75bps to 4800bps. It is an existing standard.

MIL-STD-188-141A - US Military Standard for 'Interoperability and Performance Standards for Medium and High Frequency Radio Equipment'. This existing standard contains requirements for basic radio performance and the requirements for the current US Automatic Link Establishment (ALE) system.

FED-STD-1052 – US federal standard for data communications which uses modems equivalent to MIL-STD-188-110A but has a unique ARQ standard defined.

G.3 New HF Standards

MIL-STD-188-110B - This standard was issued in 2000 and is an improved version of the existing 110A standard. It includes high data rate serial-tone waveforms providing up to 9600 bps (and 12.8 kbps uncoded) on-air data rate over conventional 3 kHz channel allocations, and 19.2 kbps over ISB channels (nominally 6 kHz).

MIL-STD-188-141B - This standard was issued in 2000 and is an improved version of the existing 141A standard. It includes a 'third' generation ALE system which is a subset of the functionality specified in STANAG 4538.

ETSI TS 201 980 Digital Radio Mondiale (DRM); System Specification – Top level specification for an LF, MF and HF digital broadcasting standard including source coding, modem waveforms and protocols.